MARCH 2001

1) CH1 + CH2 UP OFF SCREEN — POSITION NOT WORKING ?
2) CURSOR FOR RIGHT ?

CH1 = OK

CH2 = VARIABLE ADDS DC OFFSET ↑

11 = POSITION MOVES GOOD CHANNEL — ↕ — NOT ACTIVE TRACE ↑

TRIGGER LEV.

June 98

1) SUSPECT U209 DAC - NO O/P ✓
2) REPLACE R297 + 298 - WRONG VALUE INSTALLED (10K) SHOULD BE 11K5 ✓
3) 12V MISSING ON PIN 13 OF U209 - TRACE BLOCKED ✓
4) POSITION NOW OK ON CH2 BUT DRIFT SET TO GND. ✓
ALSO NO SIGNAL GETTING THROUGH CHANNEL

ALSO VARIABLE NEEDS TO BE AT ONE END OF TRAVEL + ADDS DC OFFSET

SUSPECT Q127. NOW OK ✓

FAULT WITH Q127 HAVING SIGNAL LOSS

TEST JFET. O.

S/C DRAIN — SOURCE

5) + DC OFFSET ON VARIABLE AT CH2. ?
6) VERT DATUM DRIFTS TO LEFT. — BIAS FAULT ON F/P BOARD.
7) TRIGGERING PROBLEMS ON CH2. OFF SCREEN + NO LOCKING OF TRIG.

Contents

Introduction

This service manual is written primarily for the service engineer who is performing a standard recalibration or who is undertaking repairs when the instrument has developed a fault. The system overview will help the engineer to understand the inner workings of the 1600 series.

The manual covers both the 1604 and 1602 models, the 1602 being treated as a 1604 with CH3 and CH4 not fitted.

The fault-finding procedure given in this manual takes a systematic approach. Starting with the symptoms, the engineer is led to the area or areas at fault by a series of questions in the form of several flowcharts. These require no knowledge of the system, although a basic knowledge of electronics is essential. Throughout the manual a reasonable level of understanding is assumed.

Many of the complex operational functions of the 1600 series have been designed in at chip level. The system includes four large semi-custom digital gate arrays: three handling the acquisition of data and the other controlling the display of alphanumerics and trace information. On the analog side there are two semi-custom analog I.C.s which control the generation of the realtime timebase ramp and the trigger source and coupling selection. When fault-finding, they can be treated as 'Black Boxes' so alleviating some of the more difficult servicing tasks.

Should a problem arise whilst servicing the instrument expert help and advice is available from Gould (see inside the rear cover for details).

1.0 SAFETY AND POWER REQUIREMENTS

International Safety Warning
(as required for I.E.C. 348 Class I)

This manual contains information and warnings which must be observed by the user to ensure safe operation and retain the apparatus in a safe condition. The instrument has been designed for indoor use within the specified limits of temperature, i.e. 0 to 50 deg. C. It should not be switched on if there are obvious signs of mechanical damage and it should not be used under wet conditions.

Grounding

The instrument must be operated with a protective ground connected via the appropriate yellow/green conductor of the supply cable. This is connected to the instrument before the line and neutral supply connections when the supply plug is inserted into the socket on the back of the instrument. If the final connection between this and the supply is made elsewhere, the user must ensure the ground connection is made before line and neutral.

If any supply cable other than that supplied with the instrument is used, it must carry an adequate protective ground conductor.

Any interruption of the protective ground conductor inside or outside the instrument is likely to make the instrument dangerous. Intentional interruption is prohibited.

Signal connections into the instrument should be connected after and disconnected before the protective ground connection is made, i.e. the supply lead must be connected at all times that signal leads are connected.

Live Parts

The instrument is safe to operate with covers fitted and these must not be removed under normal usage. The covers protect the user from live parts and they should be removed only by suitably qualified personnel for maintenance and repair purposes.

WARNING: *Removing the covers may expose voltages in excess of 8500V on the PDA cap at the front of the tube on the left side. Also, voltages above 2000V can occur, in particular at the rear of the tube, even when the instrument has been disconnected from the power source for some time.*

Ventilation and Dust

The instrument relies on convection and fan assisted cooling and must not be operated in a position which restricts air flow through the ventilation slots in the sides and rear of the instrument. The instrument should not therefore be used in a tightly fitting rack as this will limit ventilation. Adequate ventilation can usually be achieved by leaving an 8cm gap around the top, rear and sides of the instrument. The instrument should not be operated in dusty environments.

Operating Temperatures

The instrument is designed to be operated in an environment having an ambient temperature of between 0 deg. C and 50 deg. C. The instrument is specified to operate with full accuracy within a temperature range of 15 deg. C to 35 deg. C.

Note: The use of the instrument in strong direct sunlight or next to radiators and other heat sources may markedly increase the temperature at the instrument and this should be taken into account when assessing the viability of using the instrument in a given environment.

Power and Frequency Requirements

The instrument is designed to consume less than 100W and operate from supply voltages of between 110V and 265V, with mains tap switching.

It will operate at supply frequencies of between 48Hz minimum and 400Hz maximum.

Under the extreme conditions of 110V and 48Hz, the instrument will still operate properly even if there is a half cycle dropout in the mains supply.

Fuse Requirements

The following fuse arrangement must be followed:

* one 0.5A (at 240V) or 1A (at 120V) slow-blow fuse on the rear panel;
* one 3A fuse in the mains supply plug (UK only).

Specification

Section 2

The specification for the 1602 is identical to that of the 1604, except CH3, CH4 are not present.

DISPLAY

CRT 8 x 10cm rectangular.
Internally Illuminated Graticule with 8 x 10cm divisions and 2mm sub-divisions.

Accelerating Potential 10kV.

Graticule Continuously variable illumination.

Trace Rotation By front panel preset.

Intensity Separate controls for traces and alpha-numerics.

VERTICAL DEFLECTION

Four identical input channels, CH1, CH2, CH3, CH4 (Invert provided for all channels).

NON-STORAGE

Sensitivity 2mV/div to 10V/div in 1-2-5 sequence. Programmable.

Accuracy ±2% of full scale.

Variable Sensitivity >2.5:1 (allows continuous adjustment of sensitivity between ranges).

Input Impedance 1MΩ/30pF.

Input Coupling DC-GND-AC Programmable.

Input Protection 400V DC or pk AC.

Vertical Position ±8 div Programmable.

HORIZONTAL DEFLECTION

NON-STORAGE

Sweep Rate 0.2μs/div to 10ms/div. 15 ranges in 1,2,5 sequence. Programmable.

Accuracy ±3% of full scale.

Expansion x5 gives fastest range sweep speed of 40ns/div.

STORAGE

Sweep Rate 50μs/div-200sec/div. 21 ranges in 1-2-5 sequence. Programmable.

Accuracy ±3% of full scale (display accuracy).

Horizontal Position Programmable.

Horizontal Expansion x1, x2, x5, x10, x20, x50, x100, x200.

TRIGGER

Variable level control with Auto/Normal Facility, with resolution of at least 1mm. In Auto the timebase free runs when insufficient signal (20Hz-20MHz) is present or when the selected level is outside the range of the input signal.

Source Internal CH1, CH2, CH3, CH4, Ext, Line. Programmable.

Slope −ve or −ve. Programmable.

Band Trigger 0 to ±4 div. Programmable.

Coupling DC, DCLP, AC, ACLP, TV Frame, TV Line. Programmable. LP Filter attenuates signals >15kHz.

Post-Trigger Delay

Timebase range	Max. Delay
10μs–2ms	100ms
5ms–200ms	10s
500ms–200s	1000s

Events 2-16383 trigger events.

Trigger divide by N (N=2 to 16383).

Post-Trigger Delay cannot be used for sweep speeds faster than 5μs/div in the Non-Storage Mode.

Pre-Trigger Programmable. 0.1 - 100% in 0.1% steps.

Trigger Sensitivity Programmable.

Internal	DC Coupled	<0.3 div to 2MHz
		<1.5 div to 20MHz
	AC Coupled	<0.3 div 10Hz to 2MHz
		<1.5 div 4Hz to 20MHz.
External	DC Coupled	<150mV to 2MHz
		<600mV to 20MHz
	AC Coupled	<150mV 10Hz to 2MHz
		<600mV 4Hz to 20MHz

External Input Impedance 100kΩ/10pF approx.

External Input Protection 250V DC or pk AC.

NON-STORAGE DISPLAY MODES

All Programmable

Bandwidth DC, DC-20MHz (-3dB)
AC, 2Hz-20MHz (-3dB).

Single Trace CH1 or CH2, or CH3 or CH4.

Multi-Trace Any combination of the four available channels in Normal, Chopped or Alternate Modes, are automatically selected by the Timebase.

Add CH1 + CH2 and/or CH3 + CH4.

Invert Any channel may be inverted. When used in conjunction with ADD Mode, it gives the algebraic difference of the two channels.

X-Y CH1 gives X, CH2, CH3 and CH4 give Y deflections.

Alpha-numeric display of input voltage range and timebase range.

STORAGE FACILITIES

ACQUISITION SYSTEM

Acquisition Memory 10k words per channel.

Maximum Sample Rate 20M samples/sec per channel when operating in single channel mode or CH1 and CH3 or CH2 and CH4 at 50μs/div. timebase range. 10M samples/sec per channel when operating at 100μs/div timebase range. Reducing with timebase range to 5 samples/sec at 200sec/div.

Vertical Resolution 8 Bits (1 in 256).

A-D Conversion Linearity Less than ±½ LSB error. Monotonic.

Single/Shot Acquisition Freezes memory at the end of triggered sweep. Programmable.

Peak Detection (Glitch Capture). Capture of positive and/or negative glitches 50ns pulse width when operating in single channel mode or CH1 and CH3 or CH2 and CH4 at 100ns pulse width in three and four channels operation. 100% probability of capture.

Bandwidth DC, DC-7MHz.
AC, 2Hz-7MHz.

STORAGE DISPLAY MODES

All Programmable.

Roll Stored data and display updated continually.

Refreshed Stored data and display updated by triggered sweep.

X-Y Display As Non-Storage. 8 bit x 8 bit (256 x 256).

Interpolation Linear.

Display Resolution 8-Bits x 1k per channel (256 x 1024).

Display Hold Freezes total store.

Channel Hold Freezes individual selected channel.

Datum Cursors Independent vertical and horizontal cursor lines.

Measurement Cursor Assigned to trace.

Cursor Measurement Display ΔV and ΔT displayed on screen.

Cursor Accuracy
Voltage ±2% H.L.S.B., resolution 0.4%
Time ±0.1%, resolution 0.01%
0.02% using expansion.

Trigger Indication Trigger level indication on-screen. On-trace trigger point bright-up indication.

MEMORY

Waveforms Two reference traces can be stored and displayed in addition to input channel displays.

Set-ups A total of 4 set-ups can be stored in non-volatile memory. Set-up 4 is not available with IEEE or RS423 options.

Retention Time The memory support is trickle charged and will retain information for 3 months after power-down.

INTERNAL SCREEN PLOTTER

Direct digital screen copy of waveforms with annotation of range scales, labels and graticule selected by menu.

Plot Size 89mm wide by 102mm long (approx.)

No. of Pens 4 color automatically selected.

Speed 50sec per trace (approx.)

ANALOG OUTPUT

Analog output of the stored displays for plotters and recorders.

Y Output Parallel output of up to 4 channels selected by channel ON/OFF controls. Serial output CH1 through CH4.
Amplitude 100mV/div via bnc connectors.
Accuracy ±5%.

X Output X ramp output.
Amplitude 100mV/div via bnc connector.
Accuracy ±5%.

Output Impedance 100Ω.

Output Sweep Rate Selected via Menu.
0.1 div/sec, 1.0 div/sec, 10 div/sec ranges.

Pen Lift isolated single pole contact closes from start of plot to the end of plot cycle.

Plot Mode Manual or Auto initiates a plot at the end of acquisition and re-arms the instruments at the end of the plot cycle.

DIGITAL PLOTTER OUTPUT

(Available with an Interface Option). The instrument can directly output to HPGL format plotters via the IEEE or RS423 Interface Ports.

Plot Mode Manual or Automatic after acquisition.

Colors Color pens automatically selected when available.

Labels Range scaling, measurements, labels and graticule information selected by menu.

MISCELLANEOUS

Calibrator 1V pk-pk ±1% approx. 1kHz.

POWER REQUIREMENTS

Voltage 100V, 120V, 22V and 240V.

Frequency 45-400Hz.

Power 70VA approx.

Weight 10kg approx. (22 lb approx.).

Dimensions See Drawing Below.

ENVIRONMENTAL

Temperature

Operating	0°C to 50°C
Full Specification	+15°C to +35°C
Storage Temperature	−10°C to +70°C

Humidity Tested to IEC 62-2-Ca operating at 45°C at 95%RH.
Tested to IEC 68-2-Db cycling.
Non-operating 25°C to 45°C, 95%RH.
6 cycles (144 hours)

Safety Designed for IEC 348 Cat 1 Standards.

ACCESSORIES SUPPLIED

Operating Handbook
Line Cord.

OPTIONAL ACCESSORIES

Probe Kit PB12 A passive probe kit with switched x1 and x10 attenuators.
Input impedance: 10MΩ/11.5pF (x10).

Probe Kit PB17 A x100 passive probe with 1.5m of cable.
Input impedance: 100MΩ/4.5pF.
Working voltage: 1.2kV pl AC.

Probe Kit PB20 A 250MHz modular probe kit with a x1 and x10 switched head.
Input impedance: 10MΩ/18pF (x10)
Working voltage: 600V pk.

Rack Mount Kit PN4091631.

Rack Mount Tray with slides PN04091632.

Cart TR7 General-Purpose Cart.

Protective Carrying Case PN04101176. (A strong padded case, enclosing the oscilloscope for transportation.)

Front Panel Cover PN04101177.

WAVEFORM PROCESSOR TYPE 160 (Optional)

Introduction

The 160 Waveform Processor adds a range of functions to the 1604, which increases the power of the instrument in terms of both capture and post-storage analysis and measurement functions.

SPECIFICATION

SIGNAL CAPTURE FUNCTIONS

Initialise Clears the repeat buffer and sets cursors to normal mode.

Signal Averaging Steps selectable from 1,2,4,8,16,32,64, 128,256,512 or 1024.

Capture & Repeat Arms the scope for a capture and automatically applies the post-storage functions of shift, magnification, filtering or integration, that have been selected since the last initialisation of the keypad.

TV Steup TV Line Configure the instrument to acquire a selected TV line. (Dependent on Transmission System).

Capture Arms the scope for a single capture.

Limits Testing The scope will either hold, or display a "TEST FAILED" message if the acquired signal goes outside a pre-defined test band.

POST STORAGE ANALYSIS FUNCTIONS

Filter 6 selectable stages of low pass filtering per timebase range.

$$\text{Cut-off Frequency} = \frac{15.92}{t} \ln\left(1 + \frac{1}{2^n}\right)$$

t = Timebase range in sec/div.
n = Selected by filter step.

Restore Effectively "undoes" the *last* post-storage trace manipulation.

Vertical Trace Magnification/Attenuation Multiplies trace from 0.06 to 4.00 times in 63 steps selectable by increment/decrement controls.

Invert Inverts the trace about the centre line.

Position Moves trace and datum in X and Y planes and cursor in X plane.

Integration Calculates the indefinite integral and displays the resultant waveform. The trace is auto-scaled.

Area Calculates the area under a curve with limits defined by the cursor and datum.

POST-STORAGE MEASUREMENTS

Rise/Fall Time Calculates rise/fall time of a signal; the 0% anmd 100% points are set by cursor and datum.

Overshoot Calculates overshoot of a signal as a percent of 100 point. 0% and 100% are set by cursor and datum.

Duty Cycle Calculates a duty cycle (ratio of mark to pulse period) as a percentage. Also calculates the average frequency and period of signal. Vertical datum defines the zero crossing or uses the mean of the waveform. Cursor and datum set measurement limits.

Pulse Width Calculates time between 50% points (or voltage datum if required). With the pulse "bracketed" between the time datum and cursor.

Max. Min Display maximum and minimum voltage excursion of a waveform relative to the vertical datum position. The cursor and datum "bracket" the waveform of interest.

Peak-Peak Calculates peak-to-peak voltage of the waveform bracketed between the cursor and datum.

RMS Calculates the root mean square (RMS) voltage of a waveform bracketed between the cursor and datum. The values are calculated with respect to both the vertical datum and the mean of the waveform.

Reference Memory Additional reference memories are available with the waveform processor module. Up to 50 x 1k or 5 x 10k, configured from menu.

Retention Time The module can be detached without losing the waveform data for at least 3 months.

Realtime Clock 24 hour and date set via menu. Stored with reference traces and plotted with digital output plots for record of acquisition time. The time is retained for at least 3 months with the power disconnected.

OPTION 103 – IEEE-488 INTERFACE

Read and Write Functions
All front panel controls with the exception of:
- Variable Timebase Non-Storage
- Variable Input Attenuation
- Power On/Off
- Trace Intensity
- Scale Illumination
- Trace Rotation
- Alpha-Numeric Intensity.

All menu selections are programmable.
Memory data is programmable.
On-screen alpha-numerics can be read.
Alpha-numeric 16 line x 32 characters are programmable for display messages.

OPTION 102 – RS423 (RS232) SERIAL INTERFACE

Two ports are provided:
1. Output only, e.g. for plotter or printer.
2. Input/Output for control as IEEE specification.

Baud Rate Selectable via menu. 110 to 9600.

ORDERING INFORMATION

1604 4 Channel Digital Storage Oscilloscope.
102 RS423 (RS232) Serial Interface.
103 IEEE-488 Interface.
160 Type 160 Waveform Processor.
105 Type 105 Waveform storage module.
PN04091631 – Rack Mount Kit
PN04091632 – Rack Mount Kit with slides.
PN04101176 – Protective carrying case.
PN04101177 – Front Panel cover.
Type TR7 – General Purpose cart.

INTERNAL PLOTTER CONSUMABLES

PN04101175 – Pack of 4 replacement pens, one of each color.
PN04101165 – Pack of 8 rolls of paper.

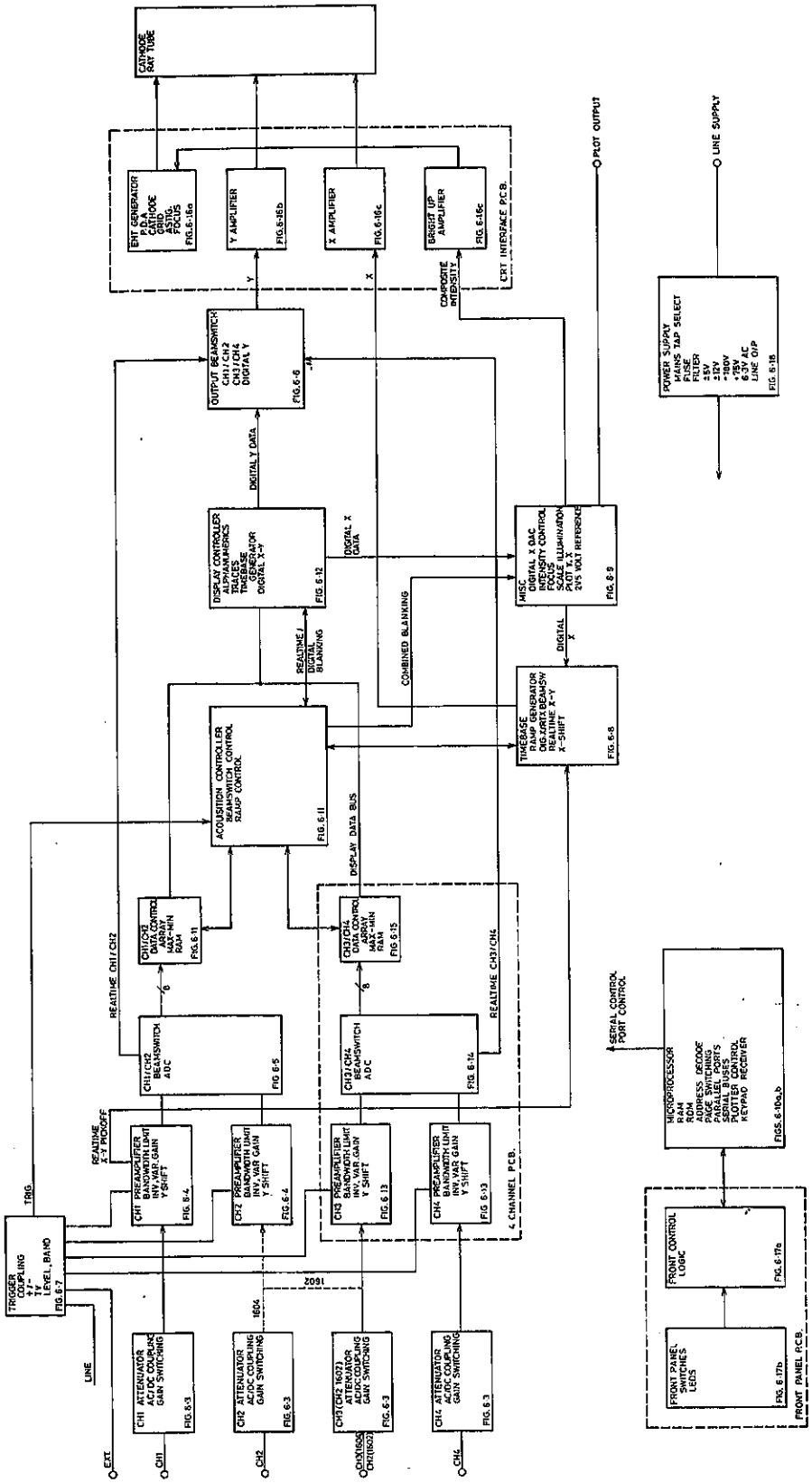


Figure 3.1 Main System Block Diagram

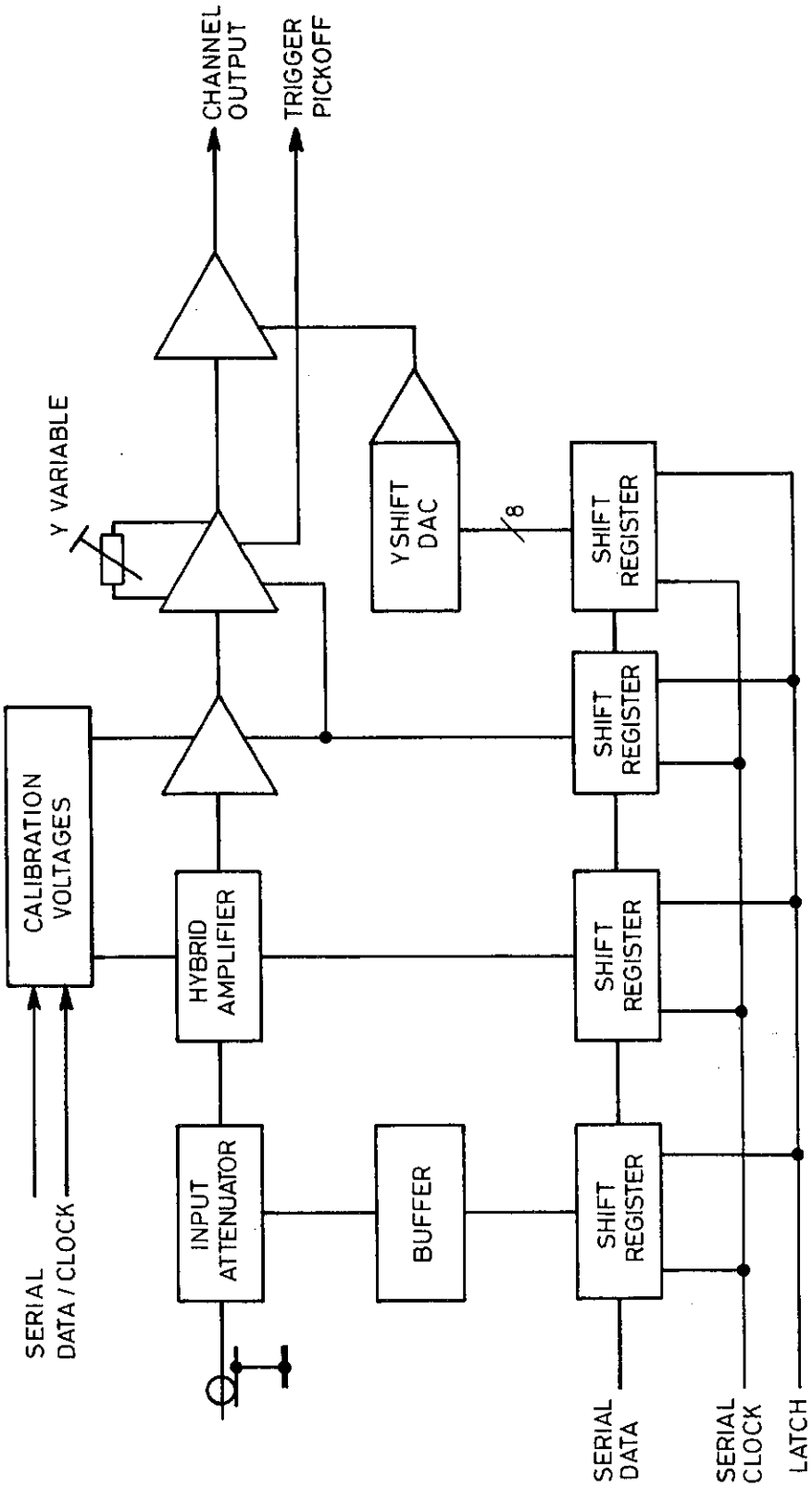


Figure 3.2 Pre-amplifier Block Diagram

3.0 SYSTEM OVERVIEW

The first step in understanding the operation of the 1600 Digital Storage Oscilloscopes is to gain an appreciation of how the signal is transferred from the input BNC to a trace on the display. In the 1600 there are two possible paths. The chosen route is dependent on the operation mode of the instrument as the paths are different in storage and non storage modes. Section 3.1 covers the storage mode path and Section 3.2 the non storage path. Following this, microprocessor control and triggering are covered in detail.

1602 is identical to 1604 except that CH3 and CH4 are not present.

3.1 FROM THE BNC TO THE SCREEN (Storage mode)

Pre-amplifier

The first circuit encountered by a signal after the input socket is the Input Attenuator. This performs the first step in converting the input signal, which has a wide dynamic range (from 10V/div to 2mV/div), to a signal of predetermined amplitude. This first circuit applies a 1:1 or a 100:1 attenuation to the signal. The degree of attenuation is set by the operator or the auto setup function when the input range is selected.

After this the signal passes into a hybrid circuit where further attenuation or gain is applied. The signal emerges from here at the required amplitude. Thus, if a sinewave of 5V pk-pk were applied with the input sensitivity set to 5V/div the same signal would appear at the output of the hybrid as a 2mV pk-pk sinewave applied with the sensitivity set to 2mV/div.

The signal then passes to the variable gain and invert amplifier. Both functions are produced in the same circuit: invert can be considered an extreme form of variable gain, where gain = −1.

Having produced a signal of the required amplitude, a pickoff is taken to the trigger circuit. This is before any Y shift is added. Y shift is controlled directly by the microprocessor and not with a potentiometer on the front panel. This control is in the form of a differential current which is added to the signal prior to the analog to digital conversion.

Analog to Digital Conversion

The 1600 contains two Analog to Digital Converters (ADCs) and when all four channels are operational each ADC converts two channels. This is achieved by rapidly switching the input of the ADC between two pre-amplifier outputs. The circuit that accomplishes this is known as a beam switch amplifier. It is at the output of the beam switch amplifier that the storage and non storage signal paths diverge (see Section 3.2 for discussion of the non storage path). In storage mode this multiplexed signal is fed into the ADC, which provides the digital data ready for storage. However, this digital output will contain alternate data from the two input channels.

When only two inputs are selected in the combination CH1 or CH2 together with CH3 or CH4, then each ADC receives input from only one channel. This enables the maximum acquisition rate to double. Also, the output from the ADC in this case is not multiplexed but contains digital data from only one channel

Glitch Capture and Data Storage

The data passes from the ADC to the Data Control gate array, a semi-custom device designed by Gould. If glitch capture is not selected then the data is merely demultiplexed, if necessary, and passed to the acquisition RAMs for storage.

When glitch capture is enabled, all the data received from the ADC during one sample period (the number of samples received is dependent on the timebase range) is fed into the Data Control gate array. This extracts from it the maximum, minimum or both depending on the selected glitch capture mode. This is passed to the acquisition RAM for storage rather than the last data sample as would happen if glitch capture were disabled.

The process of glitch capture and data storage is controlled by another gate array, the Acquisition gate array. Again, like the Data Control gate array, this device is a semi-custom logic circuit designed by Gould. The microprocessor sets the registers in this device which in turn determine how the Data Control gate array deals with the incoming data. The Acquisition gate array also controls the rate of acquisition, the beam switching of signals to the ADCs and the transfer of data from the acquisition RAM to the display RAM.

Data Transfer from Acquisition to Display RAMs.

Each acquired channel on the 1600 contains 10k (10240) bytes of data. The displayed trace, however, has only 1k (1024) points. When a trace is transferred from acquisition RAM to display RAM the 10k bytes are reduced to 1k bytes. There are two ways in which this is done: either every tenth byte is sent or a Max-Min function is applied to the acquisition store trace. This second option works in a similar way to the glitch detect function: it takes 20 samples and reduces these to two, a maximum and a minimum. Both of the above methods pass the data through the Data Control gate array to the Display gate array. The Max-Min function, when selected, is performed by the Data Control gate array.

From the Display RAM to the Screen

The Display gate array can control up to six screen traces and all of the alphanumerics. The data is held in the display RAMs. Each dot of display information, whether it be alphanumerics or trace, has a unique X-Y coordinate on the screen. To display a captured trace the gate array takes the stored data from the RAMs and presents it sequentially to the Y Digital to Analog Converter (DAC). In a similar manner the X position is set by sending a number generated by the gate array to another DAC, the X DAC.

The output of the Y DAC passes into the Y Output Beam Switch where dot join is added, if selected. There follows a two stages of amplification before the signal reaches the Y plates of the Cathode Ray Tube (CRT). The X DAC output takes a different route: the differential current from the DAC is converted into a voltage which passes through a selector (not a beam switch, it selects between CH1 for X-Y mode, the X DAC, or the real time ramp) and into the X output amplifier. The signal is amplified and applied to the X plates of the CRT. These X and Y signals produce the displays seen on the screen.

3.2 FROM THE BNC TO THE SCREEN (Non Storage)

The signal takes the same path through the attenuators, pre-amp and beam switch as in Section 3.1. When the signal reaches the ADC, a pickoff is taken to the Y output beam switch (this is the same circuit as referred to above). From here the signal is amplified and fed to the Y plates. There is a slight complication when alphanumerics are displayed: the Y output beam switch has to chop between the signal and the Y DAC output. To avoid flicker this switching is achieved by any of several different methods, the choice being dependent on the timebase range and the frequency with which triggers are being received.

The X signal in non storage mode is in the form of a ramp which sweeps the CRT spot from the left to the right of the screen. It is produced by a semi-custom analog I.C. and its associated components. The slope of the ramp is determined by the timebase rate, where the faster the timebase speed the steeper the slope.

3.3 MICROPROCESSOR CONTROL

There are few functions on the 1600 which are not controlled by the microprocessor. Those that are, are controlled by a variety of means.

8-bit Bus

The more complex functions within the 1600 are controlled directly from the 8-bit bus. These include control of the Acquisition and Display gate arrays, the RS423, GPIB and Plotter options (when fitted) and the front panel key scanning. Other functions are controlled indirectly from the bus; these use logic level control signals which are provided by ports and latches. The sort of functions controlled in this manner include the serial bus, plotter pen lift and dot join.

Serial Bus

The serial bus is a one-bit data stream with two associated clock signals. The data is extracted from the stream by a serial to parallel converter, i.e. a long shift register. This bus has some advantages over the 8-bit wide bus. Each device on the serial bus uses only three connections rather than the ten or more that are required with the 8-bit bus. So, fewer tracks are needed to distribute the information around the board and more output pins are available on the receiving device.

The serial bus controls such system functions as the attenuator relays, pre-amp control and the X shift and trigger level DACs.

Control Voltages

In addition to the functions that can be controlled by the digital signals provided by the serial and 8-bit buses, each pre-amp requires two control voltages. These are used in the self-calibration procedures to remove the offsets generated by the attenuators and the hybrids. The voltages are generated by a series of voltage output DACs which are part of the serial bus.

3.4 TRIGGERING

As with the pre-amplifier, the trigger circuits can be more easily understood by following the path from the input BNC to the trigger output.

The trigger can take its source from one of six places: Channels 1 to 4, External, and Line (mains frequency). The source and coupling selections are made within a semi-custom analog I.C. This provides two outputs, one going to the TV sync separator and the other to the trigger level circuit.

The TV sync separator extracts line and field pulses from the incoming TV waveform, which must be in NTSC, PAL or SECAM formats.

The trigger level circuit compares the trigger signal to two DC levels. Under normal operation the output of only one comparison is used, the +ve or −ve slope trigger output. However, when trigger band is operational, both outputs are combined to produce a trigger whenever the input signal passes into the selected band.

The digital output produced by the trigger level circuit goes directly to the Acquisition gate array where the more complex trigger functions are performed. These are: trigger delay by time, trigger delay by N events and trigger divided by N. This last function is used to provide TV line capture, where TV line coupling is selected and N is set to the number of lines in a field.

The Acquisition gate array initiates the start of a sweep or capture when the required number of triggers have been received and the delay conditions have been met.

4.0 CALIBRATION

Some of the features of the 1600 are maintained in calibration by the internal microprocessor. However, as with any other oscilloscope, it should have a regular annual calibration. The schedule given below uses a minimum of test equipment, all of which should be readily available in any test department.

The instrument will arrive fully calibrated. This will ensure that the instrument operates within specification for a period of not less than one year, under normal operating conditions (see Section 1.0). A few of the adjustments in the calibration procedure are interactive, i.e. the setting of one will affect the setting of others. In the schedule below it has been assumed that these controls will be set approximately correctly and require only a minor adjustment.

All controls are discussed individually with the exception of the Y Pre-Amplifiers, where only adjustments for Channel 1 are given. The setup of the other three pre-amplifiers is identical.

Calibration cannot be assured unless the entire schedule is completed in order.

Equipment Required

1. Four Digit Digital Voltmeter
2. General Purpose Oscilloscope
3. Oscilloscope Calibrator
4. Fast Edge Generator, Tektronic PG506 or similar
5. Capacitance Standardiser (30pF)
6. 50 Ohm input termination

1600 CALIBRATION SCHEDULE

For the 1602 models ignore references to CH3 and CH4 in the calibration procedure following.

Power Supply and Tube

WARNING *These controls are situated in areas containing high voltages, in some cases in excess of 8.5kV. Care should be taken to avoid touching any exposed tracks or components. All adjustments should be made with a suitably insulated tool.*

These preset adjusters can be found on the CRT Driver PCB at the side of the tube, see Figure 7.2 CRT Driver PCB Adjusters.

1. R88, EHT voltage adjustment. Using the DVM with a high voltage probe measure the voltage at the CRT cathode. This can be taken at R110 on the CRT Driver PCB. Adjust R88 to give a reading of 1600V.
2. R97, preset intensity. Select non-storage mode X-Y and set the alpha intensity control to minimum. Adjust the trace intensity control to give +8V at the wiper of the control pot. Adjust preset R97 to give a just visible spot. It may be necessary to adjust the X shift to bring the spot on the screen.
3. R109, preset focus. Select the Master Menu and set the front panel focus control to mid travel. Adjust preset R109 to give the best overall focus.
4. R112, astigmatism. Select non-storage mode Refresh and set both intensity controls to give a moderately low intensity display. Adjust preset R112 to give best overall focus, R109 may need slight re-adjustment to obtain the optimum display.

Trace Rotate

Using a small screwdriver adjust the trace rotation control through the hole in the front panel. Set this to give a horizontal trace.

Y Pre-amp DC Balance and Overall Gain

These adjusters can be found on the main PCB for CH1 and CH2, see Figure 7.1 Main PCB Adjusters and on the Four Channel board for CH3 and CH4, see Figure 7.3 Four Channel PCB Adjusters.

5. R177, DC balance. Short between L101 and L102, and adjust preset R177 for no visible movement as CH1 invert is switched on and off. Repeat for CH2 to CH4:
   CH2 - R277 Main PCB
   CH3 - R177 Four Channel PCB
   CH4 - R277 Four Channel PCB
6. R111, auto-cal balance. With the test oscilloscope measure the voltage at C156. Select each attenuator range in turn, check the measured voltage lies within the limits +2V to +9V. If the voltage exceeds this range then adjust R111 slightly, clockwise adjustment will increase the voltage of the measured range. Switch the instrument off for a few seconds then re-check the DC balance, number 5 above and auto-cal balance until the desired range is achieved. Repeat for CH2 to CH4:
   CH2 - R211 Main PCB measure at C256
   CH3 - R311 Four Channel PCB measure at C156
   CH4 - R411 Four Channel PCB measure at C256
7. R131, overall channel gain. Select storage mode refreshed and 10mV per division on the channel input. Apply a signal of 6 divisions at 10mV/Div from the oscilloscope calibrator. Using the on-screen cursors adjust R131 to give a peak to peak reading of 60mV. Repeat for CH2 to CH4:
   CH2 - R231 on the Main PCB
   CH3 - R131 on the Four Channel PCB
   CH4 - R231 on the Four Channel PCB

Screen Calibration

These adjusters can be found on the Main PCB with the exception of R740 which can be found on the Four Channel PCB, see Figures 7.2 and R4 and R131 which can be found on the CRT Driver PCB, see figure 7.3.

8. R4, Y calibration. Select non-storage Y-T mode and 10mV per division on CH1. Apply the calibration signal used in 7 above to CH1 input. Adjust preset R4 to give a display of six divisions peak to peak.
9. R740, CH3 & CH4 Y calibration. Transfer the calibration signal to CH3 input and adjust R740 to give a display of six divisions peak to peak.
10. R131, X-Y calibration. Select non-storage X-Y mode with CH1 set to 10mV per division. Select CH2 and switch off CH3 and CH4. Adjust preset R131 to give a horizontal display of six divisions.
11. R844, Y store amplitude. Select storage Y-T mode with CH1 as above. Adjust preset R844 to give a six division peak to peak trace display.
12. R991, X store amplitude. Select the cursors and 1ms per division on the timebase. Move the cursors to obtain a reading of 10ms between them. Adjust preset R991 to give exactly 10 display divisions between the two cursors.
13. R837, Y store offset. Set CH1 input to Gnd. Adjust preset R837 for no vertical movement of the trace as the instrument is repeatedly switched between non-storage and storage modes. If there is a gain discrepancy between non-storage and storage modes see 8 and 11 above.
14. R827, overall Y offset. Select cold start by pressing Menu key eight times and then switch on the cursors. Adjust preset R827 to position the horizontal cursor on the centre line.
15. R646, X offset. Select the Display Menu and adjust preset R646 to centre the display within the graticule lines.
16. R675, X shift (store) offset. Select storage mode, 1ms/Div and centre the trace using the X shift control. Select x10 magnification and adjust preset R165 to centre the trace in the X direction.
17. R997, X shift (store) gain. With x1 magnification selected adjust preset R997 to obtain 10.2 divisions of X shift. This allows the left and right hand edges of the displayed trace to be shifted to the centre graticule line.

Non-Storage Mode Timebase Calibration

These adjusters can be found on the Main PCB with the exception of R133 which can be found on the CRT Driver PCB, see Figures 7.1 and 7.2.

18. R609, 5ms calibration. Select non-storage Y-T mode and 5ms per division. Set the oscilloscope calibrator to give 5ms time markers. Adjust preset R609 to give one marker per division.
19. R608, 0.1ms calibration. Select 0.1ms per division on the timebase and 0.1ms time markers on the calibrator. Adjust preset R608 to give one marker per division.
20. R607, 1μs calibration. Select 1μs per division on the timebase and 1μs time markers on the calibrator. Adjust preset R607 to give one marker per division.
21. R648, X shift (non-store) offset. Select 0.2ms per division on the timebase and 1ms time markers on the calibrator. Adjust preset R648 to give no visible shift in the trace as the instrument is repeatedly switched between storage and non-storage modes.
22. R133, X chop compensation. Select non-storage mode and 10ms per division on the timebase. Adjust preset R133 to give minimum movement on the on-screen alphanumerics.

Attenuator Compensation and Input Capacitance

These adjusters can be found on the Main PCB, see Figure 7.1 Main PCB Adjusters.

23. C107, attenuator compensation. Select non- storage mode, 0.2ms per division on the timebase and 1V per division on the channel attenuators. Apply a 1V x5 division 1kHz squarewave from the oscilloscope calibrator to the Channel 1 input. Adjust trimmer C107 to give square corners on the trace. Repeat for CH2 to CH4:
    CH2 - C207
    CH3 - C307
    CH4 - C407
24. R100, Attenuator accuracy. With the instrument as in 23 above adjust R100 to obtain a display of six divisions exactly. Repeat for CH2 to CH4:
    CH2 - R200
    CH3 - R300
    CH4 - R400
25. C105, input capacitance. Select 0.2V per division on the channel attenuators. Apply a 0.2V x 10 division 1kHz squarewave from the calibrator to the CH1 input via the capacitance standardiser. Check that the over/undershoot on squarewave corner is less than 3mm. Switch calibrator and volts/div to .5V and adjust C105 to match previous shape. Repeat for CH2 to CH4:
    CH2 - C205
    CH3 - C305
    CH4 - C405

Pulse Response

The adjusters C1, C10 and C13 can be found on the CRT Driver PCB, see Figures 7.3. The remaining adjusters can be found on the Main PCB, see Figure 7.1 and some of those for CH3 and CH4 are on the Four Channel PCB, see Figure 7.2.

26. C1, C10 & C13, Y frequency compensation. Set C121 (CH1) to mid position and C10 to minimum. Select 2mV per division on the channel attenuators and 0.2μs per division on the timebase (non-storage

mode). Connect a 1MHz fast rise pulse via the 50Ohm load to CH1 input, adjust the amplitude to give approximately five screen divisions. Adjust trimmers C1 and C13 for a flat top and a square corner on the input trace. Apply the fast rise input to CH2 to CH4 in turn, adjusting the relevant capacitor for a square corner on the trace:

CH2 - C221 Main PCB
CH3 - C121 Four Channel PCB
CH4 - C221 Four Channel PCB

27. C134, frequency compensation. Reconnect the input signal to CH1 and select 20mV per division on the channel attenuators. Adjust trimmer C134 for a square corner on the trace. Repeat for CH2 to CH4:

CH2 - C234 Main PCB
CH3 - C334 Main PCB
CH4 - C434 Main PCB

28. C136, frequency compensation. Reconnect the input signal to CH1 input and select 0.2V per division on the channel attenuators. Adjust trimmer C136 for the best pulse shape. Repeat for CH2 to CH4:

CH2 - C236 Main PCB
CH3 - C336 Main PCB
CH4 - C436 Main PCB

LED Intensity

These adjusters can be found on the Front Panel PCB, see Figure 7.4.

29. R26 & R28, LED intensity. Although these should not need re-setting a slight adjustment can be made if the front panel LEDs are felt to be excessively dim or bright. Note that increasing the LED current to greater than 25mA per device may damage the driver I.C.

5.0 SERVICING

This section takes a systematic approach to servicing a faulty instrument. Starting with a list of symptoms, symptom tables are consulted. These indicate a section of text or a flow chart which will aid in locating the faulty circuit area(s). At the end of this section are the circuit descriptions. These describe the circuits block by block indicating what the circuit does rather than how it does it. It is left to the engineer to interpret them and to make the final diagnosis of the fault within the circuit areas.

5.1 HOW TO USE THIS SECTION

This section covers the detailed information required to service a faulty 1600. It is divided into three parts: symptom tables, fault-finding flowcharts and circuit descriptions.
When approaching an instrument for servicing it is necessary to discover all the symptoms of the fault. In some cases this can be easy; for example if the microprocessor fails then the instrument will be unable to do anything. But many very different faults have fairly similar, if not identical, symptoms.

With the list of symptoms consult the symptom tables. These are rather like the index of a book, the symptoms referring to a flowchart or piece of text in Section 5.3.

The flowchart will lead to the faulty area(s) by giving instructions for a series of measurements to be taken on the boards. These are fairly detailed and no knowledge of the instrument is required to follow them. There are two types of box in these flowcharts: decision boxes and command boxes. Decision boxes have sloping sides and two exits, one marked 'Y' for Yes and the other 'N' for No. The command boxes have straight sides and contain instructions about actions that need to be performed. Within the flowcharts the circuit blocks under scrutiny are indicated by their reference number in the bottom right-hand corner of the command and decision boxes. If no reference is shown then it is the same as shown previously.

Having ascertained the area at fault, or in some cases the component, the final decision as to the required cure is left to the engineer. Considering the high reliability of the components used in the manufacture of the 1600 it may be advisable to discover the cause of the failure.
Section 5.4 provides descriptions of all the circuit blocks. These are of varying sizes depending on the function(s) provided. In-circuit measurements are given, particularly in the analog areas, to aid the engineer.

The 1600 contains many features controlled and calibrated directly by the microprocessor. When a circuit fails within one of these control loops the final results are not predictable. This uncertainty is caused by the software/hardware interaction. The fault-finding flowcharts presented take this into account.

The flowcharts are based mainly on failures of semiconductor devices. These are the most likely faults on new models. However, as the instrument ages interconnections and wiring will fail more frequently. This type of fault may be deduced from the circuit areas that apparently fail.

WARNING *Many of the circuits within the 1600 contain high voltages, in some cases in excess of 8.5kV. Suitable precautions should be taken whilst working on a 'live' instrument. The circuits associated with the tube can retain charges for about a minute after power down.*

5.2 SYMPTOM TABLES

The tables given below cover the most likely symptoms to be expected. They are used in conjunction with Section 5.3 to locate the faulty circuit areas.

How to Use the Tables

Make a list of the fault's symptoms.

2. Check through the index of symptoms, Sections 5.2.1 to 5.2.6, and make a note of the likely faults.
3. Refer to each of the indicated tables for a more detailed description of the fault and its symptoms.
4. If one of the tables matches the fault closely then follow the procedure given in the text. If not, re-check the problem and its symptoms looking for additional clues.

5.2.1 General System Faults

Table No.	Symptom
1	Total system failure
2	Total failure of the trigger system
3	No CRT display
4	Some or all of the front panel LEDs not functioning
5	No response to some or all of the front panel keys
15	Alpha and trace brilliance affected by the same front panel control
16	No alphanumerics and a flat trace in storage mode
17	Machine setups lost on power down

5.2.2 Display Faults

Table No.	Symptom
3	No CRT display
6	No X deflection
7	Trace and Alpha displays at maximum intensity
8	Trace and alpha displays squashed or otherwise distorted
9	No X deflection in non-storage mode
15	Alpha and trace brilliance affected by the same front panel control
16	No alphanumerics and a flat trace in storage mode
18	No X shift
19	Alphanumerics unreadable or incomprehensible

20	No blanking
21	Poor focusing
22	Trace rotate inoperative
23	No dot join
24	Alphanumerics shifted on the screen
25	No X deflection in X-Y mode
32	One or more traces not displayed

5.2.3 Triggering Faults

Table No.	Symptom
2	Total failure of the trigger system
10	Trigger source and coupling not selectable
11	Instrument will not trigger on TVL or TVF couplings
22	Cannot trigger from the EXT source
27	Auto bright-line inoperative
28	Low pass filter not selectable or always selected
29	Poor triggering on CH1 to CH4
30	No control of the trigger level
31	Trigger window inoperative

5.2.4 Acquisition Faults

Table No.	Symptom
12	Trace off the screen top or bottom
33	Add mode permanently selected or not selectable
34	Trace 'stepped'

5.2.5 Y Pre-amplifier Faults

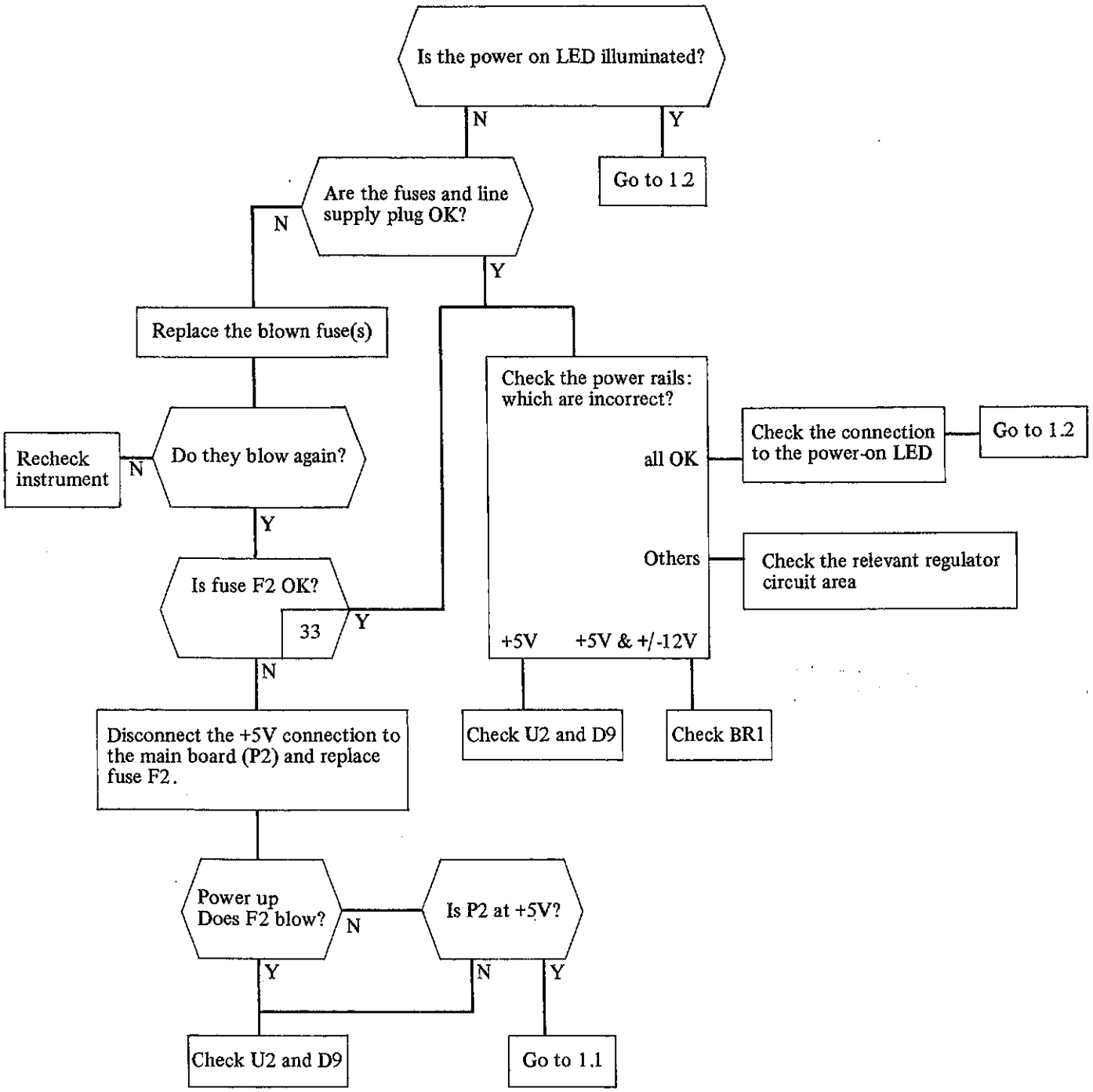
Table No.	Symptom
13	Trace distorted
14	Invert and Variable Gain not Functioning
35	No Y shift
36	DC offset on the trace
37	One or more attenuator range or input coupling selection not available
38	Bandwidth limited to 5MHz in non-storage mode

5.2.6 I/O and Options Faults

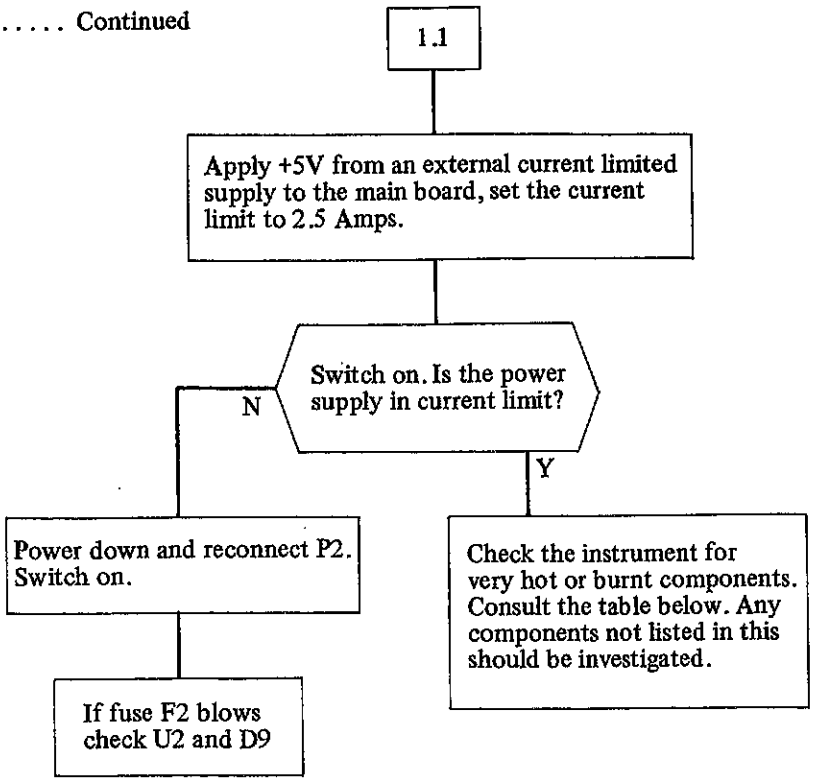
Table No.	Symptom
39	X plot output permanently enabled or inoperative
40	Y plot output(s) missing
41	No calibrator signal
42	Internal plotter option not functioning correctly
43	Backup traces in keypad option lost on power down
44	No response to the keypad
45	No response over RS423
46	No response over GPIB bus

1 Total System Failure

Symptoms: After power up neither the front panel LEDs nor the CRT display come on. The power on LED may or may not be illustrated. See also faults number 3 and 4.



1.1 Total system failure . . . . . Continued



Note: Some components within the 1600 run at high temperatures under normal conditions. Others may be slightly warm. The table below lists all the components which fall into these two categories. Any other components which are running excessively hot will need to be investigated.

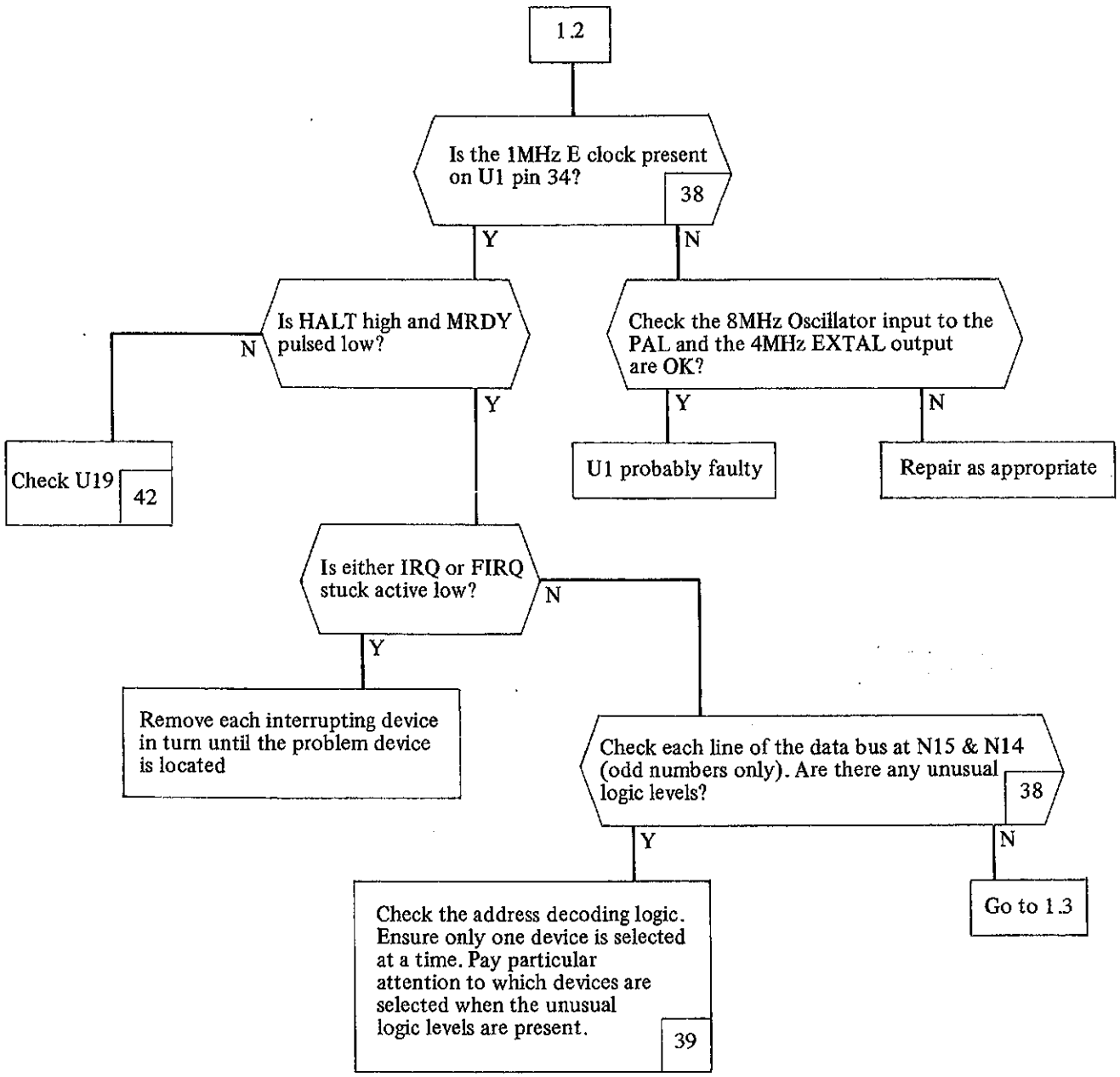
Table 5.3.1 Hot components under normal running conditions

Component ref	Circuit block
R22 & R23	17, Y Output Amplifier
Q3 & Q4	17, Y Output Amplifier
Q19	22, EHT Oscillator
U1 to U4	33, Power Supply
Q2	33, Power Supply
U1	38, Microprocessor
U701	12, Analog to Digital Converter (both Main and Four Channel Boards)
U604	18, Monochip

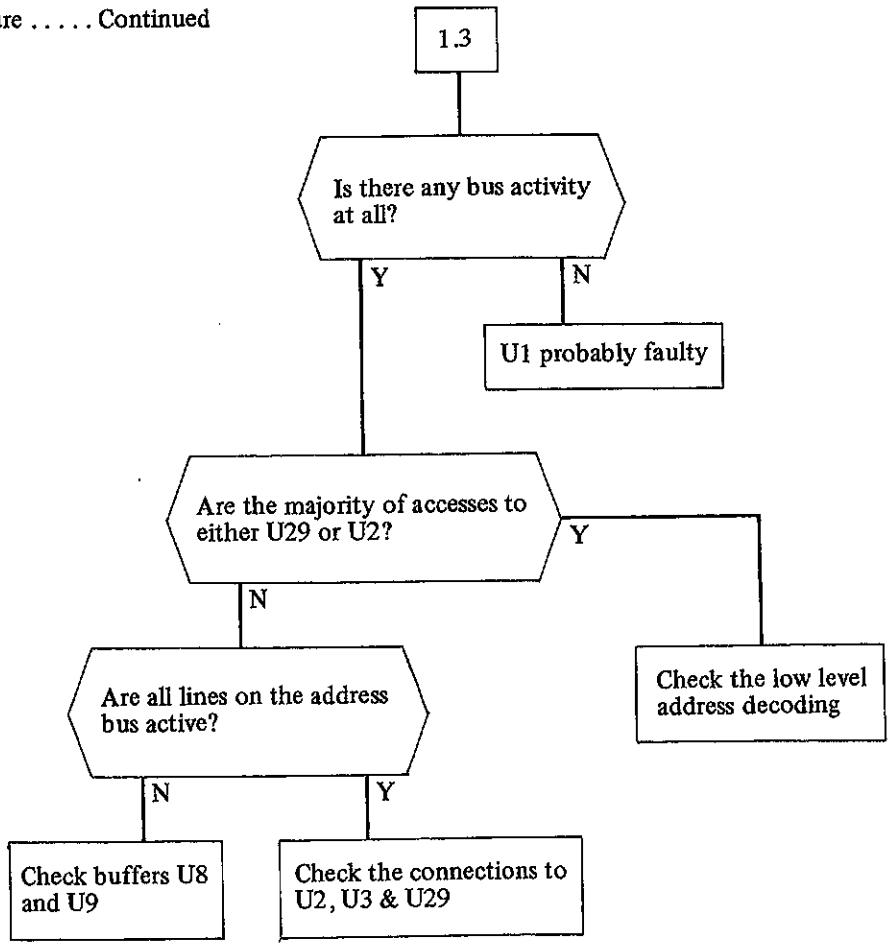
1.2 Total system failure . . . . . Continued

Flow chart 1.2 covers general problems associated with the microprocessor. If a 6809 bus analyser or development system is available then this would provide a quicker and more reliable means of finding the fault.

The flow chart below gives some guidelines on how to find the fault without specialised equipment.

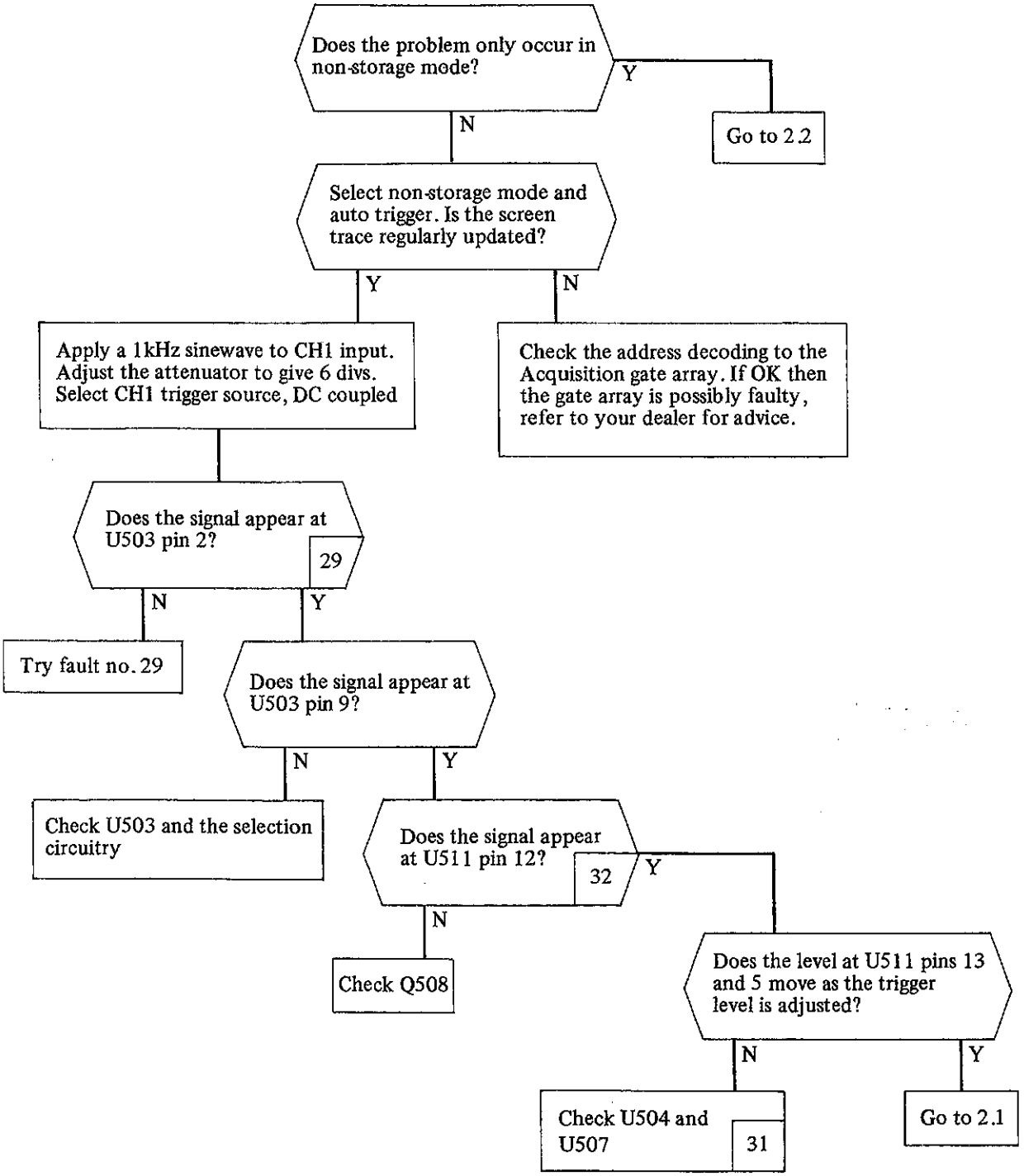


1.3 Total system failure . . . . . Continued

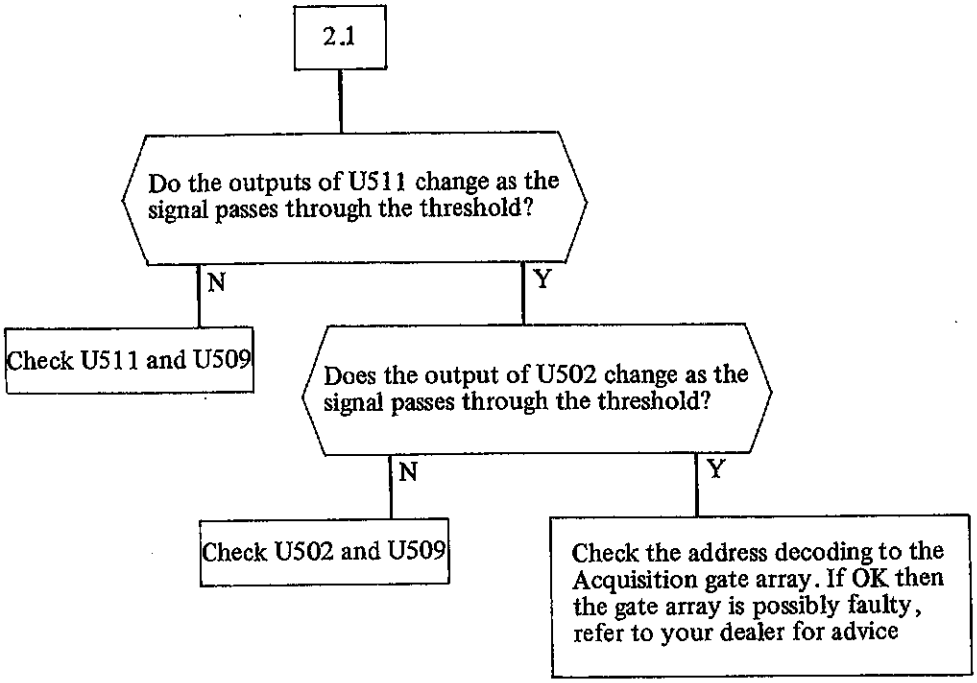


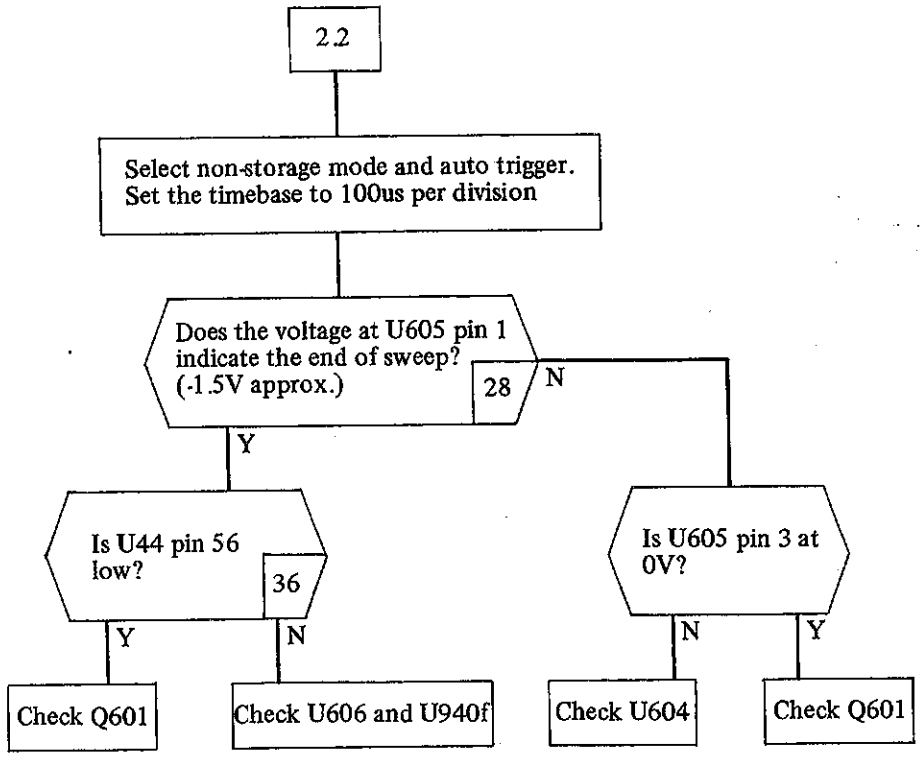
2 Total Failure of the Trigger System

Symptoms: The instrument cannot trigger on any externally applied signal irrespective of the choice of source, coupling, slope and trigger level.



2.1 and 2.2 Total Failure of the Trigger System . . . . . Continued

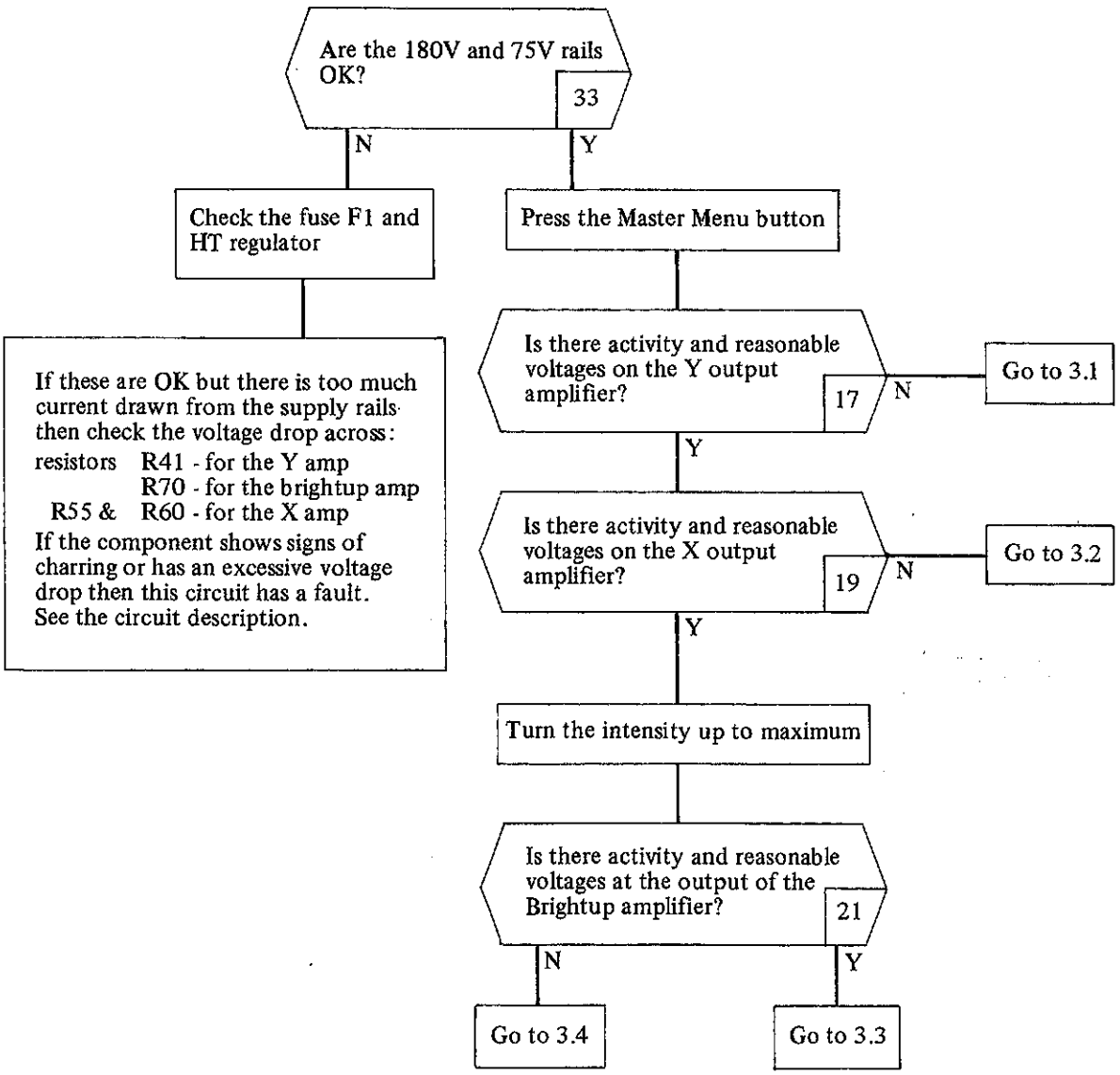




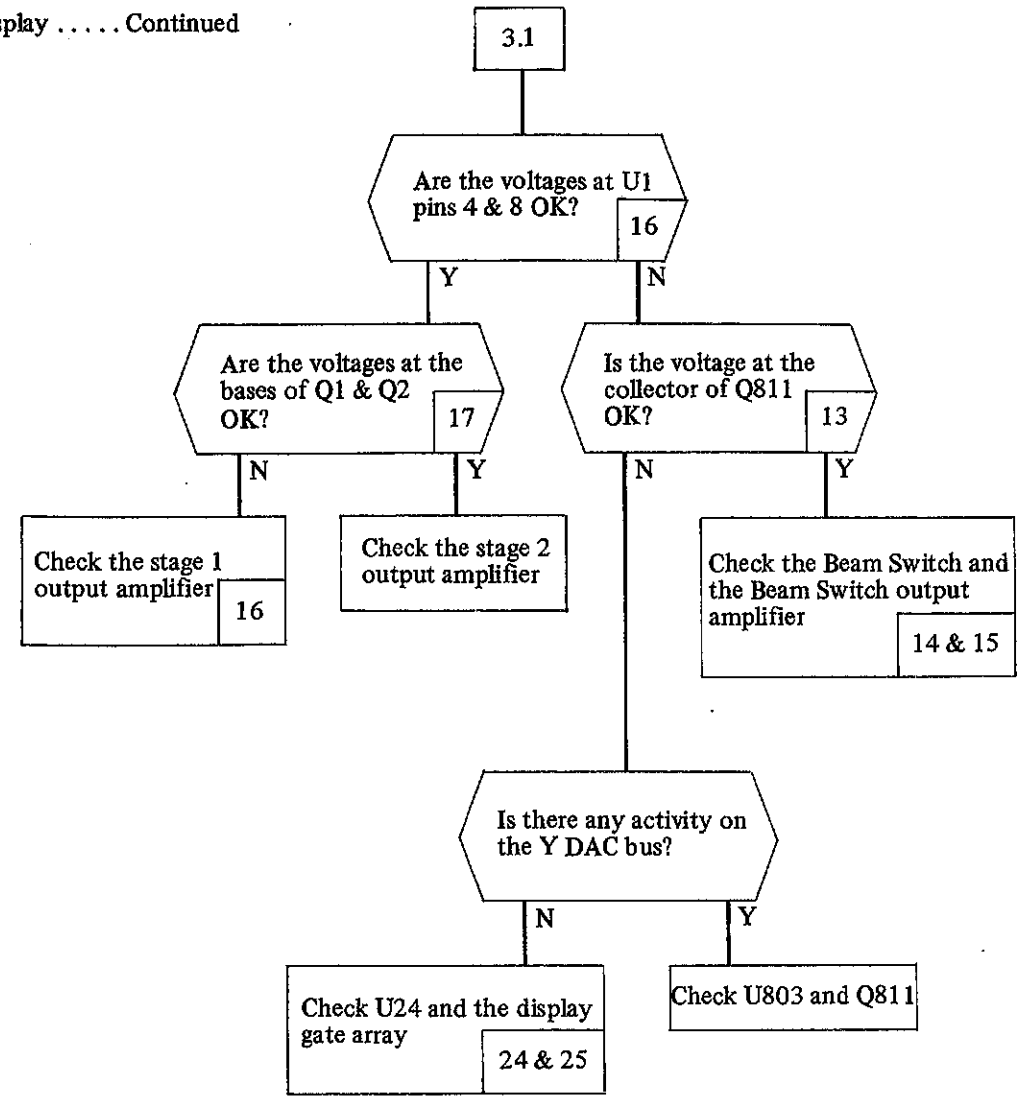
3 No CRT Display

Symptoms: There are no traces or alphanumerics displayed on the CRT screen. The front panel LEDs illuminate as usual.

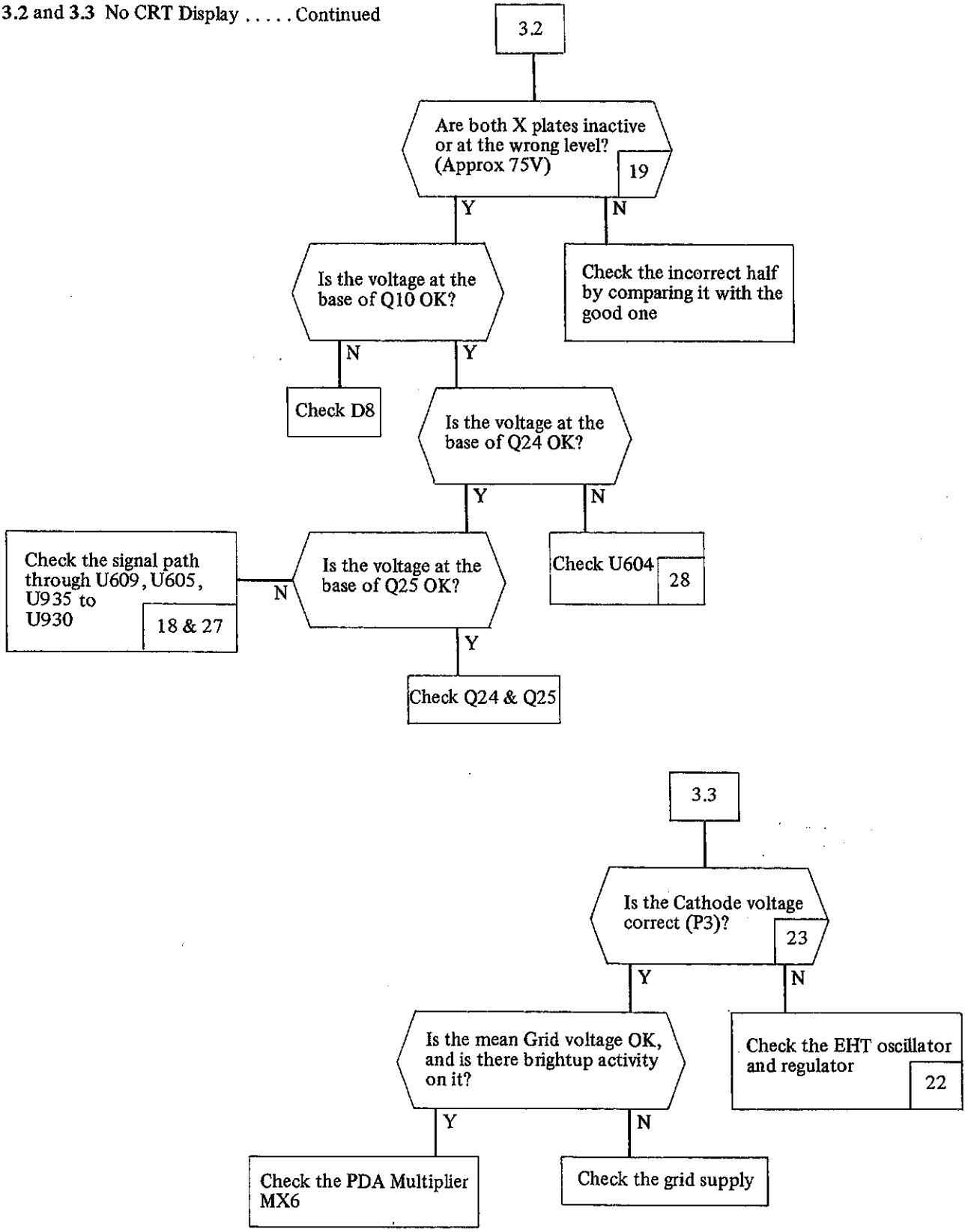
WARNING: Measurements may be required on the tube driver PCB. This contains voltages in excess of 8.5kV. Due care should be taken when working in this area.



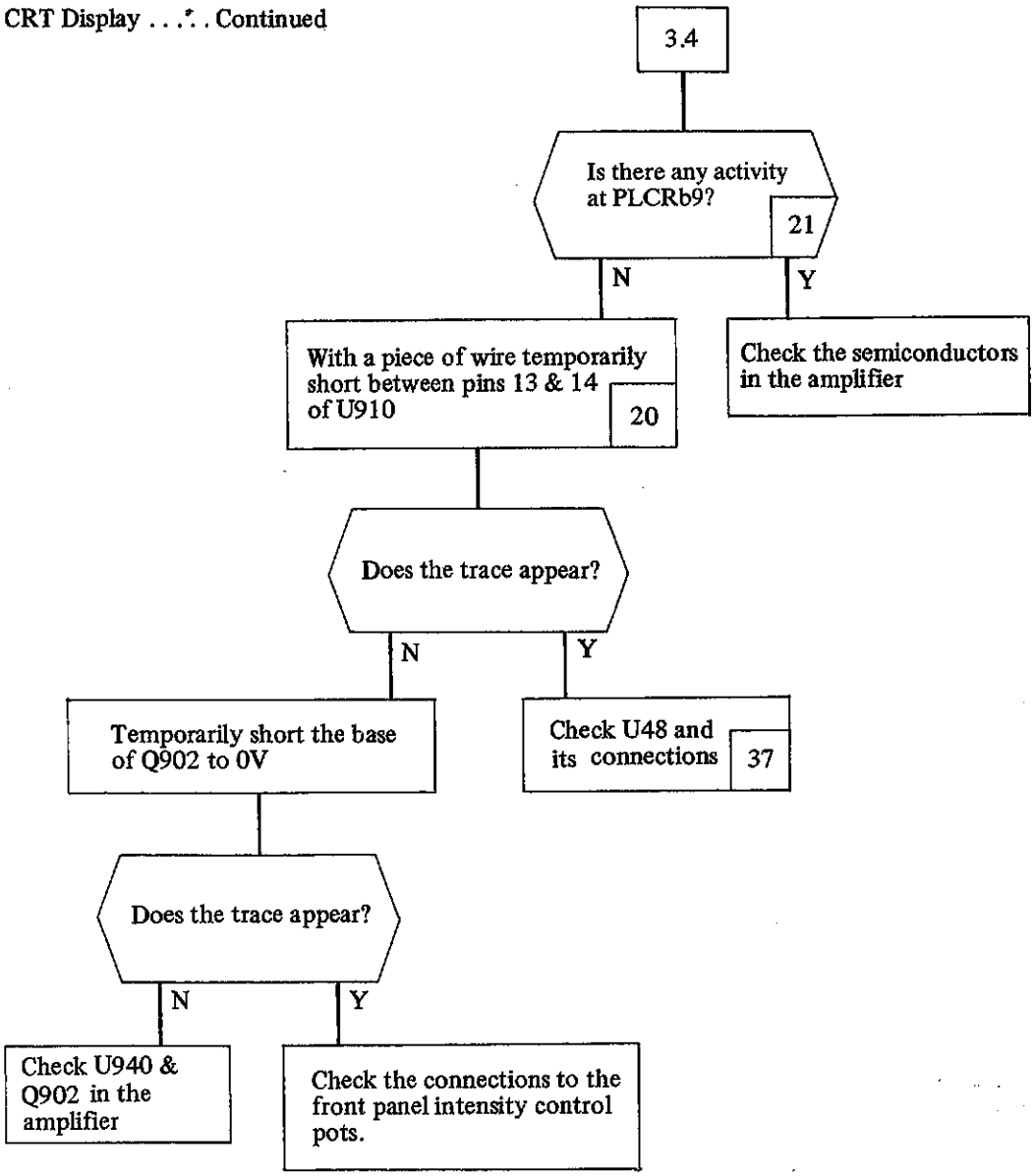
3.1 No CRT Display . . . . . Continued



3.2 and 3.3 No CRT Display . . . . . Continued

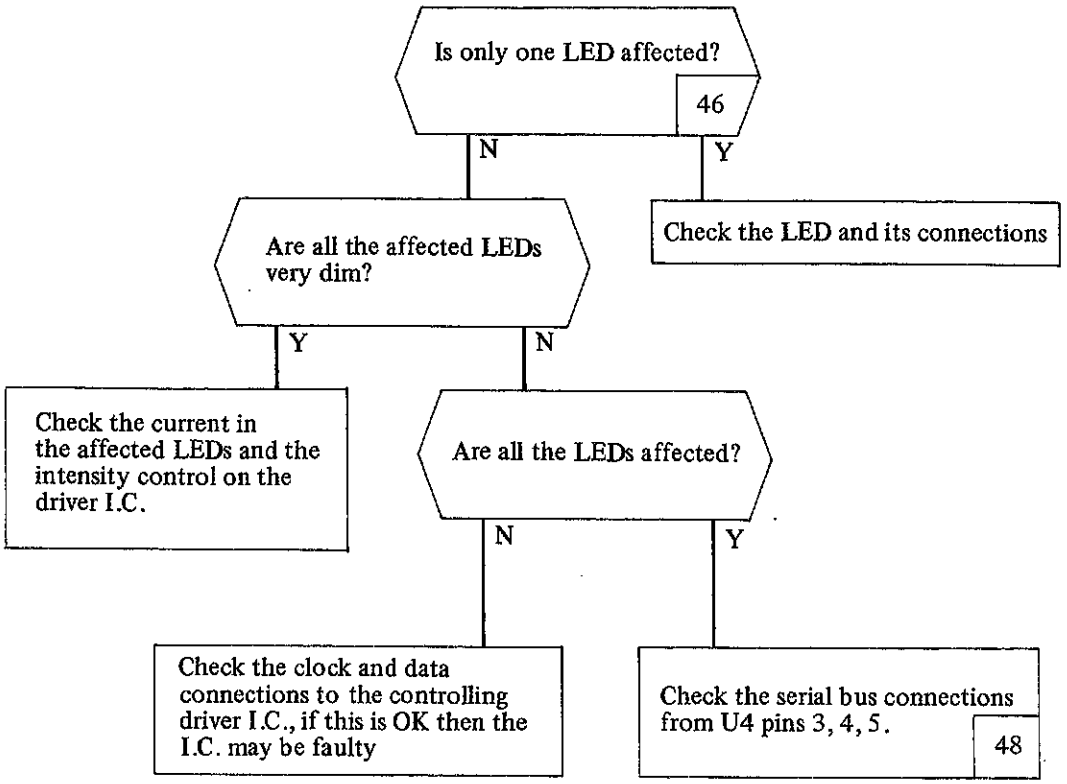


3.4 No CRT Display . . . . . Continued



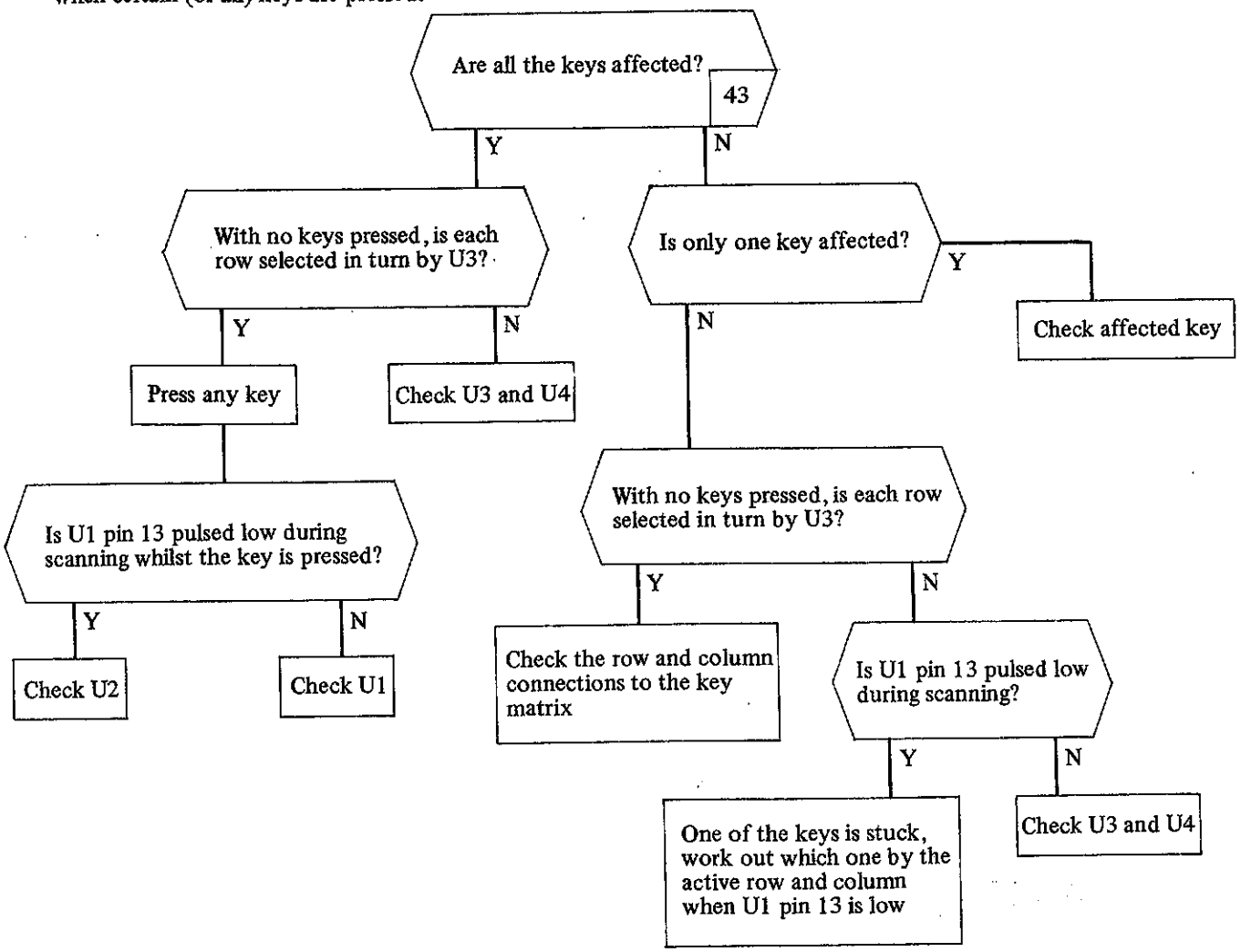
4. Some or All of the Front Panel LEDs not Functioning

Symptoms: Some of the front panel LEDs will indicate the wrong status, i.e. they will be off when they should be on, or vice versa.



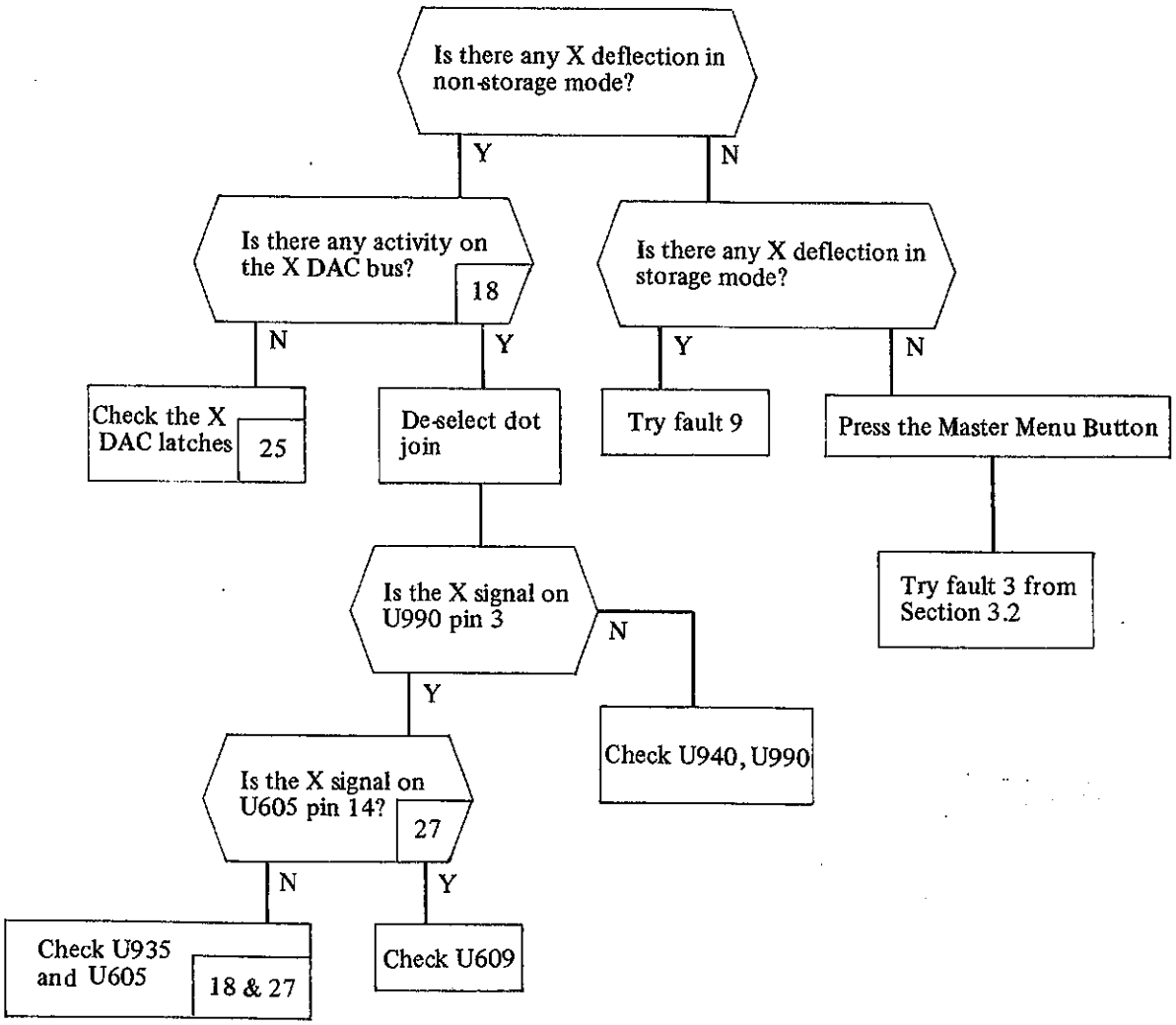
5 No Response to Some of All of the Front Panel Keys

Symptoms: The instrument does not respond when certain (or all) keys are pressed.



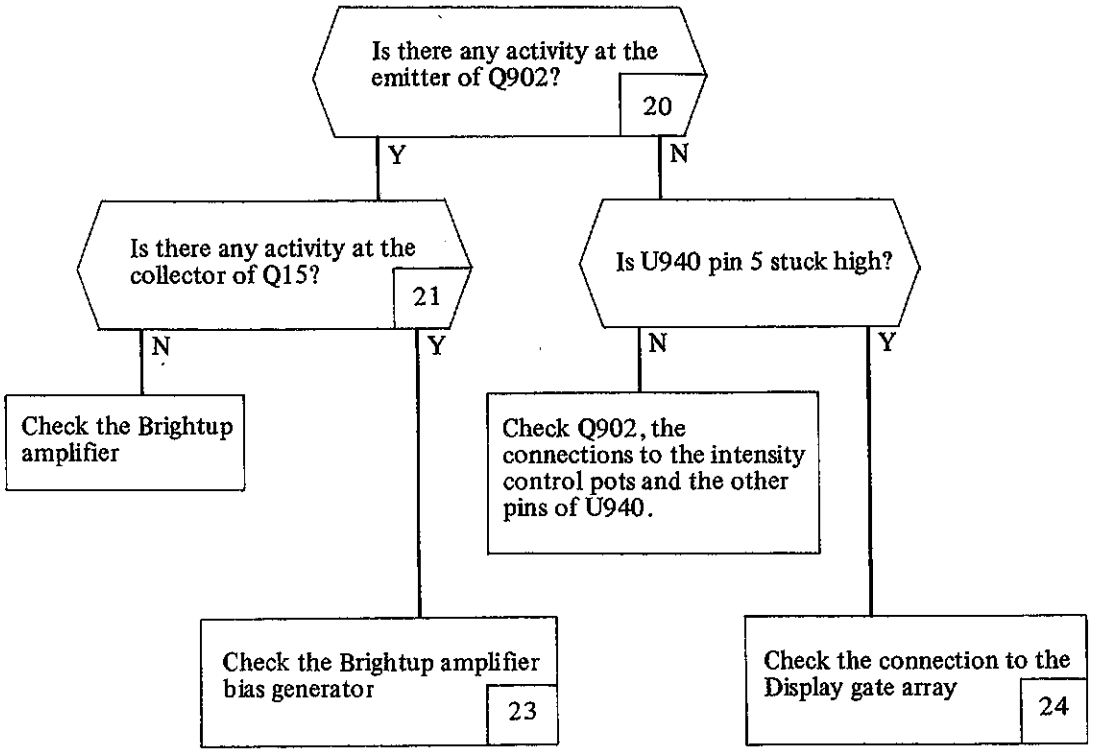
6 No X Deflection

Symptoms: The trace displays appear as a vertical bar, the height of which is dependent on the captured or displayed trace. These may be positioned anywhere on the screen. Alphanumerics appear as a series of short vertical bars with small gaps.



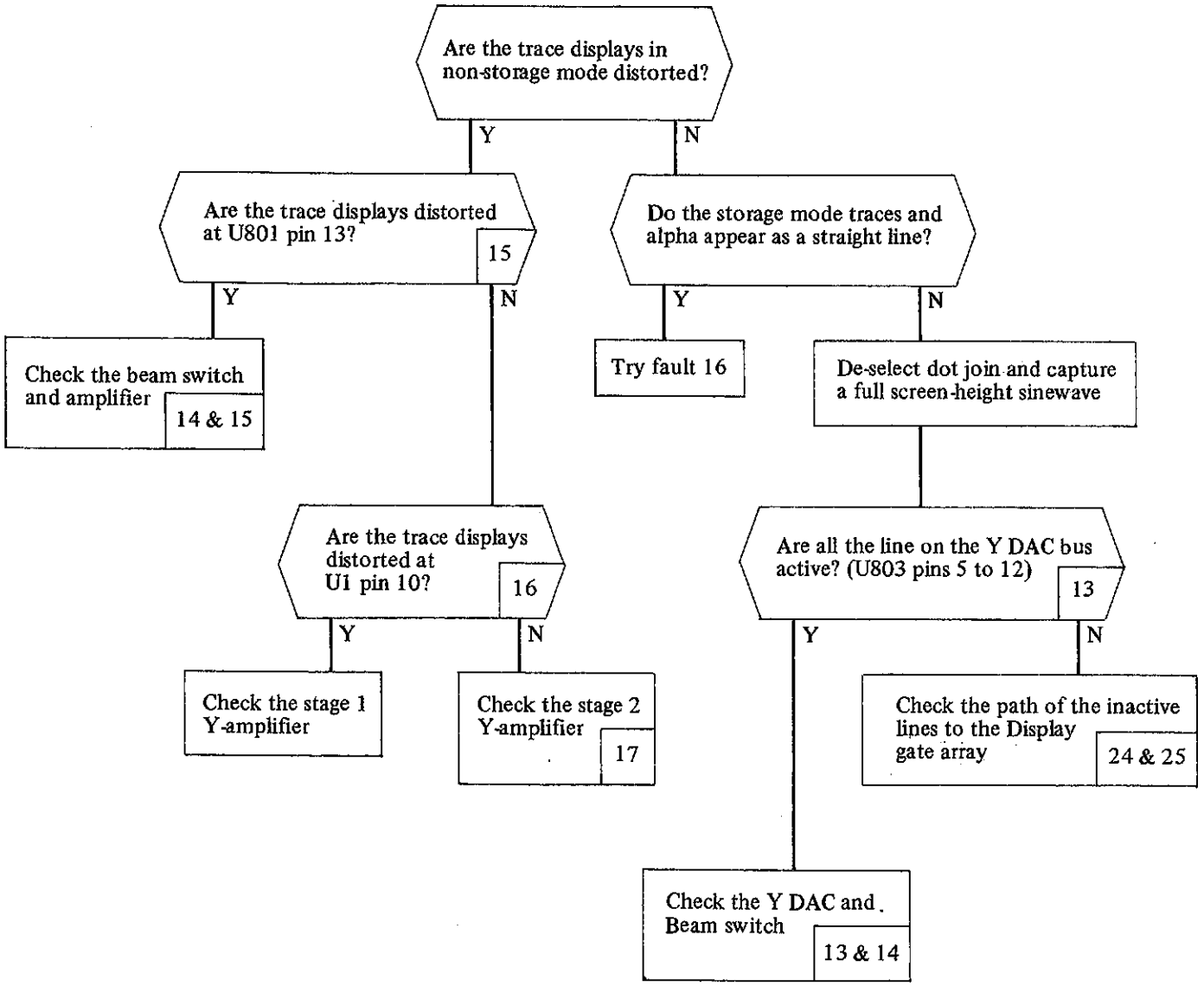
7 Trace and Alpha Displays at Maximum Intensity

Symptoms: Both the trace and alphanumeric displays are stuck at maximum intensity. Neither of the front panel control pots can be used to affect the brilliance. There will be no blanking.



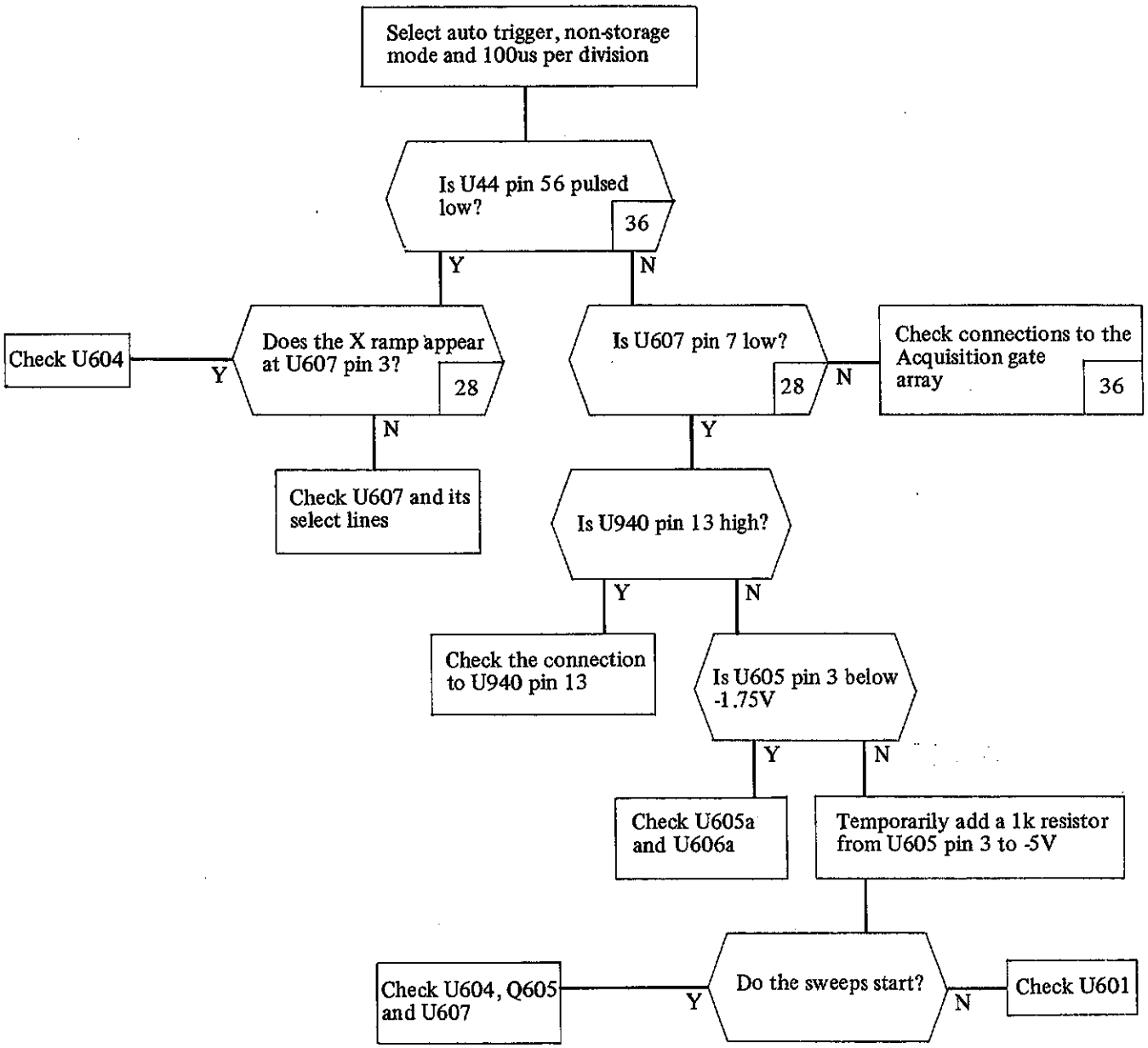
8 Trace and Alpha Displays Squashed or Otherwise Distorted

Symptoms: In storage mode both the trace and alpha displays are distorted. However, in non-storage mode the trace display may not be distorted.



9 No X Deflection in Non-Storage Mode

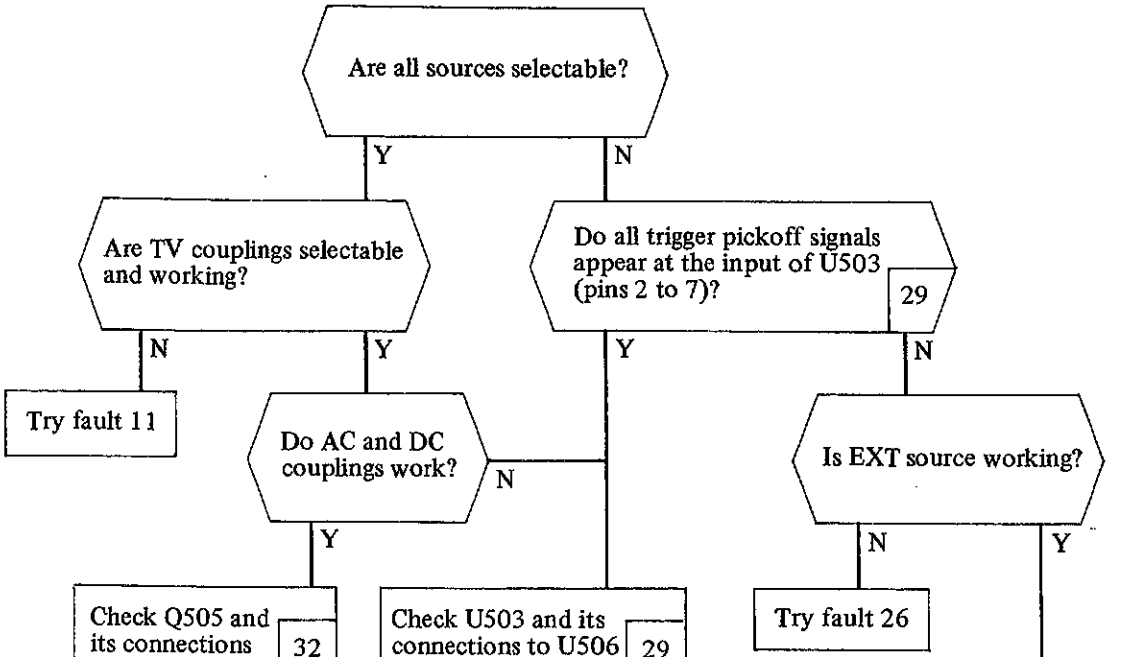
Symptoms: Alphanumerics and storage mode traces appear as normal. In non-storage mode the alpha appears but there are no traces.



10 Trigger Source and Coupling not Selectable

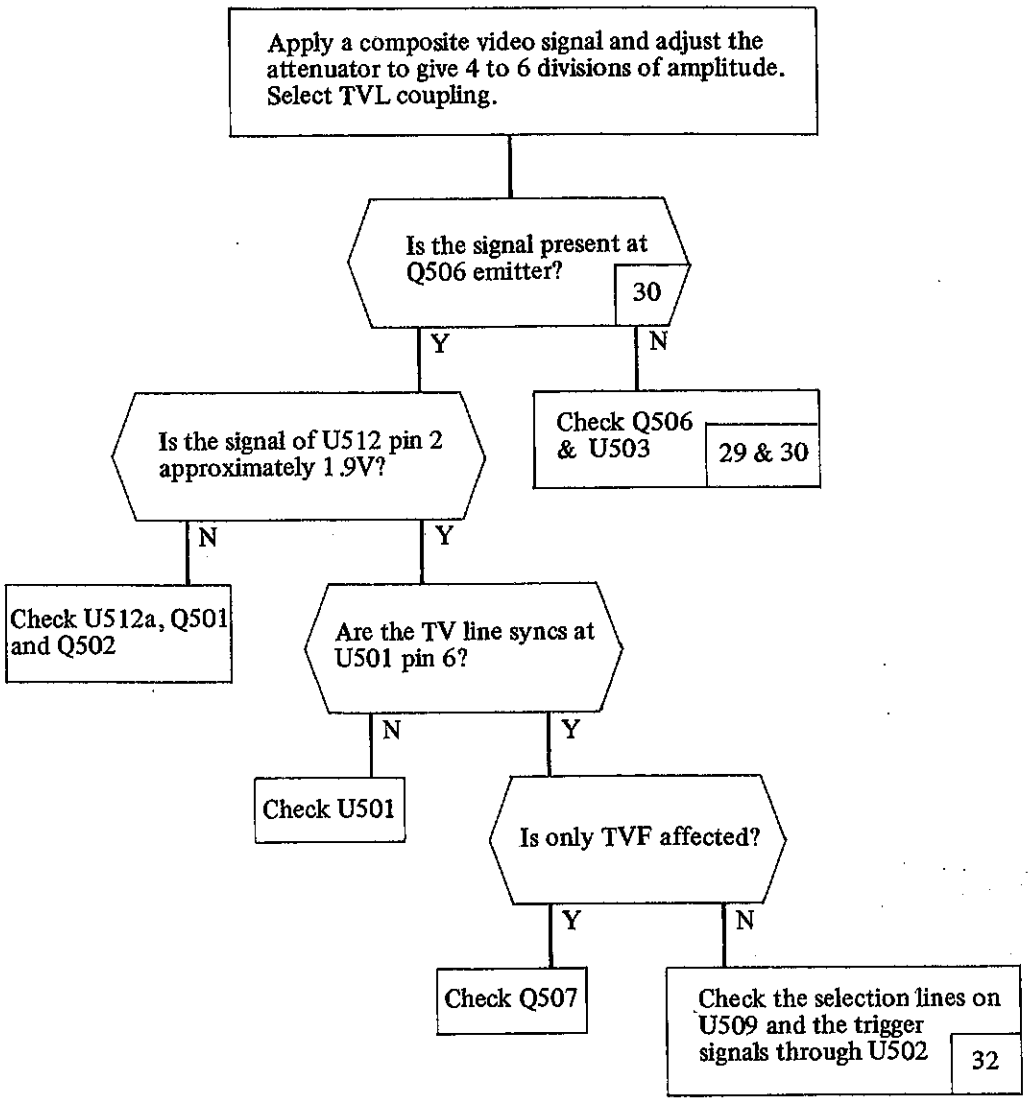
Symptoms: It is not possible to select certain trigger sources or couplings.

Note: It may be possible that the front panel select switch is not working, see also fault 5.



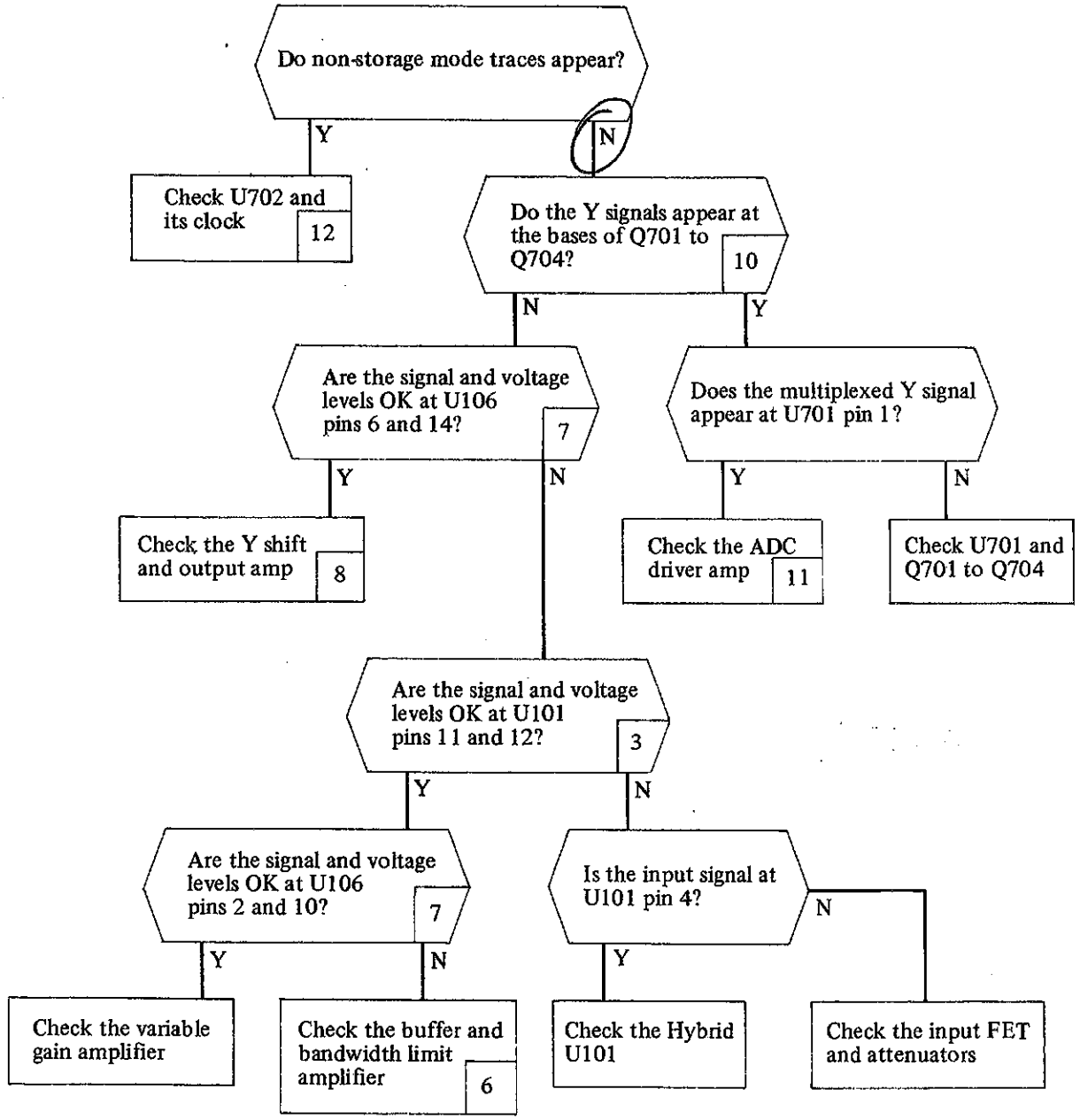
11 Instrument will not Trigger on TVL or TVF Couplings

Symptoms: When a composite video signal is applied to an input and TVl or TVF coupling is selected it is not possible to obtain a stable trigger.



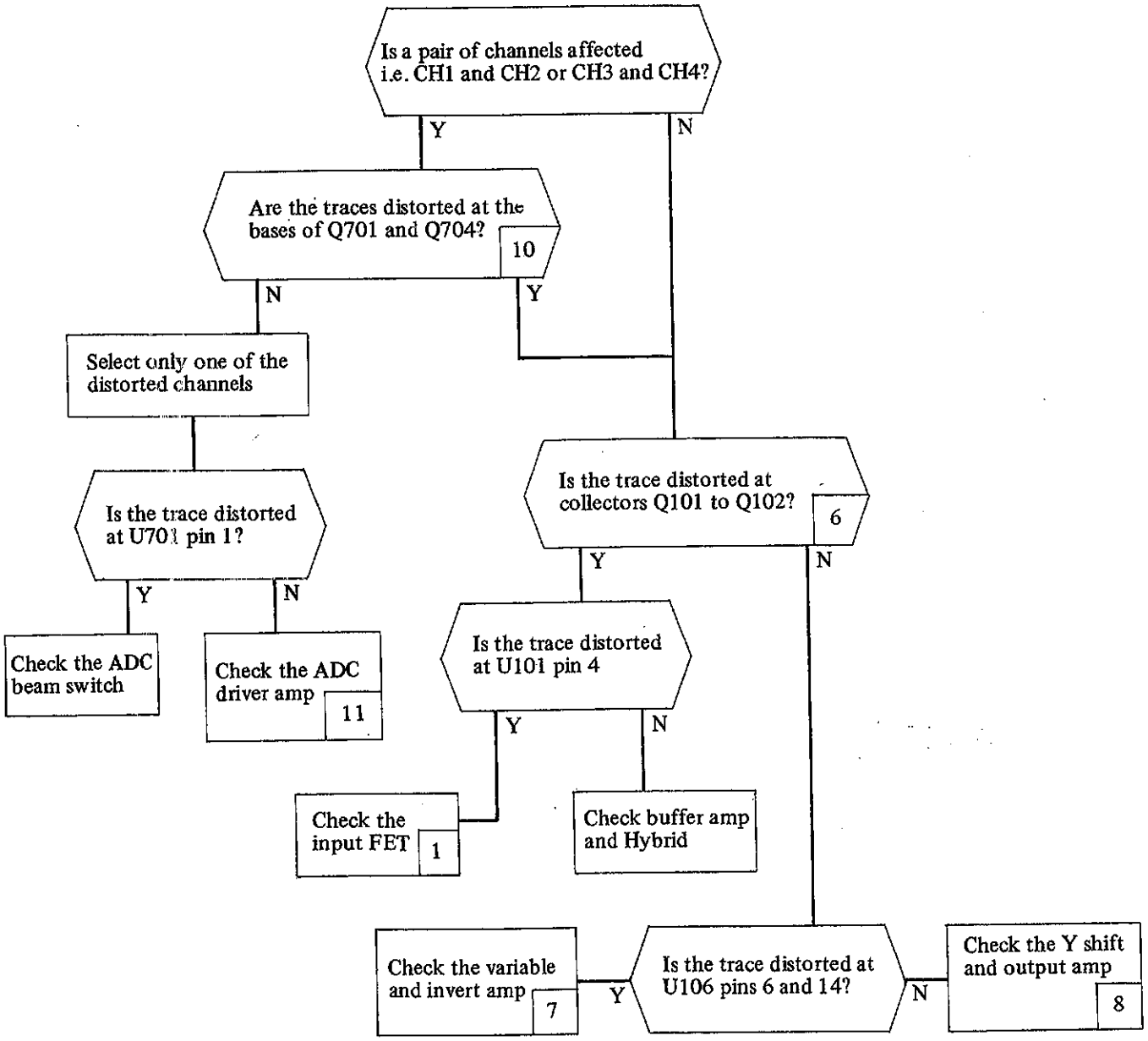
12 Trace off the Screen Top or Bottom

Symptoms: Alphanumerics appear as normal but captured traces and possibly non-storage mode traces do not appear. In storage mode acquisitions will go to completion as normal.



13 Trace Distorted

Symptoms: One or more of the display traces is distorted on both storage and non-storage modes. Alphanumerics is not affected, see fault 8 otherwise.



14 Invert and Variable Gain not Functioning

Symptoms: Variable gain may not be working or may have only a limited range. Independently of this, invert may be permanently selected or not selectable.

Note: The operation of the four Variable gain and invert amplifiers is identical, hence reference is made to Channel one only.

This circuit is described in circuit block 7, Variable Gain and Invert Amplifier. There are two controls; a digital signal to switch invert on or off and a voltage to control the amount of variable gain. Check both are present and functioning. If invert is missing check the serial bus, and if the control voltage is missing then check the connection to the front panel control pot. If both are OK then check the voltages on U107 and U106.

15 Alpha and Trace Brilliance Affected by the Same Front Panel Control

Symptoms: The intensity of both the alphanumerics and the trace displays are affected by the same front panel control. It is possible that both controls may affect both displays; in this case there will also be no blanking: see fault 20.

This circuit is described in circuit block 20, the Brightup Combining Amplifier. The intensity control is selected by the output of U50d. When this fault is present the output of this gate is fixed. One or other of the gate inputs will be stuck low. Trace signal 'Select Alpha' back to the Acquisition gate array (circuit block 36), and 'DACREF' to the miscellaneous control latch (circuit block 40).

16 No Alphanumerics and a Flat Trace in Storage Mode

Symptoms: Normal non-storage mode traces appear, but without alphanumerics. In storage mode the trace(s) will appear flat and in some cases they may be off the screen.

This circuit is described in circuit block 13, Y Output DAC. Check first that there is activity on the Y DAC bus, pins 5 to 12 of U803. If this is inactive then trace it back to U24 (circuit block 25) and then to the Display gate array (circuit block 24). If there is reasonable activity on the Y DAC bus, de-select linear dot joining and check for the display signal on Q811 collector. If this is present check the beam switch (circuit block 14).

17 Machine Setups Lost on Power Down

Symptoms: Machine setups cannot be recalled once the instrument has been switched off.

This circuit is described in circuit block 42, Battery Backup Control. The machine setups are saved in a battery backed up RAM, U3. When the instrument is switched off power is supplied to this I.C. by battery B1. When this fault occurs the battery needs replacing.

18 No X Shift

Symptoms: The real time and storage mode traces cannot be shifted in the X direction, i.e. left and right. However, they may have a permanent offset to one side.

This circuit is described in circuit block 26, X shift DAC and Control. Continually adjust the X shift control and check for activity on the X shift bus, pins 5 to 12 of U603. If there is no activity check the serial bus and U601. If the bus is active check for the X displacement signal on U603 pin 4. If this is at a fixed DC level the DAC (U603) may be faulty, otherwise check the Op-amps, U605.

19 Alphanumerics Unreadable or Incomprehensible

Symptoms: The on screen alphanumerics contains unrecognisable symbols or has characters in the wrong positions.

Note: Check the storage mode trace is OK, otherwise try fault 8.

This circuit is described in circuit block 24, Display Gate Array and RAM. Check the address and data bus connections to U22.

20 No Blanking

Symptoms: Extra dots will appear on the screen. They can most easily be seen on the menu screens. The intensity control pots may work as normal or possibly they may both affect both alpha and trace displays. If the displays are stuck at maximum intensity see fault 7.

Check the output of the brightup combining amplifier (circuit block 20), if the blank level does not occur here check the amplifier and its connection back to the Data Control gate array (circuit block 37). If both control pots are affecting the intensity the bandwidth of the brightup amps has become too low. Follow the signal path from the combining amp through the Brightup amp (circuit block 21) to the grid (circuit block 23), at some stage the essential high frequency components will be removed from the signal.

21 Poor Focusing

Symptoms: It is not possible to obtain an adequately focused display with the front panel control.

This circuit is described in circuit block 23, EHT Output Multipliers. Check the adjustment of the preset focus control, see Section 4 Nos. 3 & 4. If reasonable focus can not be obtained check the semiconductors in the remote focus amplifier and the connection to the front panel control pot.

22 Trace Rotate Inoperative

Symptoms: It is not possible to bring the trace to horizontal by adjusting the front panel preset.

This circuit is shown on the miscellaneous circuits diagram. Check the emitter of Q903 and Q904 can be adjusted between +11V and −11V by the preset control. If this is working then check the connection to the trace rotate coil.

23 No Dot Join

Symptoms: The linear dot joiner does not work in X, Y or in both X and Y.

If both X and Y are not functioning then check the control signal at U30 pin 15 (circuit block 38). If X is not working then check U990 (circuit block 18), and if Y then check Q811 and Q812 (circuit block 13).

24 Alphanumerics Shifted on the Screen

Symptoms: The alphanumerics are no longer centralised on the CRT display. This is most easily seen on the menu screens, where the text lines up with the buttons to the side of the screen.

The position of the alphanumerics is set up during calibration, see Section 4. If the error persists after re-calibration then:

X Offset, follow the X signal from U935 pin 7 (circuit block 18) to the X output amplifier (circuit block 19) to the X plates.

Y Offset, follow the Y signal from Q811 collector (circuit block 13) through the beam switch amplifier (circuit block 14) to the output amps (circuit blocks 15 and 16).

Compare the measured voltages with those given in the circuit descriptions to locate the faulty area(s).

25 No Deflection in X-Y mode

Symptoms: The X-Y traces appear as a vertical bar, the height of which is dependent on the applied Y signal. Both non-storage and storage mode problems are covered here.

Storage Mode: This circuit is described in circuit block 25, Display DAC Latches. Check U23 is selected instead of the U25 and U27 combination.

Non-Storage Mode: Check the X signal is selected at U607 pin 1 (U607 pins 9 and 10 should be high) and that the End Of Sweep (EOS) is disabled by U940 pin 12 being low.

26 Cannot Trigger from the EXT Source

Symptoms: The instrument can trigger from the channel and line inputs, but when EXT is selected it is no longer possible to obtain a stable trigger.

This circuit is described in circuit block 29, Trigger Source and Coupling Selector. Check the signal path from the front panel through the main board cable to U503 pin 6. If the signal is present here check the control signal at U503 pin 14.

27 Auto Brightline Inoperative

Symptoms: There will be mistriggering on signals with moderate trigger repetition rates, i.e. greater the 30ms but slower than the selected timebase speed.

This circuit is described in circuit block 32, Trigger Level Comparator. Check the A and B control lines to U501b. While triggers are being received the output on pin 10 should remain high.

28 Low Pass Filter Not Selectable or Always Selected

Symptoms: It is either not possible to trigger on high frequency signals (L.P.F. always selected) or it is not possible to reject the high frequency components on the input signal to trigger on the low frequency ones (L.P.F not selectable).

This circuit is described in circuit block 32, Trigger Level Comparator. Check Q505 and its control line.

29 Poor Triggering on CH1 to CH4

Symptoms: It is difficult, or not possible, to trigger on signals applied to one of the four input channels.

This circuit is described in circuit block 8, Y Shift and Output Amplifier. Check the channel signal appears on Q105 emitter and at U110 pin 2. If the signal appears at these points or if more than one channel is affected then check U503 and its select lines (circuit block 29).

30 No Control of the Trigger Level

Symptoms: Although the instrument can be triggered on applied signals it may not be possible to adjust the trigger point with the trigger level control.

This circuit is described in circuit blocks 31 and 32, Trigger Level DACs and Comparator. Check that the on-screen trigger bar moves up and down as the trigger level is adjusted. If not, check the front panel switch and see fault 5. If this is working check the digital inputs to the DAC, pins 5 to 12 of U504, are active and that the voltage at pin 1 of U510a changes in response to the adjustment. If these are also OK, check the Op-amps U510c and U510d.

31 Trigger Window Inoperative

Symptoms: The trigger window appears to be not selectable or at a fixed size.

This circuit is described in circuit blocks 31 and 32, Trigger Level DACs and Comparator. Check there is activity on the digital inputs of U505, pins 5 to 12, as the trigger window is adjusted. If not check the front panel switch (see fault 5) and U508. If this is OK check the outputs at U510 pins 14 and 7 move in antiphase as the size of the window is adjusted.

32 One or More Traces Not Displayed

Symptoms: One or more of the traces cannot be displayed. The front panel LED indicators may or may not show the actual state of the instrument.

Note: The affected trace(s) may be off the screen, see also fault 12.

This circuit is described in circuit block 10, ADC Beam Switch. Check that the front panel indicator Off/Norm/Inv changes in response to repeated presses of the associated button. If not check the front panel switch, see fault 5. If a pair of channels is missing check the Y output beam switch, circuit block 14. If only one channel is missing from either pair then check the ADC beam switch and its control lines (circuit block 10).

33 Add Mode Permanently Selected or not Selectable

Symptoms: If Add mode is permanently selected both CH1 and CH2 shift controls will affect the CH1 display, similarly for CH3 and CH4. The front panel indicator may not show the actual state of the instrument.

This circuit is described in circuit block 10, ADC Beam Switch. If the front panel indicator cannot be changed by repeated presses of the Add button then check the switch, see fault 5. If this is functioning check U703 and its connections to U44.

34 Trace 'Stepped'

Symptoms: This problem occurs in storage mode only. A smooth continuous trace such as a sinewave appears to be mixed up and has large gaps in it. Alternatively the trace seems to be made large, clearly visible steps.

Note: In storage mode the trace is made up from 256 discrete Y levels, on close examination of the screen the levels can be seen. This is normal for a digital storage oscilloscope and should not be confused with the problem described above.

This circuit is described in circuit block 37, Data Control and Acquisition RAMs. Apply a full screen height sinewave to one of the affected channels. Check all the lines are active on the following buses:

1. ADC to Data Control gate array
   AD0-AD7 on U48
2. Data Control gate array to Acquisition RAMs
   AAD0-AAD7, BAD0-BAD7 and CAGD0-CAD7 on U48
3. Data Control gate array to Display gate array
   LD0-LD7 on U48

If this problem occurs on CH3 and CH4 then check the Data Control gate array on the Four Channel PCB.

35 No Y Shift

Symptoms: One or more of the traces cannot be shifted by the front panel Y shift controls.

This circuit is described in circuit block 8, Y Shift and Output Amplfier. If more than one channel is affected check the serial bus to U108, U208 etc. If only one channel is affected check activity on the shift DAC bus, U109 pins 5 to 12, as the front panel control is adjusted. If there is no activity check the front panel switch (see fault 5) and check U108. If the bus is active check the DAC, U109.

36 DC Offset on the Trace

Symptoms: The Y shift adjustment needs to be near one end of its range to bring the trace on the screen. The input should be coupled to ground while this is verified.

Select storage mode and check the affected pre-amp circuit, starting from the input BNC and ending at the ADC input. The input should be shorted to ground during these tests. When a circuit with incorrect DC voltages is located a fault has been located.

37 One or more Attenuator Range or Input Coupling Selections Not Available

Symptoms: One or more of the attenuator ranges cannot be selected. It is possible to obtain abnormal ranges and possibly the input may be permanently AC, DC or Ground coupled.

If the attenuator readout on the CRT screen does not change as the front panel control is adjusted see fault 5.

The input attenuator is control by three circuits. Check first that the correct control signals are present for the selected range, see circuit block 2 and the table at the end of circuit block 3 description. Check all the relays are activating properly and the control signals are reaching U101. If both of these are OK U101 is possibly faulty.

38 Bandwidth Limited to 5MHz in Non-Storage Mode

Symptoms: The real time bandwidth is limited to 5MHz (should be 20MHz) even after re-calibration.

Note: The bandwidth of the instrument can be severely reduced by incorrect calibration, although this should never drop as low as 5MHz.

This circuit is described in circuit block 6, Buffer Amplifier and Bandwidth Limit. Check Q103 and Q104 and their control signals. The bases should be at 0V in non-storage mode.

39 X Plot Output Permanently Enabled or Inoperative

Symptoms: The X plot output is either permanently active (should be at 0V when not plotting) or is stuck at a DC level while plotting.

This circuit is described in circuit blocks 18 and 34, X DAC and X Plot Output Latches. If plot output is permanently active check U942 and the control line on pin 11. If the plot is inoperative but the trace sweeps the screen during plotting check U942 and the control line on pin 11, otherwise check the plot output latches are enabled.

40 Y Plot Output(s) Missing

Symptoms: One or more of the Y plot outputs is stuck at a DC level during plotting.

This circuit is described in circuit block 35, Plot DACs. If all four outputs are inactive check the microprocessor interface and address decoding. If a pair are inactive, i.e. CH1 and CH2 or CH3 and CH4, check the associated DAC and Op-amps. Otherwise check the connections to the rear panel connector and the Op-amps of the affected channel.

41 No Calibrator Signal

Symptoms: The front panel time/voltage calibrator signal is not present.

This circuit is described in circuit block 45, Calibrator. Check for oscillations at U60 pin 3, if these are missing check U60 otherwise check Q60 and the connections to the front panel.

42 Internal Plotter Option not Functioning Correctly

Symptoms: The internal plotter does not function at all or cannot produce a correct drawing (see Operators Manual).

This circuit is described in circuit block 51, Internal Plotter Option. If there is no response from the plotter during plotting but it responds to the paper feed button check U3 and U18 (circuit block 41) and its address decoding. If there is no response from the paper feed button check U1 and the reset line on pin 2. If partial plots are produced check the buffers, U2 and Q3 to Q8.

43 Backup Traces in Keypad Option Lost on Power Down

Symptoms: The backed-up traces from the save trace facility are lost when the instrument is switched off. The date and time may also be corrupted.

This circuit is described in circuit block 49, 160 Processor Interface. Check battery B1 and replace as necessary.

44 No Response to the Keypad

Symptoms: The instrument does not respond to any of the keypad buttons.

This circuit is described in circuit block 50, Keypad Option. Check the connections to the Keypad, if these are OK check U1 and U2 are operating. If U1 is transmitting data from pin 8 then check U18, circuit block 41.

45 No Response Over RS423

Symptoms: Data and commands cannot be sent or received with the RS423 interface option.

This circuit is described in circuit block 47, RS423 Option. Check all the connections from the instrument to the option pod. If these are OK try transmitting a trace, or send several commands, to the instrument, check the chip select line on U1 pin 39 is active. If not check U4, U6 and U8 otherwise check U1 and the RS423 buffers U2 and U3.

46 No Response Over GPIB Bus

Symptoms: Data and commands cannot be sent or received with the GPIB interface option.

This circuit is described in circuit block 48, GPIB (IEEE488) Option. Check all the connections from the instrument to the option pod. If these are OK try transmitting a trace, or sending several commands, to the instrument. Check the chip select line on U1 pin 3 is active. If not check U4, U6 and U7 otherwise check U1 and the bus buffers U2 and U3.

5.4 CIRCUIT DESCRIPTION

The following sections of text descibe what the circuit blocks of the 1604 do. Each block is preceded by a number, this is used in Section 5.3 to cross-reference the circuits under discussion in the flow charts with those described here. To find the components on the circuit board see figures 6.1 and 6.24 - 6.29.

Index of Circuit Blocks

1 Input Attenuator

This circuit consists of

for Channel 1: RL101 to RL104, N104, Q111 and associated discrete components

for Channel 2: RL201 to RL204, N204, Q211 and associated discrete components

for Channel 3: (1602 CH2) RL301 to RL304, N304, Q311 and associated discrete components

for Channel 4: RL401 to RL404, N404, Q411 and associated discrete components

CH2 on the 1602 is handled by the components for CH3 on the 1604.

All four channels operate identically, hence only Channel 1 is described below.

This circuit provides the input coupling control and the x1 and x100 attenuators. RL101 controls the AC/DC coupling. Gnd is achieved by having RL102 and RL103 open circuit with RL104 closed. Q111 is activated to provide a low impedance path to ground.

See also the table of control settings and attenuator ranges after the description of circuit block 3.

Measurements:

	x1	x100	AC	DC	Gnd
RL101 pin 3	-	-	0V	4V	0V
RL102 pin 3	0V	4V	-	-	0V
RL103 pin 3	4V	0V	-	-	0V
RL104 pin 2	0V	4V	-	-	4V
Q111 gate	-12V	-12V	-	-	0V

x1 attenuation on ranges 2mV to 0.2V per division
x100 attenuation on ranges 0.5V to 20V per division

2 Attenuator Relay Control

This circuit consists of:

U120 to U125, Q123 to Q125 and associated discrete componets

This circuit provides the source currents to activate the attenuator relays. U120 to U122 form a 24 bit shift register which are used to extract the control signals from the serial bus interface. Their outputs are at CMOS levels and select transistors U123 to U125 and Q123 to Q125. When active these transistors close the contacts on the appropriate relay.

See Figure 5.4.11 for Serial Bus Timing

Measurements:

U120 pin 15	0V	RL101 open
U120 pin 15	5V	RL101 closed
U123 pin 16	4.6V	RL101 closed
U123 pin 16	0V	RL101 open
U123 pin 1	4V	RL101 closed
U123 pin 1	0V	RL101 open

3 Hybrid Amplifier/Attenuator

This circuit consists of

for Channel 1: U101, RL105, RL106 and associated discrete components

for Channel 2: U201, RL205, RL206 and associated discrete components

for Channel 3: (1602 CH2) U301, RL305, RL306 and associated discrete components

for Channel 4: U401, RL405, RL406 and associated discrete components

CH2 on the 1602 is handled by the components for CH3 on the 1604.

All four channels operate identically, hence only Channel 1 is described below.

circuit buffers the incoming signal and applies gain or attenuation to bring it to a predetermined level. The output is differential and is connected to the Pre-amplifier by a screened twisted pair. Channels 3 and 4 Pre-amplifiers are on the Four Channel board situated to the rear of the attenuators. On the 1602 the CH3 output is connected to the CH2 preamplifier.

Refer to Fig. 5.4.1 for Functional Diagram of this circuit.

RL105 and RL106 provide a low impedance divide by 10 attenuator with frequency compensation.

See also the attenuator settings in circuit block 1 description.

Measurements:

U101 pin 11	4.3V, current mode signal
U101 pin 12	4.3V, current mode signal
U101 pin 4	input signal, may be attenuated by 100:1
X2 to X20	-1V high control level
X2 to X20	-2.5V low control level
RL105 pin 3	0V relay open
,105 pin 3	4V relay closed

In the following table H stands for a high control level or relay closed and L stands for a low control level or relay open.

Table 5.4.1 Attenuator Control Settings

Volts/div	20mV	10mV	5mV	2mV	RL102	RL103	RL104	RL105	RL106
2mV	H	H	H	L	L	H	L	H	L
5mV	H	H	L	H	L	H	L	H	L
10mV	H	L	H	H	L	H	L	H	L
20mV	L	H	H	H	L	H	L	H	L
50mV	H	H	L	H	L	H	L	L	H
100mV	H	L	H	H	L	H	L	L	H
200mV	L	H	H	H	L	H	L	L	H
500mV	H	H	L	H	H	L	H	H	L
1V	H	L	H	H	H	L	H	H	L
2V	L	H	H	H	H	L	H	H	L
5V	H	H	L	H	H	L	H	L	H
10V	H	L	H	H	H	L	H	L	H
20V	L	H	H	H	H	L	H	L	H
GND	X	X	X	X	L	L	H	X	X

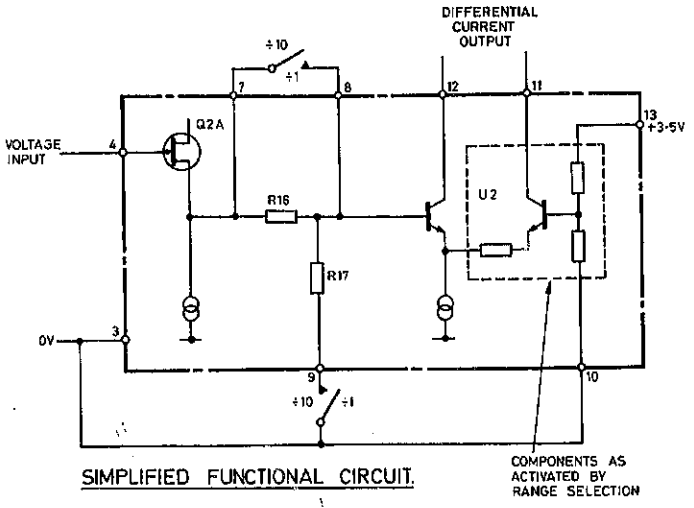


Fig 5.4.1 1600 Hybrid Preamplifier

4 Hybrid Control Logic

This circuit consists of:

U126, U127 and associated discrete components

This circuit extracts the control information for the hybrid gain/attenuator settings from the serial bus. U126 and U127 form a 16-bit shift register. Each hybrid requires 4 bits of data for the X2, X5, X10 and X20 controls.

See Fig. 5.4.12 for Serial Bus Timing.

Measurements:

U126 pin 15	0V X2 inactive
U126 pin 15	5V X2 active
U126 pin 14	serial data in
U127 pin 9	serial data out

5 Voltage Control

This circuit consists of:

U129 on the main board & U129 on the Four Channel PCB

These integrated circuits generate voltages which are used to remove the offsets generated in the hybrids and pre-amplifiers (and also when Add mode is selected). Each IC contains six voltage output DACs which are interfaced to the microprocessor through the serial bus.

Function	DAC
Add mode balance (CH1 + CH2)	U129c (pin 6)
Add mode balance (CH3 + CH4)	U129c (pin 6) (On Four Channel Board)
CH1 Attenuator Bal	U129a (pin 3)
CH2 Attenuator Bal	U129f (pin 16)
CH3 Attenuator Bal	U129d (pin 12)
CH4 Attenuator Bal	U129a (pin 3) (On Four Channel Board)

CH1 Pre-amp Offset	U129b (pin 5)
CH2 Pre-amp Offset	U129e (pin 14)
CH3 Pre-amp Offset	U129b (pin 5) (On Four Channel Board)
CH4 Pre-amp Offset	U129e (pin 14) (On Four Channel Board)

See Figure 5.4.11 for serial bus timing

Measurements:

U129 pin 3	0V Minimum
U129 pin 3	12V Maximum

6 Buffer Amp and Bandwidth Limit

This circuit consists of

for Channel 1: Q101 to Q104 and associated discrete components

for Channel 2: Q201 to Q204 and associated discrete components

for Channel 3: Q301 to Q304 and associated discrete components

for Channel 4: Q401 to Q404 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. All four circuits operate identically, hence only Channel 1 is described below.

This circuit buffers and voltage shifts the output signal from the hybrid (circuit block 3) and applies the bandwidth limit when in storage mode. Bandwidth limit is effected through Q103, Q104 and capacitors C117 and C119 and has an upper 3dB point of 5MHz.

Measurements

Q101 base	3.5V
Q101 emitter	4.2V
Q101 collector	-110mV trace top of screen
Q101 collector	-170mV trace bottom of screen
Q103 base	0V non-storage mode
Q103 base	0.7V storage mode

7 Variable Gain and Invert Amplifier

This circuit consists of

for Channel 1: U106, U107 and associated discrete components

for Channel 2: U206, U207 and associated discrete components

for Channel 3: U306, U307 and associated discrete components

for Channel 4: U406, U407 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. All four circuits operate identically, hence only Channel 1 is described below.

This circuit takes the differential output from the buffer amp (circuit block 6) and applies a fixed gain, a variable gain and/or invert, depending of the chosen selections. The balanced modulator U106 provides the variable gain and invert, both of these functions being controlled by U107 and its two control lines.

In addition to the above functions, the overall channel gain and frequency response are set by R131 and C121 respectively in this amplifier.

Measurements:

Note: The measurements given for U106 pins 2 and 10 below assume that no invert or variable gain has been applied. With invert the voltages given for top and bottom of screen are reversed.

U106 pin 2	-170mV trace top of screen
U106 pin 2	-110mV trace bottom of screen
U106 pin 10	-110mV trace top of screen
U106 pin 10	-170mV trace bottom of screen
U106 pin 14	5.65V trace top of screen
U106 pin 14	5.4V trace bottom of screen
U106 pin 11	2.61V normal
U106 pin 11	2.45V invert
U106 pin 11	2.71V maximum variable gain
U106 pin 4	2.45V normal
U106 pin 4	2.61V invert
U106 pin 4	2.69V maximum variable gain
U107 pin 6	3.4V
U107 pin 4	-2.4V normal
U107 pin 4	0.13V invert
U107 pin 9	-2.61V no variable gain
U107 pin 9	-4.25V maximum variable gain

8 Y Shift and Output Amplifier

This circuit consists of

for Channel 1: U110, Q105 to Q107 and associated discrete components

for Channel 2: U210, Q205 to Q207 and associated

for Channel 3: U310, Q305 to Q307 and associated discrete components

for Channel 4: U410, Q405 to Q407 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. All four circuits operate identically with the exception of the X-Y pickoff, which is present on Channel 1 only.

This circuit takes the differential output from the variable gain and invert amplifier (circuit block 7) and adds the Y shift. It also supplies two pickoffs, one to the trigger circuit (circuit block 29) the other to the X signal selector (circuit block 27) to provide realtime X-Y. Both of these signals are taken before Y shift is added.

Y shift is achieved by adding a differential current supplied by U109 (circuit block 9) to the input signal. The resultant output is sent to the ADC input beam switch.

U110 is used to provide an accurate voltage drop.

Measurements:

Q106 base	3.5V	
Q105 base	5.65V	trace top of screen
Q105 base	5.4V	trace bottom of screen
U110 pin 2	170mV	trace top of screen
U110 pin 2	-100mV	trace bottom of screen
U110 pin 1	U110 pin 2 4.4V	
N103 pin 9	-0.3V	trace top of screen
N103 pin 9	-0.46V	trace bottom of screen
Q106 collector	2.0V	trace top of screen
Q106 collector	2.25V	trace bottom of screen
Q107 collector	2.25V	trace top of screen
Q107 collector	2.0V	trace bottom of screen

9 Y Shift DAC

This circuit consists of

for Channel 1: U108, U109 and associated discrete components

for Channel 2: U208, U209 and associated discrete components

for Channel 3: U308, U309 and associated discrete components

for Channel 4: U408, U409 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. All four circuits operate identically, hence only Channel 1 is described below.

This circuit provides the differential current used to generate the Y shift. The digital setting for this is received over the serial bus via U108.

Measurements:

U109 pin 2	4.25V	maximum shift up
U109 pin 2	0.2V	maximum shift down
U109 pin 4	0.2V	maximum shift up
U109 pin 4	4.25V	maximum shift down
U109 pin 14	0V	
U109 pin 15	0V	

10 ADC Beam Switch

This circuit consists of

for Channels 1 and 2: U701a,e, U703, Q701 to Q704 and associated discrete components

for Channels 3 and 4: U701a,e, U703, Q701 to Q704 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. Both circuits operate identically, hence only the main board circuit is described below.

This circuit takes in the outputs of the Channel 1 and 2 preamplifiers and provides one of three outputs: Channel 1, Channel 2 or Channel 1 summed with Channel 2.

In storage mode the operation of the beam switch is dependent on the number of channels selected. With only one channel the output is the selected channel. However, with both channels selected the beam switch swaps between the two at a rate of 50ns per channel.

In non-storage mode the operation is slightly more complex. In single channel the beam switch outputs the selected channel, as before. In dual channel there are two different modes, chop and alternate. In chop the beam switch swaps between the two channels at a rate of 5us per channel. In alternate the beam switch swaps channels at the end of each sweep; the frequency of this is dependent on the timebase speed and the trigger rate.

In Add mode both channels are selected and any offset so generated is removed by the Add Balance control voltage.

Measurements:

U703 pin 13	0V	Channel 1 selected
U703 pin 13	5V	Channel 1 not selected
U703 pin 9	0V	Channel 2 selected
U703 pin 9	5V	Channel 2 not selected
D704 pin 1	3.4V	Channel 1 selected
D704 pin 1	0.7V	Channel 1 not selected
Q701 base	2.0V	trace top of screen
Q701 base	2.25V	trace bottom of screen
U701 pin 1	-1.8V	trace top of screen
U701 pin 1	-1.4V	trace bottom of screen
ADD BAL	12V	maximum
ADD BAL	-0.7V	minimum
U701 pin 14	-3.5V	single channel trace or add mode

11 ADC Driver Amplifier

This circuit consists of

for Channels 1 and 2: U701a,c,d, Q705, Q706 and associated discrete components

for Channels 3 and 4: U701a,c,d, Q705, Q706 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. Both circuits operate identically, hence only the main board circuit is described below.

This circuit buffers the output of the ADC beam switch. Its output drives the ADC input and the output beam switch. The signal path is through the ADC in storage mode and to the output beam switch in non storage mode.

The circuit forms a shunt feedback amplifier, the feedback being provided by R720. Q706 limits the positive excursion to prevent damage to U702, the ADC.

Measurements:

Q706 base	50mV	
U701 pin 4	-1.8V	trace top of screen
U701 pin 4	-1.4V	trace bottom of screen
Q705 emitter	-150mV	trace top of screen
Q705 emitter	-1V	trace centre of screen
Q705 emitter	-1.85V	trace bottom of screen

12 Analog to Digital Converter

This circuit consists of

for Channels 1 and 2: U702, U704 and associated discrete components

for Channels 3 and 4: U702 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. The main board circuit contains the master voltage reference in addition to the ADC, hence this circuit is described below.

The ADC takes the output from the ADC driver amp (circuit block 11) and converts the signal into an 8-bit digital word. The conversion rate is one sample every 50ns irrespective of the timebase speed. When both channels are selected the input signal chops between the two channels at a rate of 50ns per channel, and so, the digital output is multiplexed between the two in a similar way.

The digital output levels are TTL compatible.

See Fig. 5.4.2 for A.D.C. Timing.

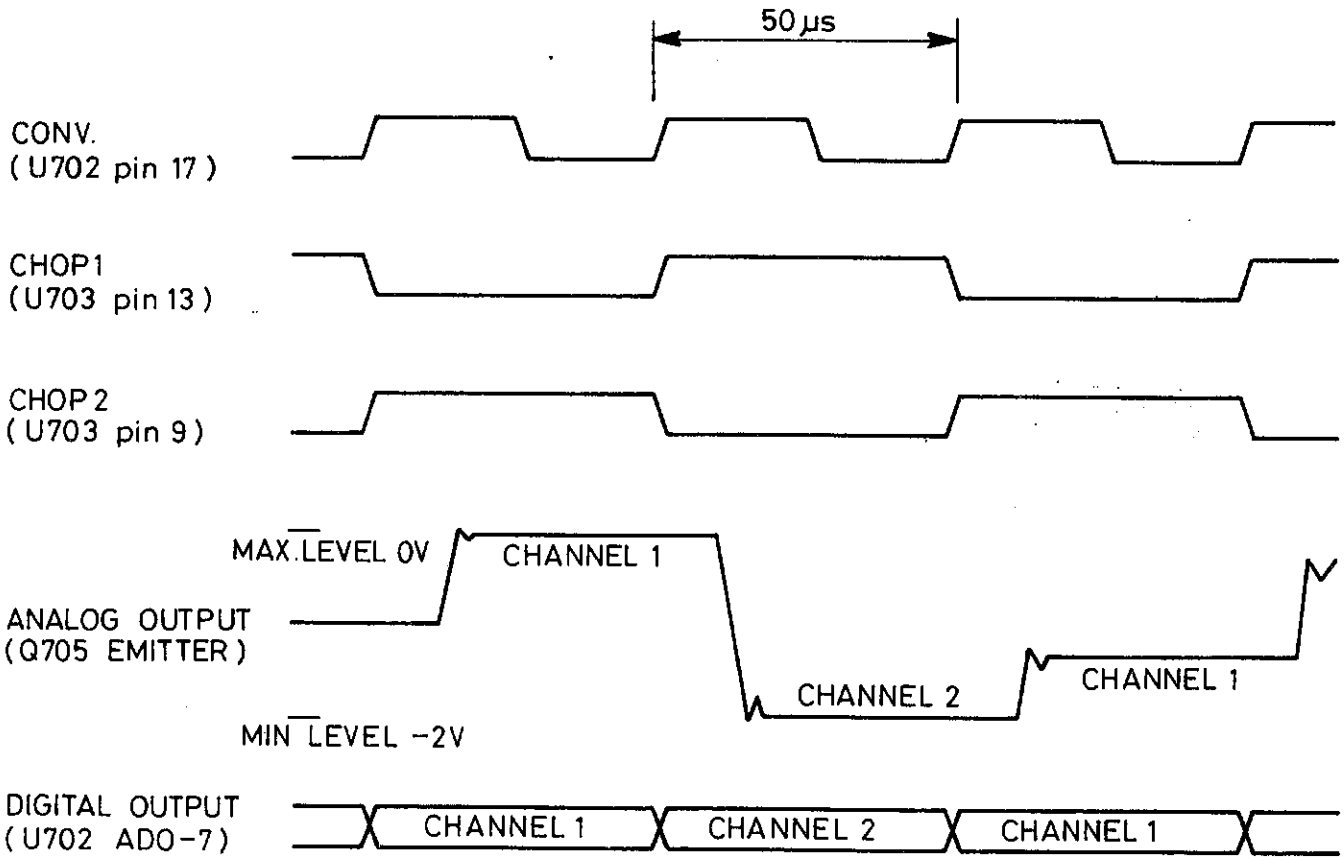


Figure 5.4.2 A/D Timing

Measurements:

U702 pin 20	-150mV	trace top of screen
U702 pin 20	-1.85V	trace bottom of screen
U702 pin 26	-2V	
U702 output	3.6V	min logic high
U702 output	0.7V	max logic low
U702 pin 17	20MHz	clock, TTL levels
U704 pin 1	-0.75V	

13 Y Output DAC

This circuit consists of:

U803, Q811 to Q816 and associated discrete components

The Y DAC receives an 8-bit data word from the display circuit and produces a current output proportional to the Y screen displacement. This output can reach the Y output beam switch (circuit block 13) by one of two routes. The straight path is used by all alphanumerics and stored traces when dot join is not selected, this is through Q811. The other path, which adds dot joining, is through Q812.

Q813 and Q814 change the alphanumerics gain and offset respectively, aligning the on-screen text with the numeric buttons.

Measurements:

U803 pin 14	0V	
U803 pin 15	0V	
U803 pin 4	-4.2V	dot join
U803 pin 4	-2.8V	no dot joining
Q812 base	-3.5V	
Q811 gate	-5V	dot join
Q811 gate	0V	no dot joining
Q813 base	0V	trace display
Q813 base	0.7V	alphanumerics display

14 Y Output Beam Switch

This circuit consists of:

U801c, U802, U804 and associated discrete components

The Y output beam switch accepts three signal inputs: CH1/CH2, CH3/CH4 and the Y DAC. The first two signals are the outputs from the ADC driver amps (circuit block 11), the third signal is from the Y output DAC (circuit block 14). Only one of these is presented to the Y beam switch amplifier at a time, and hence to the Y output stage. The Acquisition gate array selects which of these signals is to be displayed.

In storage mode only the Y DAC output is used.

Measurements:

U802 pin 14	1.6V	
U802 pin 9	0V	CH3/CH4 selected
U802 pin 9	2.2V	CH3/CH4 not selected
U802 pin 4	0V	CH1/CH2 selected
U802 pin 4	2.2V	CH1/CH2 not selected
U801 pin 8	0V	alpha and storage mode traces selected
U801 pin 8	2.2V	alpha and storage mode traces not selected
U802 pin 11	3.7V	
U804 pin 1	+5V	CH3/CH4 selected
U804 pin 4	+5V	CH1/CH2 selected
U804 pin 12	+5V	alpha selected

15 Y Beam Switch Amplifier

This circuit consists of:

U801 and associated discrete components

This circuit is a shunt feedback amplifier accepting the signal in current mode from the Y output beam switch (circuit block 13) and providing a differential voltage output to drive the Y output stage.

Measurements:

U801 pin 4	3.9V	
U801 pin 15	3.9V	
U801 pin 2	6.6V	trace top of screen
U801 pin 2	5.8V	trace bottom of screen
U801 pin 1	5.8V	trace top of screen
U801 pin 1	6.6V	trace bottom of screen
U801 pin 13	5.1V	trace top of screen
U801 pin 13	5.9V	trace bottom of screen

16 Y Output Amplifier Stage 1

This circuit consists of:

U1 and associated discrete components

These components can be found on the CRT driver PCB.

This circuit accepts the differential output from the Y beam switch amplifier, applies a small amount of gain and drives the Y Output Amplifier Stage 2 (tube driver). The overall Y gain is set by R4 and frequency compensation by C1.

Measurements:

U1 pin 4	5.1V	trace top of screen
U1 pin 4	5.9V	trace bottom of screen
U1 pin 16	8.8V	trace top of screen
U1 pin 16	7.2V	trace bottom of screen

17 Y Output Amplifier Stage 2

This circuit consists of:

Q1 to Q4 and associated discrete components

These components can be found on the CRT driver PCB.

This circuit takes the output of Y output stage 1 and drives the Y CRT plates directly. The circuit is formed from a differential pair, Q1 and Q2, and a cascode pair, Q3 and Q4. Extra frequency compensation is provided by C10.

WARNING *This circuit contains voltages up to 180V and due care should be taken when working on a live instrument.*

Measurements:

Q1 base	8.8V	trace top of screen
Q1 base	7.2V	trace bottom of screen
Q1 collector	11.5V	trace top of screen
Q1 collector	13.6V	trace bottom of screen
Q3 base	15.6V	
Q3 collector	34V	trace top of screen
Q3 collector	54V	trace bottom of screen
P8	68V	trace top of screen
P8	88V	trace bottom of screen

18 X DAC

This circuit consists of:

U28a,b, U930, U942, U935, U990, and associated discrete components

This circuit provides the analog X signal for the digital displays and the plot output. When dot join is applied to the display, the X signal is routed through U990 pin 5. The X signal is routed through U990 pin 3 when dot join is off. When menus are selected, the gain of the X DAC is changed by U942a and an offset is added to the trace by U942b.

Measurements:

U930 pin 16	0V	
U930 pin 17	0V	
U930 pin 4	0V	
U930 pin 2	-1V	no dot join
U930 pin 2	-2V	dot join
U942 pin 15	2.3V	trace display
U942 pin 15	2.0V	menu display
U942 pin 4	2.3V	trace display
U942 pin 4	2.0V	menu display
U942 pin 9	5V	menu display
U942 pin 9	0V	trace display
U942 pin 14	0V	not plotting
U942 pin 14	0V	left edge of plot
U942 pin 14	1.1V	right edge of plot
U990 pin 9	0V	dot join
U990 pin 9	5V	no dot join
U990 pin 10	5V	menu display
U990 pin 10	0V	trace display
U935 pin 7	2V	left edge of the screen
U935 pin 7	-3V	right edge of the screen

19 X Output Amplifier

This circuit consists of:

Q6 to Q11, Q24 to Q26 and associated discrete components

These components can be found on the CRT driver PCB.

This circuit is formed from a differential amplifier and two shunt feedback amplifiers. The transistors Q24 and Q25 form the differential amplifier with Q26 helping to reduce the effect of the short term thermal pulse response errors on Q24. The shunt feedback amplifiers each drive one of the X plates: Q7, Q8, Q11 and feedback resistor R50 for the X2 plate and Q6, Q9, Q10 and feedback resistor R57 for the X1 plate.

R131 sets the overall X gain. R133, C21 and C33 adjust the frequency response.

WARNING *This circuit contains voltages up to 180V and due care should be taken when working on a live instrument.*

Measurements:

	left edge	**right edge**
Q24 base	3.2V	4.0V
Q25 base	3.6V	3.6V
Q26 drain	9.7V	9.0V
Q25 collector	4.4V	4.4V
Q11 collector	57V	117V
Q10 collector	117V	57V
Q7 base	9.4V	
Q6 base	9.4V	
Q11 base	175V	
Q10 base	175V	

20 Brightup Combining Amplifier

This circuit consists of:

U50d, U910b,f, U940, Q902 and associated discrete components

This circuit combines the various digital blanking and brightup signals to produce the composite intensity signal used to the drive the brightup amplifier.

Measurements:

U940 pin 8	0V	blank alpha display
U940 pin 8	8V	max intensity alpha
U940 pin 2	0V	blank trace display
U940 pin 2	8V	max intensity trace
U940 pin 4	0V	alpha display
Q902 emitter	0.4V	blanked
Q902 emitter	-0.4V	maximum intensity

21 Brightup Amplifier

This circuit consists of:

Q14 to Q16 and associated discrete components

These components can be found on the CRT driver PCB.

This circuit takes the output from the intensity combining amplifier (circuit block 20) and drives the CRT grid. It is formed into a shunt feedback amplifier, the feedback being supplied by R77.

WARNING *This circuit contains voltages up to 75V and due care should be taken when working on a live instrument.*

Measurements:

PLCB9	0.4V	trace blanked
PLCB9	-0.4V	trace max intensity
Q16 base	0V	
Q14 base	67V	
Q15 base	0.7V	
Q15 collector	10V	(or less) trace blanked
Q15 collector	40V	trace max intensity

22 EHT Oscillator and Regulator

This circuit consists of:

Q17 to Q19, T1 and associated discrete components

These components can be found on the CRT driver PCB.

This circuit forms an oscillator and regulator. The frequency of oscillation is approximately 40kHz and its output drives the transformer, T1, which supplies power to the output multiplier stages (circuit block 21). Regulation is achieved with the feedback resistor R99 which is connected to the cathode supply.

Q19 forms the 40kHz oscillator.

Measurements:

Q17 collector	11.3V	maximum
Q18 collector	-1V	minimum, 30%
Q18 collector	3.5V	maximum, 70%

23 EHT Output Multipliers

This circuit consists of:

Q20, Q22, Q23, MX6 and associated discrete components

These components can be found on the CRT driver PCB.

Altogether there are four separate circuits in the block:

PDA Multiplier This circuit is formed from the MX6 multiplier only. It multiplies the transformer output to give the Post Deflection Anode (PDA) voltage.

Cathode Supply This circuit is formed from C69, D23, D24 etc. It doubles the voltage output from the transformer. This is smoothed to produce the DC cathode voltage.

Focus Supply This circuit is formed from Q22, Q23 etc. It is configured as a shunt feedback amplifier.

Brightup Bias Generator This circuit is formed from Q20 etc. It adds the grid bias voltage necessary to drive the tube to the brightup signal (produced in circuit block 21).

WARNING *These circuits contain voltages in excess of 8.5kV and due care should be taken when working on a live instrument. These voltages may be retained for up to a minute after power down.*

Measurements:

MX6 output	8.5kV	
P3	-1600V	cathode supply
Q20 emitter	10V	trace blanked
Q20 emitter	40V	trace max intensity
P4	-1700V	trace blanked
P4	-1600V	trace max intensity
Q22 base	-0.7V	
Q22 collector	-75V	maximum
Q22 collector	-180V	minimum
Q23 collector	-550V	maximum
Q23 collector	-750V	minimum
P5	-940V	maximum
P5	-1010V	typical
P5	-1140V	minimum

24 Display Gate Array and RAM

This circuit consists of:

U17e, U20 to U22 and associated discrete components

IC U20 controls the display and plot functions of the 1604. In addition the device also communicates directly with the Acquisition gate array so that traces may be transferred from acquisition RAM to display RAM. The functions controlled by this device include: acquisition to display transfers, trace displays (storage mode only), timebase clock, alphanumerics displays and transfers to and from the microprocessor.

U21 and U22 form the memory for the Display gate array:

U21 alpha and trace RAM
U22 alphanumerics pattern ROM

See Fig. 5.4.3 Display Data Timing.

Measurements:

U20 pin 54	1MHz micro. E clock
U20 pin 63	10MHz TTL clock
U20 pin 42	timebase clock
U20 pin 39	rising edge, DAC latch pulses
U20 pin 35	pulsed low, reading alpha ROM
U20 pin 2	pulsed low, reading display RAM

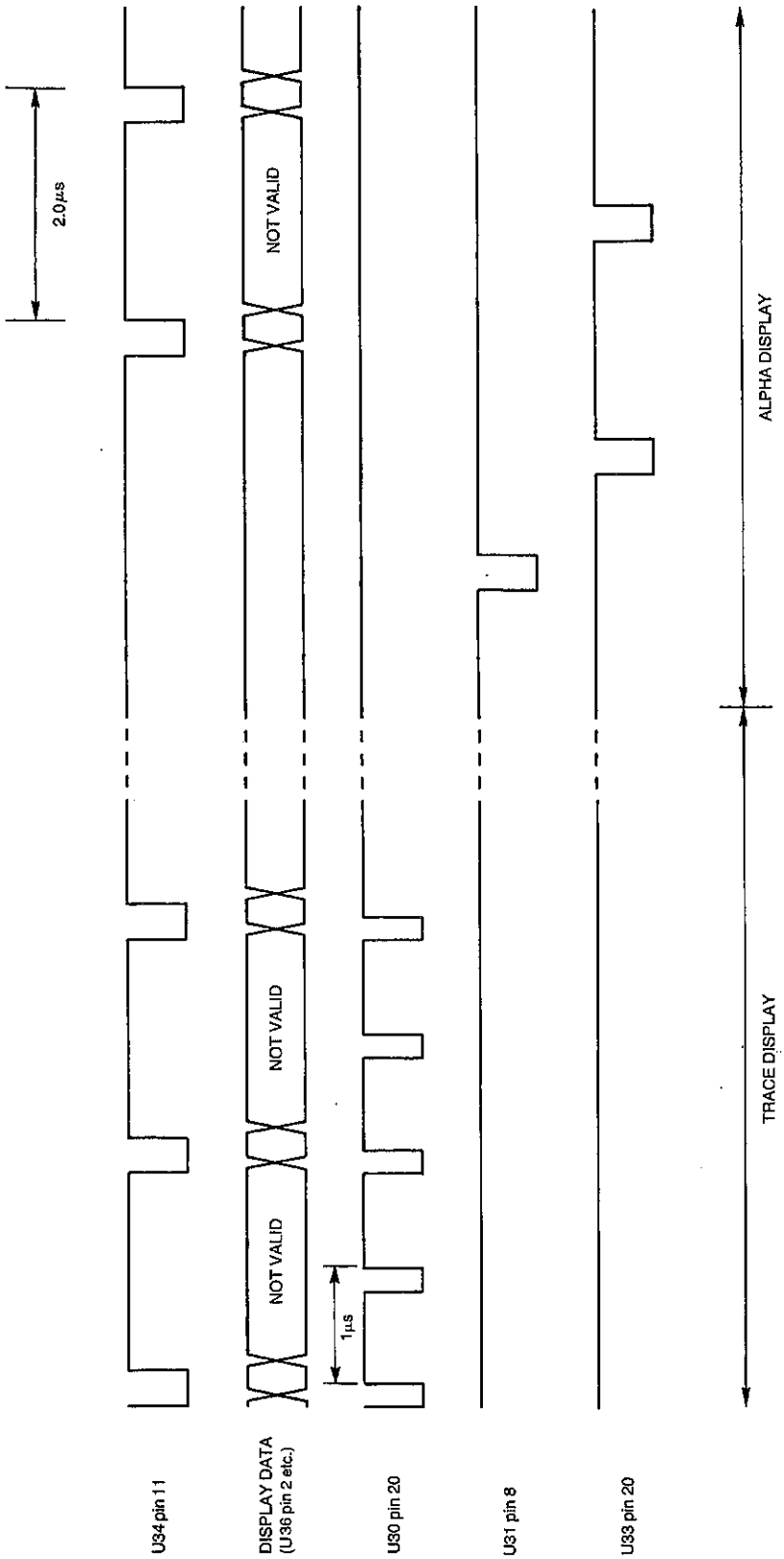


Figure 5.4.3 Display Data Timing

25 Display DAC Latches

This circuit consists of:

U14, U23, U24, U25, U27 and associated discrete components and logic gates

This circuit latches the data for the X and Y display DACs. The X components of the trace can be supplied from two places: U25 and U27 for normal Y-T traces and from U23 for X-Y traces. The Y output is latched in U24, a PAL: this ensures the trace limits correctly at the top and bottom of the screen when post-storage shift is applied.

Measurements:

U24 pin 11	+5V	upward PS shift
U24 pin 11	0V	downward PS shift
U24 pin 14	+5V	post-storage shift applied
U24 pin 14	0V	no post storage shift
U24 pin 10	+5V	trace not in limit
U24 pin 10	0V	trace in limit
U24 pin 1	rising edge at the start of each displayed dot	
U25 pin 1	0V	normal Y-T trace display
U25 pin 1	+5V	X-Y trace display

26 X Shift DAC and Control

This circuit consists of:

U601, U603, U605b,c, and associated discrete components

The X shift information is extracted from the serial bus by U601 which supplies the eight most significant bits. The lowest two significant bits are supplied by U602 which forms part of the analog timebase circuit (circuit block 28). Of the two outputs of the DAC one is sent to the analog timebase circuit and the other to the X DAC circuit (circuit block 18). To give extra precision in analog shift the two least significant bits are added in via resistors on the timebase circuit side only.

Measurements:

U603 pin 14	0V	
U603 pin 15	0V	
U603 pin 2	0V	
U603 pin 4	-1.8V	maximum left shift
U603 pin 4	1.8V	maximum right shift
U605 pin 8	-6V	maximum left shift
U605 pin 8	6V	maximum right shift
U605 pin 7	-1.6V	maximum left shift
U605 pin 7	-0.75V	maximum right shift

27 X DAC Buffer and Selector

This circuit consists of:

U605d, U609 and associated discrete components

The X DAC output is amplified by U605d where an offset adjustment is supplied by R646. When alphanumerics or digital trace displays are in progress the output of U605d passes straight through U609 to the X output amplifier (circuit block 19). However, in non-storage mode the output of U609 takes the ramp output of U604 (circuit block 28).

Measurements:

U605 pin 14	6.2V	left edge of screen
U605 pin 14	7.2V	right edge of screen
U609 pin 14	6.2V	left edge of screen
U609 pin 14	7.2V	right edge of screen
U609 pin 2	6.2V	real time trace display left edge of screen
U609 pin 2	7.2V	real time trace display right edge of screen

28 Analog Ramp Generator

This circuit consists of:

Q601 to Q603, Q605, U602, U604, U605a, U606a, U607 and associated discrete components

The analog ramp is generated by charging a capacitor with a constant current. The value of the capacitor and the current used determine the slope of the ramp and hence the sweep speed. These values are set by U602 which extracts the information from the serial bus.
One of a range of constant currents is selected by inputs DFE and flows into TCO (Timing Current Out). With one of the selected capacitors C611/12/13 this generates a linear ramp which is fed via U605a, U607a into the RAMP input of U604.

The ramp is combined with the Shift input, inverted and is output from OE (Output Emitter). The ramp then passes through U609 which switches between ramp and alpha signals and is output on XOP PLCRA6 to the CRT board. Alpha-numeric signals are fed in via P601, P602.

The ramp current is controlled by the current fed into U604 Pin 14 (Resistor Timing). Some of this current can be removed via R614 to allow adjustment by R607/8/9 and by the continuously variable control VAR-SW via Q605.

U604 Pin 7 (A) switches a x5 gain for X-expansion.

VREF is used as a reference voltage for the constant current generation. VM, Alpha and C are all grounded. CC and OC are connected to the positive supply. Pin 17 (Compensation Emitter) is a compensation output which is fed to the CRT board X-amplifier (Circuit Block 19) and to the alpha-numeric amplifier U605d.

U606a detects the ramp voltage level at the end of sweep and generates an output at EOS. RT XY (Real Time XY) is used in XY mode to force EOS low.

Other functions performed by this circuit:

Q601	discharges the capacitor at the end of the sweep
U606a	determines the end of sweep
U607a	selects between the analog ramp and the Channel 1 signal for X-Y
U607b	sets a correction current to compensate for any error in the capacitance value

See Fig. 5.4.4.

Measurements:

Q601 base	0.6V	sweep in progress
Q601 base	pulsed to -0.7V at end of sweep	
U605 pin 3	0V	left edge of screen
U605 pin 3	-1.75V	right edge of screen
U606 pin 7	0V	at end of sweep and in X-Y
U606 pin 7	+5V	sweep in progress
U607 pin 1	Channel 1 input signal	
U604 pin 2	6.2V	left edge of screen
U604 pin 2	7.2V	right edge of screen
U604 pin 17	6.6V	

Table 5.4.2 Timebase Control Settings

Timebase range	U602 C	D	E	F	G	H
10ms	L	H	H	L	L	L
5ms	L	H	H	H	L	L
2ms	L	H	H	H	H	L
1ms	H	L	H	L	L	L
0.5ms	H	L	H	H	L	L
0.2ms	H	L	H	H	H	L
0.1ms	H	L	L	L	L	L
50μs	H	L	L	H	L	L
20μs	H	L	L	H	H	L
10μs	H	H	H	L	L	L
5μs	H	H	H	H	L	L
2μs	H	H	H	H	H	L
1μs	H	H	L	L	L	L
0.5μs	H	H	L	H	L	L
0.2μs	H	H	L	H	H	L
X-Y	L	L	L	L	L	H

29 Trigger Source and Coupling Selector

This circuit consists of:

U503, U506 and associated discrete components

There are six possible trigger sources, Channels 1 to 4, External and Line (mains frequency). U503 selects one of these and applies AC coupling if selected. The IC provides two outputs, one to the TV Sync Separator (circuit block 28), and one to the Trigger level circuit (circuit block 30).

U506 extracts the selection information from the serial bus.

Measurements:

U503 pin 2	Channel 1 input signal
U503 pin 3	Channel 2 input signal
U503 pin 4	Channel 3 input signal
U503 pin 5	Channel 4 input signal
U503 pin 6	External Trig input signal
U503 pin 7	Line Trig input signal mains frequency 400mV pk-pk
U503 pin 13	3.4V maximum
U503 pin 13	2.2V minimum
U503 pin 9	270mV maximum
U503 pin 9	-70mV minimum

Table 5.4.3 Trigger Control Settings

Selection	U506 A	B	C	D	E	F	G
CH1	5V	0V	0V	0V	0V	-	-
CH2	0V	5V	0V	0V	0V	-	-
CH3	0V	0V	5V	0V	0V	-	-
CH4	0V	0V	0V	5V	0V	-	-
Ext	0V	0V	0V	0V	5V	-	-
Line	0V	0V	0V	0V	0V	-	-
DC	-	-	-	-	-	0V	-
AC/TV	-	-	-	-	-	5V	-
TV NON INV	-	-	-	-	-	5V	0V
TV INV	-	-	-	-	-	5V	5V

30 TV Sync Separator

This circuit consists of:

U501a, U502a,c, U512a, Q501, Q502, Q506, Q507 and associated discrete components

This circuit takes the special TV output from the trigger source and coupling selector (circuit block 29) and provides line and field pulses. Q502 forms a peak-detecting sample and hold, storing a voltage just below the level of the sync pulses. U512 detects the line sync pulses and these are fed to Q507 which detects the field pulses.

See Figs. 5.4.5, 5.4.6, 5.4.7.

Measurements:

Q506 base	2V	maximum
Q506 base	1.65V	minimum
U512 pin 2	1.9V	typically
Q502 gate	-12V	S & H gate open
Q502 gate	5V	S & H gate closed
U501 pin 5	rising edge on start of sync pulse	
U501 pin 6	32μs	wide pulse
U502 pin 1	0V	field sync pulse, low for 500ns
U502 pin 1	5V	no field sync pulse

31 Trigger Level DACs

This circuit consists of:

U504, U505, U507, U508, U510a and associated discrete components

This circuit produces the two trigger level voltages. These are required for the trigger window function, where U504 provides the mid-point level and U505 defines the width of the window. The digital data for U504 and U505 is extracted from the serial bus by U507 and U508 respectively.

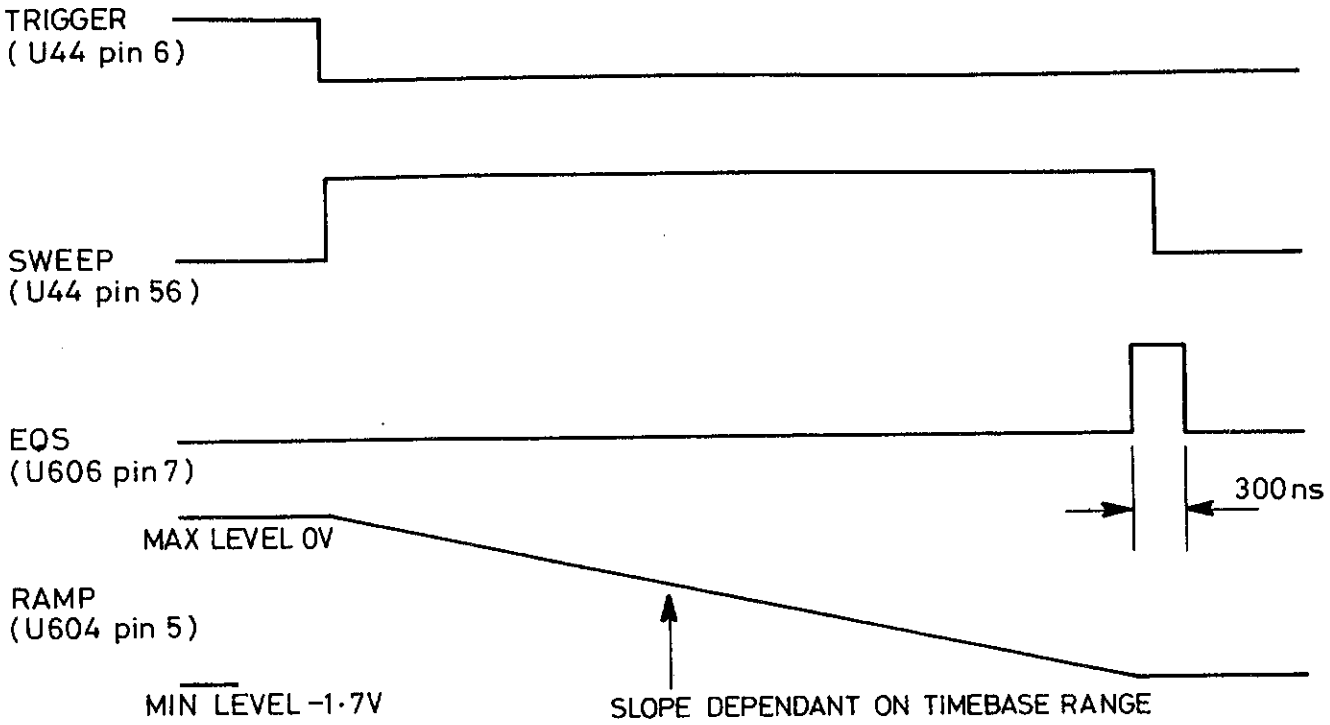


Figure 5.4.4 Real Time Trace Waveforms

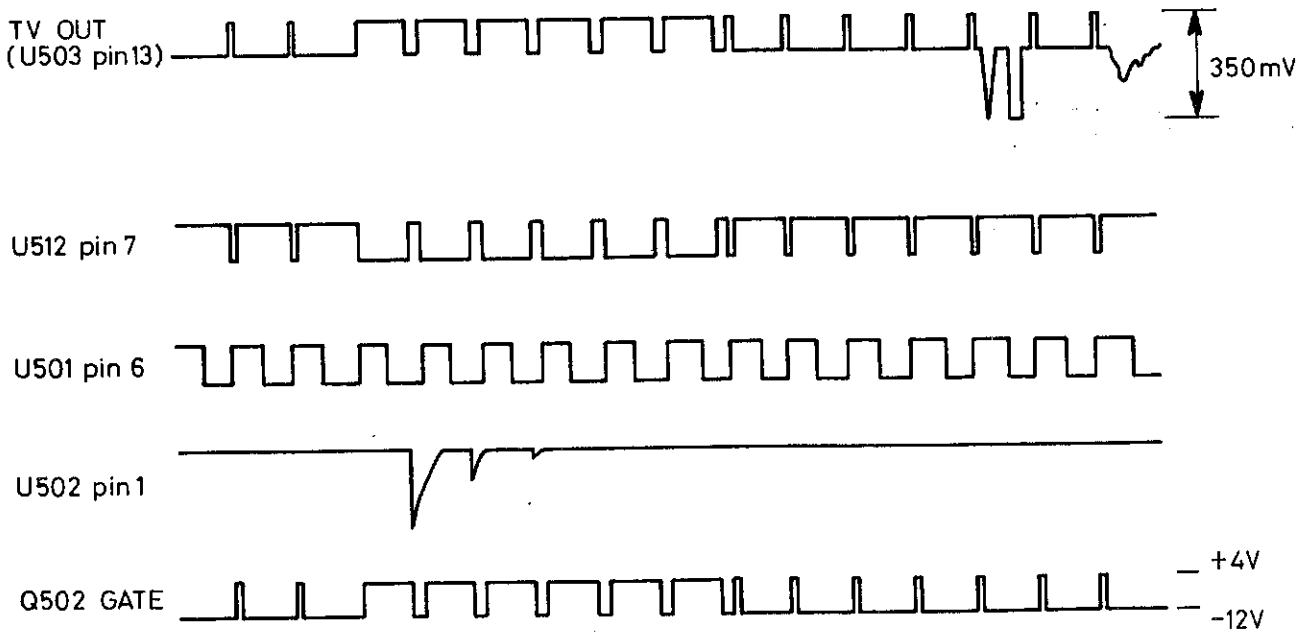


Figure 5.4.5 TV Sync Separator Waveforms

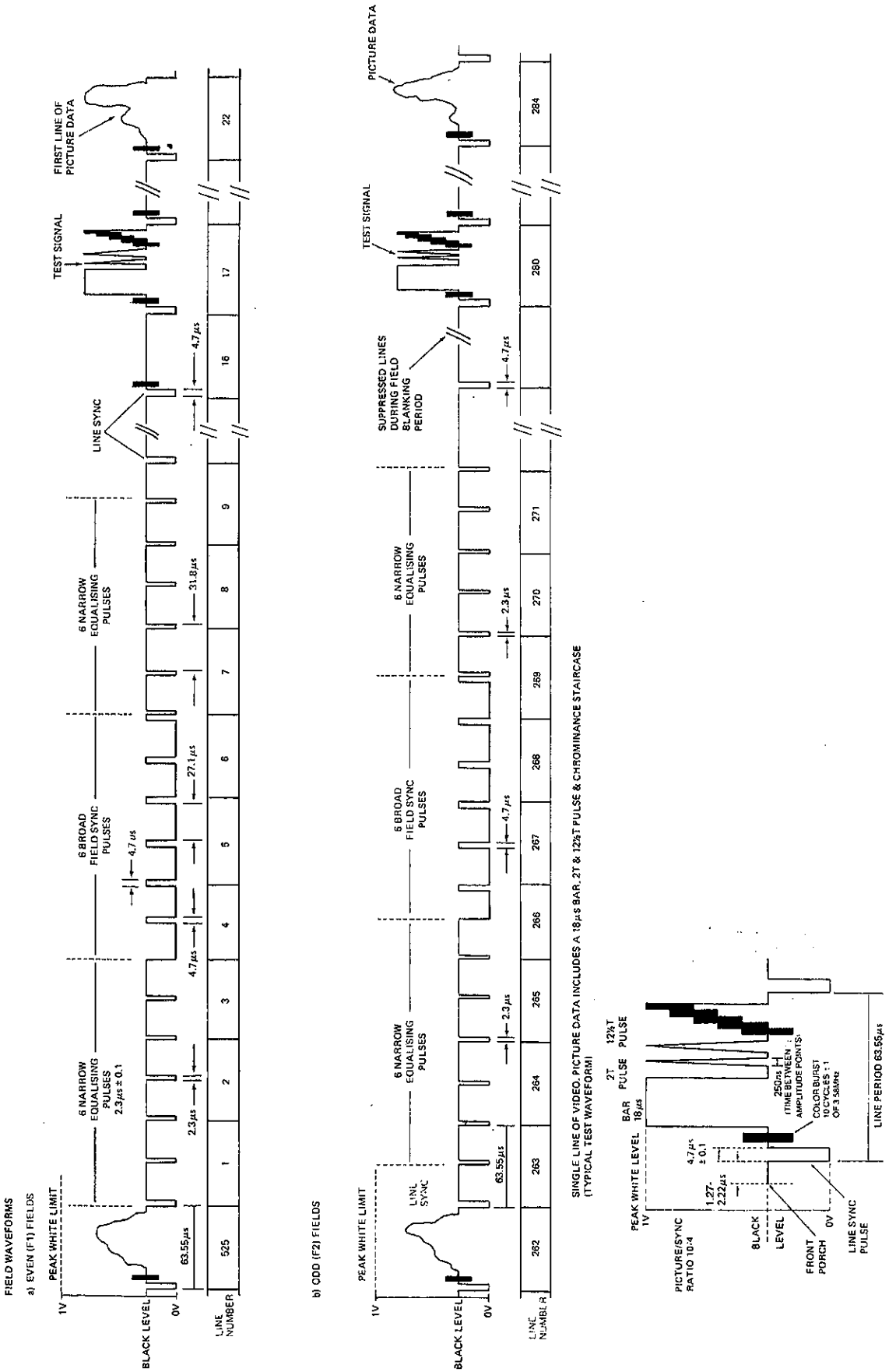


Figure 5.4.6 NTSC TV Waveforms

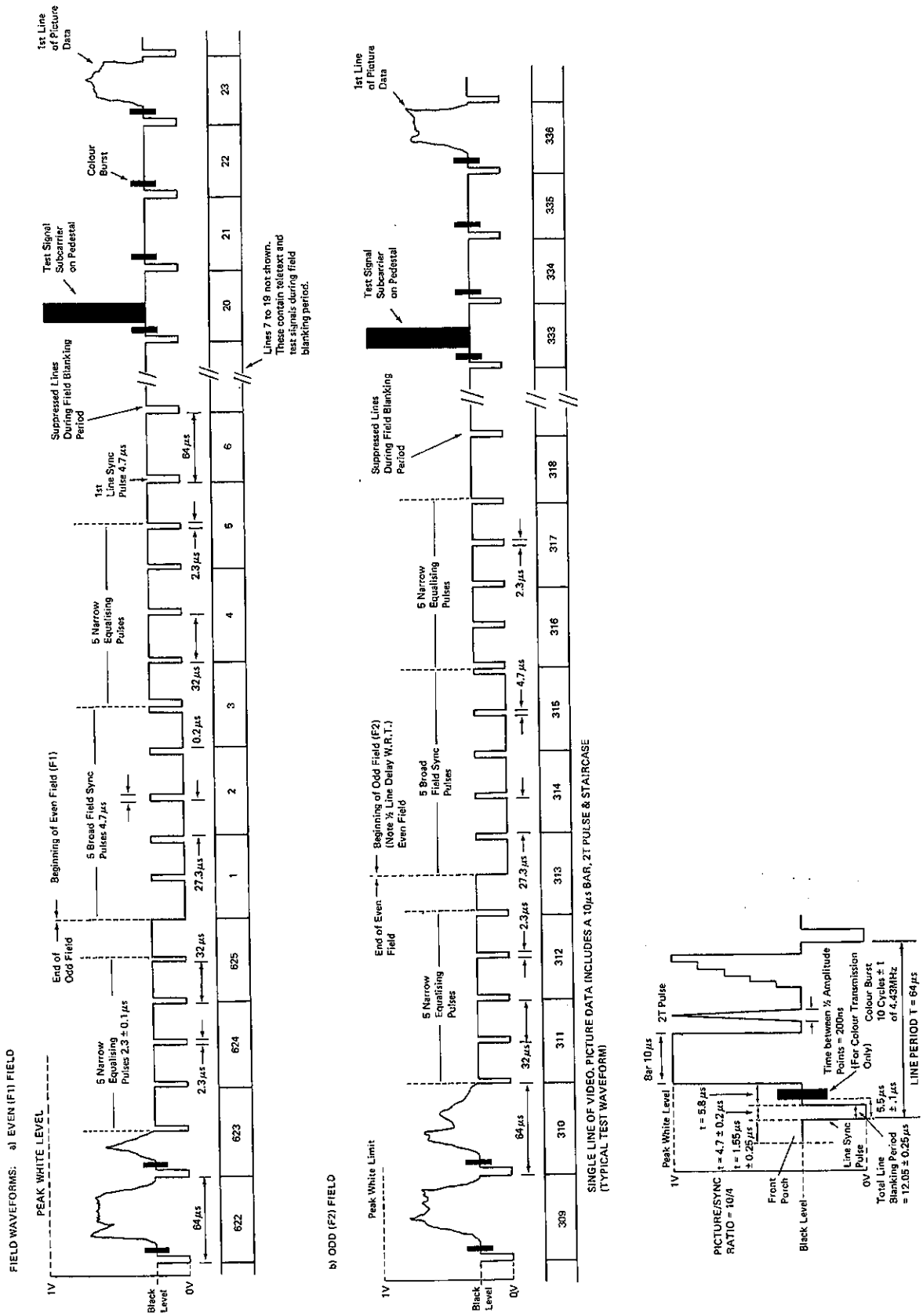


Figure 5.4.7 PAL TV Waveforms

Measurements:

U504 pin 14	0V	
U504 pin 15	0V	
U504 pin 4	0V	
U504 pin 2	0V	
U505 pin 14	0V	
U505 pin 15	0V	
U505 pin 4	0V	
U505 pin 2	0V	
U510a pin 1	200mV	maximum
U510a pin 1	-200mV	minimum

32 Trigger Level Comparator

This circuit consists of:

Q505, Q508, U501b, U502b, U509, U510c,d, U511a,c, and associated discrete components

This circuit compares the selected input signal with the trigger level, two digital outputs are produced: the trigger and triggered (indicating that triggers are present) outputs. The signal is buffered by Q508 and a low pass filter is applied by Q505 if this type of coupling is selected. U509 takes information from the serial bus to control the comparators and the low pass filter.

Measurements:

U510 pin 14	-200mV	minimum, no window
U510 pin 14	-60mV	minimum, max window
U510 pin 14	200mV	maximum, no window
U510 pin 14	350mV	maximum, max window
U510 pin 7	-200mV	minimum, no window
U510 pin 7	-350mV	minimum, max window
U510 pin 7	200mV	maximum, no window
U510 pin 7	60mV	maximum, max window
Q505 base	0.7V	low pass filter on
Q505 base	0V	low pass filter off
Q508 pin 5	300mv	maximum
Q508 pin 5	-50mV	minimum
Q508 pin 1	same vol	tage as Q508 pin 5
U509 pin 15	0V	TV coupling not selected
U509 pin 15	5V	TV coupling selected
U509 pin 1	0V	TV frame selected
U509 pin 1	5V	TV frame not selected
U509 pin 2	0V	+ve or TV coupling
U509 pin 2	5V	-ve, +/− on non TV coupling
U509 pin 3	0V	-ve or TV coupling
U509 pin 3	5V	+ve, +/− on non TV coupling
U502 pin 6	rising ed	ge, trigger received
U501 pin 10	0V	not triggered
U501 pin 10	5V	triggered

33 Power Supply

This circuit consists of:

U1 to U5, Q1,Q2, T1, BR1 to BR3 and associated discrete components.

These components, with the exception of T1, can be found on the power supply board situated to the rear right-hand side of the instrument. Transformer T1 is bolted to the rear panel.

This circuit provides the DC power requirements of the instrument. The tube EHT voltages are provided elsewhere, see circuit block 22. The rails are supplied by a series of linear regulators, U1 to U5, for -12V to +12V, and by the transistors Q1 and Q2 for 75V.

WARNING *These circuits contain voltages in excess of 250V on the secondary windings and the line input voltages on the primary windings of T1. Due care should be taken whilst working on a live instrument.*

Measurements:

U2 pin 3	22V	plus 1.5V pk-pk ripple
P2	4.8V	minimum
P2	5.2V	maximum
U1 pin 1	22V	plus 1.5V pk-pk ripple
P1	11.8V	minimum
P1	12.2V	maximum
U3 pin 2	-22V	plus 5V pk-pk ripple
U3 pin 1	-10.4V	
P5	-12.3V	minimum
P5	-11.7V	maximum
P6	5V	pk-pk at line frequency
U4 pin 1	-4V	
C14	-1.5V	
P7	-5.2V	minimum
P7	-4.8V	maximum
P8	170V	minimum plus 1V ripple
P8	190V	maximum plus 1V ripple
Q1 base	-0.7V	
Q2 base	0V	
Q2 collector	-17V	typical, 3V pk-pk ripple
P9	71V	minimum
P9	79V	maximum

34 X Plot Output Latches

This circuit consists of:

U15, U16 and associated discrete components

This circuit forms a 10-bit latch which is used to drive the X DAC during plotting.

Measurements:

U15 pin 11	rising edge, writing MSB of X plot latch
U16 pin 7	rising edge, writing LSB of X plot latch

35 Plot DACs

This circuit consists of:

U28d, U933, U934, U936, U937 and associated discrete components

This circuit provides the four Y plot outputs. The two dual DACs, U936 and U937, are connected to the microprocessor by the 8-bit bus. These four plot outputs are connected to the miscellaneous I/O connector on the rear panel. The circuitry associated with U937 is not fitted on the 1602.

Measurements:

U936 pin 4	2.5V	
U937 pin 4	2.5V	
U936 pin 2	0V	
U936 pin 3	0V	maximum
U936 pin 3	-2.5V	minimum
U933 pin 7	0V	not plotting
U933 pin 7	-440mV	minimum during plot
U933 pin 7	440mV	maximum during plot
U936 pin 15	pulsed low, writing to DAC	

36 Acquisition Control

This circuit consists of:

U44, U50, U51, U53, U54, U56, U57 and associated discrete components

This circuit controls the acquisition of data from the ADC output and the selection of channels during analog sweeps. This circuit also controls the mode by which the data is captured. The options are: X-Y, Refreshed, Roll and Pre-trigger roll. In addition, the Acquisition gate array, U44, controls other functions: Acquisition to Display store transfers, beam switching of the analog traces and control of the data flow through the Data Control gate array. The rate of acquisition is determined by the A and B clocks from the Display gate array (circuit block 24).

U44 pin 55 is pulsed low to indicate to the Display gate array that an alpha sweep can be performed if required.

See Fig. 5.4.9

Measurements:

U44 pin 56	5V Ramp in progress
U44 pin 56	0V hold off
U44 pin 62	pulsed low at end of ramp
U44 pin 68	0V alpha sweep complete
U44 pin 68	5V alpha sweep in progress
U44 pin 63	0V alpha sweep finished
U44 pin 37	5V CH1 selected (non storage)
U44 pin 37	0V CH1 not selected
U44 pin 38	5V CH2 selected (non storage)
U44 pin 39	5V CH3 selected (non storage)
U44 pin 43	5V CH4 selected (non storage)
U44 pin 41	5V alpha selected
U44 pin 1	pulsed low during micro access to gate array
U44 pin 67	1MHz micro. E clock
U44 pin 42	blanking signal

37 Data Control and Acquisition RAMs

This circuit consists of

for CH1 and CH2:U45 to U48 and associated discrete components

for CH3 and CH4:U45 to U48 and associated discrete components

The components for Channels 1 and 2 can be found on the Main PCB and those of Channels 3 and 4 on the Four Channel PCB. Both circuits operate identically, hence only the Main board circuit is described.

This circuit controls the flow of data from the ADC to the Acquisition RAMs and from the Acquisition RAMs to the Display RAM. Glitch Detect is provided on the path from the ADC to the Acquisition RAMs and Max-Min on the path to the Display RAM. The setup information is received by the Data Control gate array from the serial bus. This includes commands about the number of active channels, whether Max-Min and Glitch Detect are selected and the number of data bytes per sample period.

See Fig. 5.4.8.

Measurements:

U48 pin 8	Acquisition to Display transfer clock
U48 pin 57	Acquisition to Display transfer handshake line
AD bus	ADC data output bus
AA bus	RAM 1 data bus
BA bus	RAM 2 data bus
CA bus	RAM 3 data bus
LD bus	Display RAM bus

38 Microprocessor

This circuit consists of:

U1 to U3, U7 to U9, U11c, U12b,c,d, U13a, U29, U30 and associated discrete components

This circuit includes the microprocessor which controls the 1604 system. The main program is split in two parts: U2 the boot-up ROM and the paged I.C.s in the auxiliary program ROMs. Additional ROMs can be attached to the system through the option interfaces on the rear panel.

MRDY is used to stretch the bus access times when the Display gate array or real time dock in the waveform processor interface pod aer accessed.

U1	main microprocessor
U8 & 9	buffers the address bus
U7	buffers the data bus
U2	boot ROM
U3	system RAM
U29	Auxiliary program ROM
U30	control latch

For details of the bus timing see a 68B09 data sheet.

See Fig. 5.4.10 for Memory address decoding

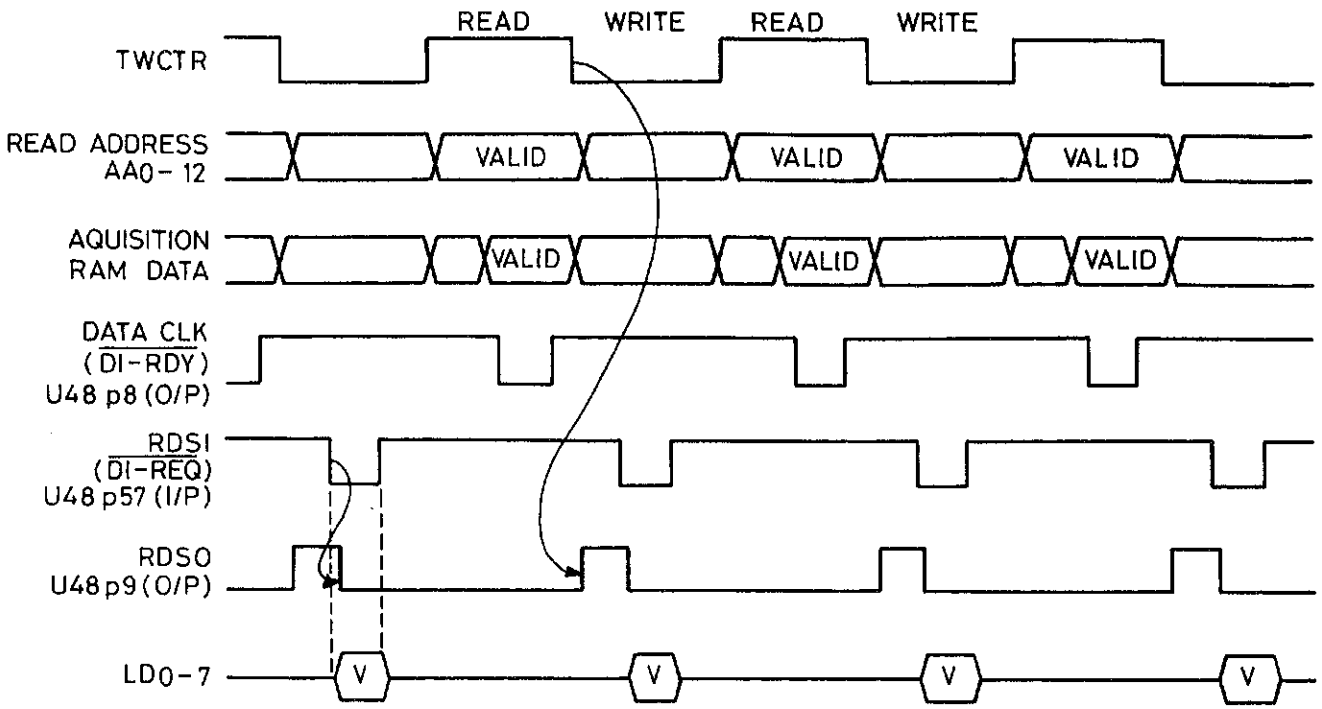


Figure 5.4.8 Acquisition To Display Transfer Timing

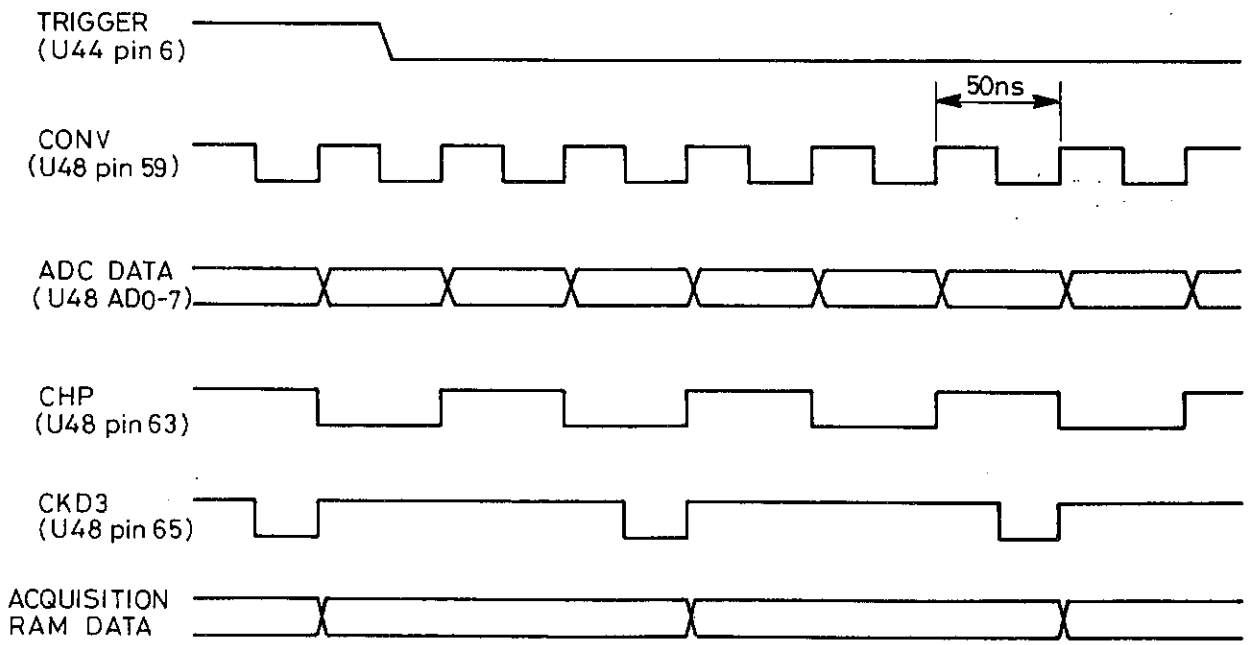


Figure 5.4.9 Acquisition Timing

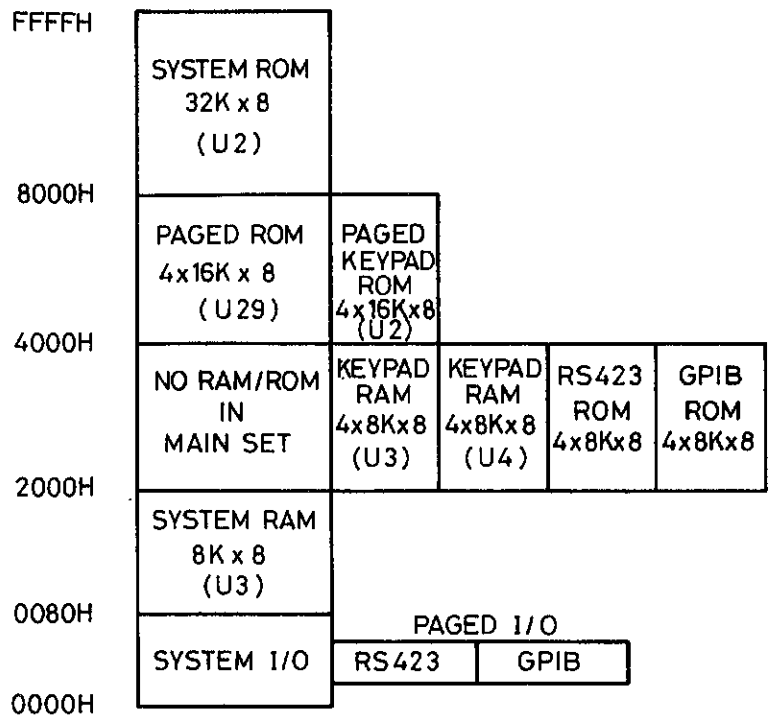


Figure 5.4.10 High Level Address Decoding

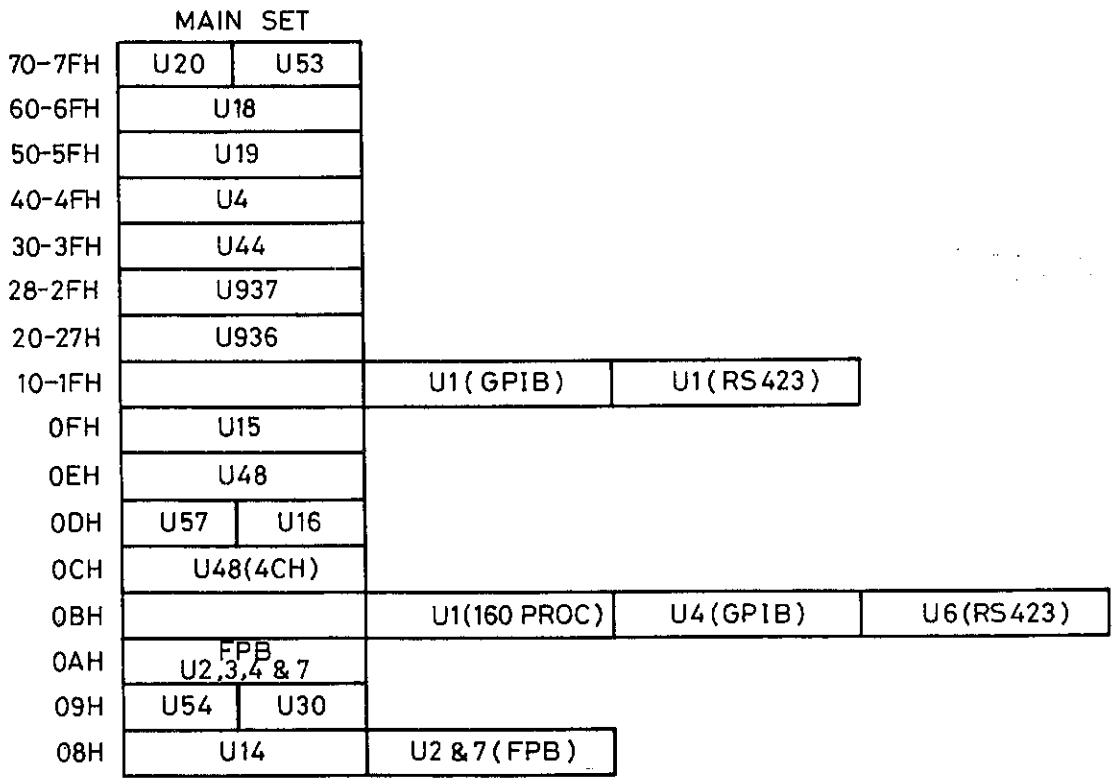


Figure 5.4.11 Low Level Address Decoding

Measurements:

U1 pin 34	1MHz micro. E clock	
U1 pin 35	1MHz clock, 90 degrees out of phase with pin 34	
U1 pin 2	pulsed low on TV frame odd field	
U1 pin 3	pulsed low for alpha display request	
U30 pin 9	rising edge write to control latch	
U30 pin 15	0V	dot join selected
U30 pin 15	5V	no dot join
U30 pin 10	0V	no post-storage shift
U30 pin 10	5V	post-storage shift
U30 pin 7	0V	post-storage shift down
U30 pin 7	5V	post-storage shift up

39 Low Level Address Decoding

This circuit consists of:

U5, U6, U10, U11a,b, U12a,e,f, U13b,c,d, U17b,c and associated discrete components

This circuit decodes the buffered address bus to provide the chip select pulses for the system ports, latches and gate arrays.

See Fig. 5.4.11 for address information.

40 Miscellaneous Control Latch

This circuit consists of:

U4, Q2, Q3 and associated discrete components

This circuit provides many outputs that control widely varying functions throughout the 1604 system.

PA0-2	serial bus to drive front panel LEDs
PA3	clear keyboard scan circuit
PA4-7	DAC serial bus
PB0	Y pre-amp serial bus latching pulse
PB2	timebase serial bus latching pulse
PB3	trigger serial bus latching pulse
PB4	X Magnification (on/off)
PB5	penlift (up/down)
PB6	X plot DAC (on/off)
PB7	realtime X-Y (on/off)
CB1	serial bus clock
CB2	serial bus data

See Fig. 5.4.12 for Serial Bus Timing

41 Keypad and Printer Interface

This circuit consists of:

U18, U31 and associated discrete components

This circuit interfaces the keypad and printer to the microprocessor. When a Keypad option is fitted, serial data representing the keys pressed is received. The UART, U18, converts this to parallel format for the microprocessor. The printer interface, when fitted, receives its commands in serial form transmitted by the UART.

Measurements:

U18 pin 27	1MHz micro. E clock
U18 pin 12	Keypad serial data
U18 pin 10	Printer serial data
U18 pin 17	0V keypad option fitted
U18 pin 17	5V no keypad fitted
U31 pin 3	3.2V
U31 pin 6	2.8V

42 Battery Back-up Control

This circuit consists of:

U19, B1 and associated discrete components

This circuit provides back-up power for the system RAM. Access to the system RAM is inhibited until repeated line trigger pulses are received. When these disappear it gives an early warning that the power is about to be removed and access to the system RAM is again inhibited to stop it being corrupted during power down. U19 also controls MRDY to the microprocessor and chip selects to the Real Time clock, when the Real Time clock on the waveform processor interface is accessed.

Measurements:

U19 pin 2	Line trigger pulses
U19 pin 12	Real Time Clock enabled
U19 pin 13	system RAM enabled
U19 pin 16	5V normal operation
U19 pin 16	4V power off

43 Front Panel Switch Scanner

This circuit consists of:

U1 to U4 and associated discrete components

These components can be found on the Front Panel PCB.

This circuit is used by the microprocessor to scan the front panel switch matrix. U3 activates one row at a time, U1 detects when any key in the selected row is pressed and U2 passes the column information to the microprocessor enabling the pressed key to be determined.

See Fig. 5.4.14 for timing.

Measurements:

U1 pin 13	0V key pressed in the selected row
U1 pin 13	5V no key pressed in the selected row
U2 pin 3	serial data to micro.
U4 pin 1	rising edge, select next row
U3 pin 9	0V row 2 not selected
U3 pin 9	5V row 2 selected
U1 pin 2	0V CO18 not active
U1 pin 2	5V CO18 active

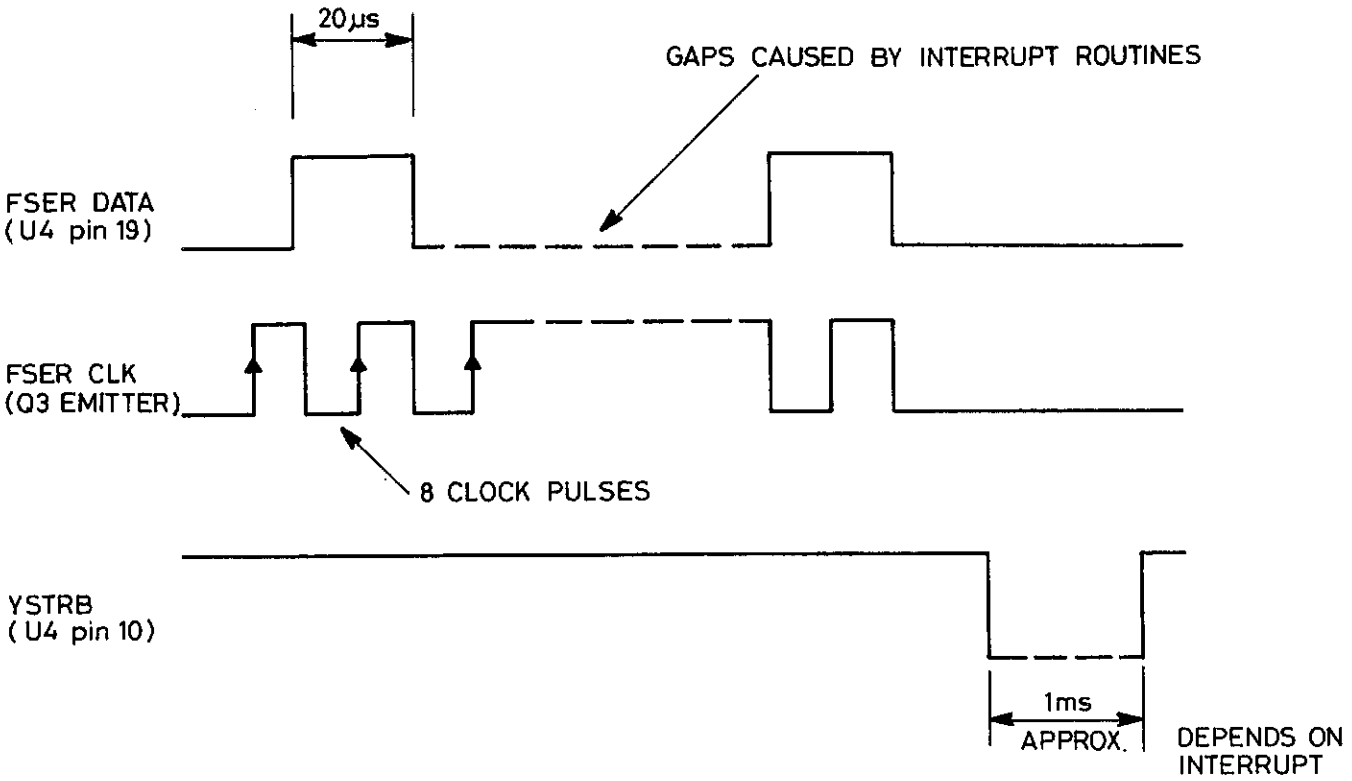


Figure 5.4.12 Typical Serial Bus Timing

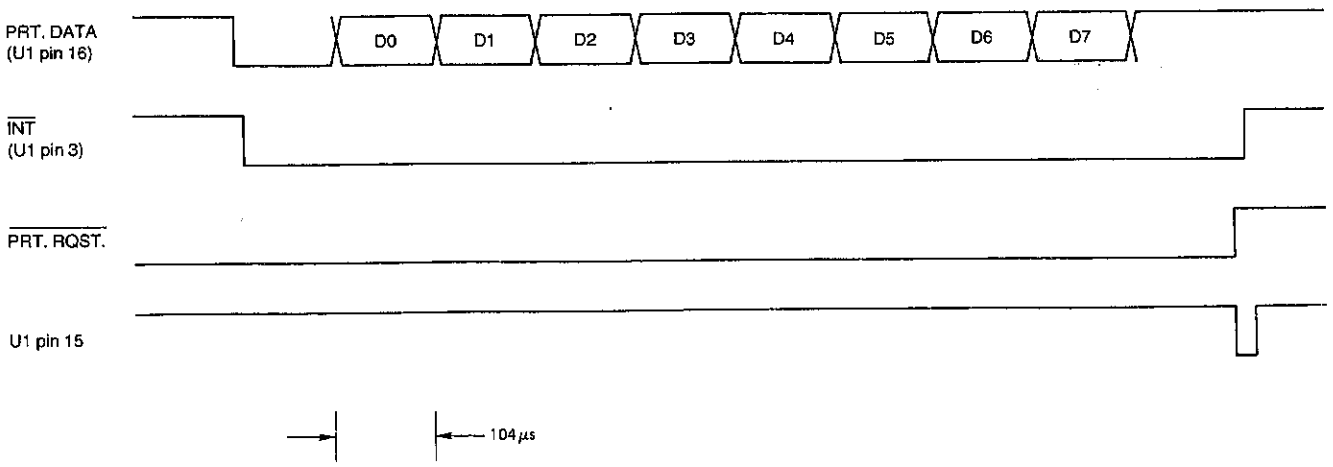


Figure 5.4.13 Internal Printer Interface Timing

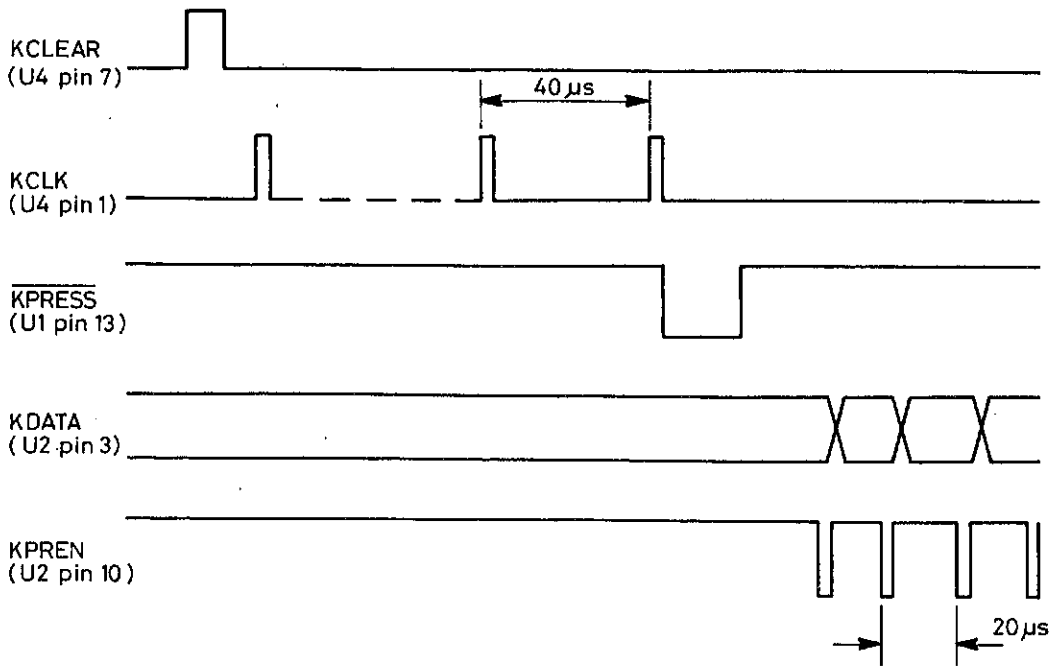


Figure 5.4.14 Front Panel Switch Scan Timing

Table 5.4.4 Front Panel Switch Assignments

Switch No.	Function
S1	CH1 Var Cal/Uncal
S2	CH2 Var Cal/Uncal
S3	CH3 Var Cal/Uncal
S4	CH4 Var Cal/Uncal
S5	X Var Cal/Uncal
S6	0
S7	1
S8	2
S9	3
S10	4
S11	5
S12	6
S13	7
S14	Add (CH1 + CH2)
S16	Add (CH3 + CH4)
S17	8
S18	9
S19	Auto Setup
S21	X Mag
S22	Select Trace
S23	Hold
S24	Lock/Unlock CH1
S25	Lock/Unlock CH2
S26	Lock/Unlock CH3
S27	Pre-Trig
S28	Lock/Unlock CH4
S29	Plot
S30	Refr/Roll/X-Y
S31	Store/Non-store
S32	S/Shot
S33	Continuous
S34	Trigger Source
S35	Trigger Coupling
S36	Auto/Norm
S37	+/−
S38	CH1 AC/Gnd/DC
S39	CH1 Off/Norm/Inv
S40	CH2 AC/Gnd/DC
S41	CH2 Off/Norm/Inv
S42	CH3 AC/Gnd/DC
S43	CH3 Off/Norm/Inv
S44	CH4 AC/Gnd/DC
S45	CH4 Off/Norm/Inv
S50	CH1 Y Position
S51	CH1 Attenuator Range
S52	CH2 Y Position
S53	CH2 Attenuator Range
S54	CH3 Y Position
S55	CH3 Attenuator Range
S56	CH4 Y Position
S57	CH4 Attenuator Range
S58	Time/Division
S59	X Position
S60	Datum Left/Right
S61	Delay S62 Datum Up/Down
S63	Trigger Band
S64	Cursor Left/Right
S65	Trigger Level

44 Front Panel Variable Controls

This circuit consists of:

U7, S1 to S5, R16, R18, R20, R22, R24 and associated discrete componets

These components can be found on the front panel PCB.

The five front panel potentiometers, Channels 1 to 4 Y variable controls and the realtime X variable, affect the scaling of the Y and X signals. When switches S1 to S5 are closed these pots are in their calibrated positions. U7 enables the microprocessor to read the status of these switches.

Measurements:

U7 pin 1	0V Y1 Var uncalibrated
U7 pin 1	5V Y1 Var calibrated
U7 pin 3	serial data out
U7 pin 10	serial data clock

45 Calibrator

This circuit consists of:

U60, Q60 and associated discrete components

These components can be found on the front panel PCB.

This circuit produces the 1V calibrator signal. The circuit consists of an oscillator operating at 1kHz, an output buffer and a potential divider.

Measurements:

U60 pin 3	0V/12V	1kHz squarewave
Q60 collector	0V/12V	1kHz squarewave
P60	0V/1V	1kHz squarewave

46 Front Panel LED Drivers

This circuit consists of:

U5, U6 and associated discrete components

These components can be found on the front panel PCB.

These ICs extract the information about which LEDs should be on or off from the serial bus. The preset intensity of the LEDs is controlled by R26 and R28.

Table 5.4.5 Front Panel LED Assignments

LED No.	Function
D1	Refr
D2	TVL
D3	Roll
D4	X-Y
D5	Non
D6	Store
D7	TVF
D9	Stor'd
D10	Arm'd
D11	Add (CH1 + CH2)
D12	CH1 DC
D13	CH1 Gnd
D14	CH1 AC
D15	CH1 Inv
D16	CH1 Norm
D17	CH1 Off
D18	CH2 DC
D19	CH2 Gnd
D20	CH2 AC
D21	CH2 Inv
D22	CH2 Norm
D23	CH2 Off
D24	Line (trigger)
D25	CH3 (trigger)
D26	CH1 (trigger)
D27	Ext (trigger)
D28	CH4 (trigger)
D29	CH2 (trigger)
D30	On (hold)
D31	AC
D32	DC
D33	ACLP
D34	DCLP
D35	CH3 DC
D36	CH3 Gnd
D37	CH3 AC
D38	CH3 Inv
D39	CH3 Norm
D40	CH3 Off
D41	Norm
D42	Auto
D43	-
D44	+
D45	+/–
D46	Add (CH3 + CH4)
D47	CH2 (Lock/Unlock)
D48	CH4 DC
D49	CH4 Gnd
D50	CH4 AC
D51	CH4 Inv
D52	CH4 Norm
D53	CH4 Off
D54	Trigd
D55	X Mag On
D56	CH3 (Lock/Unlock)
D57	CH4 (Lock/Unlock)
D58	Var (Pre-Trig)
D59	50%
D60	10%
D61	CH1 (Lock/Unlock)
D62	Plot On
D70	Power On

47 RS423 Option

This circuit consists of:

U1 to U8 and associated discrete components

These components can be found in the RS423 interface pod on the rear panel assembly.

This circuit comprises two sections: the UART, U1, and its drivers, and the RS423 program ROM, U7, and its associated address decoding logic. The UART controls the transmission and reception of data, its format, baud rate and the interface protocol. The ROM contains the extra software required to drive the interface and service the commands received from it.

Measurements:

U2 pin 7	RX1 data at RS423 levels
U2 pin 5	RX1 data at TTL levels
U1 pin 26	TX1 data at TTL levels
U3 pin 14	TX1 data at RS423 levels
U1 pin 5	16x Baud rate clock out, TTL
U1 pin 39	pulsed low on micro. access to the UART
U6 pin 9	rising edge, select new ROM page
U7 pin 20	pulsed low on micro. access to ROM

48 GPIB (IEEE488) Option

This circuit consists of:

U1 to U7 and associated discrete components

These components can be found in the GPIBinterface pod on the rear panel assembly.

This circuit comprises two sections: the GPIB controller, U1, and its drivers, and the GPIB program ROM, U5, and its associated address decoding logic. The GPIB controller takes care of the transmission and reception of data, the handshaking and the interface protocol. The ROM contains the extra software required to drive the interface and service the commands received from it.

Measurements:

U1 pin 6	1MHz micro. E clock
U1 pin 3	pulsed low on micro. access to the GPIB controller
U4 pin 9	rising edge, select new ROM page
U5 pin 20	pulsed low on micro. access to the ROM

49 160 Processor Interface

This circuit consists of:

U1 to U7, Q1, Q2 and associated discrete components

These components can be found in the 160 interfaoe pod on the rear panel assembly.

In addition to interfacing the Keypad to the 1604 this circuit includes an extra program ROM, some extra battery backed-up RAM and a Real Time Clock.
The ROM contains the extra software required to drive the Keypad interface and service the instructions received from it. The extra RAM allows reference traces to be saved and recalled for later use, even after power down.

U1	page selection and address decoding
U2	program ROM
U3	battery backed-up RAM
U4	battery backed-up RAM
U5	Real Time Clock
U6	miscellaneous functions
U7	address decoding

Measurements:

U1 pin 9	rising edge, select new ROM/RAM or new page
U3 pin 28	5V normal operation
U3 pin 28	4V power off
U6 pin 3	1MHz micro. E clock
Q1 base	4.4V power on
Q1 base	0V power off
Q2 base	0.7V power on
Q2 base	0V power off

50 Keypad

This circuit consists of:

U1, U2, S1 to S26 and associated discrete components

These components can be found in the hand held keypad unit.

The switch matrix is scanned by U1, which also transmits the data in serial format to the keypad interface.

Measurements:

U1 pin 5	3.68MHz clock, TTL level	
U1 pin 6	9.60kHz clock, TTL level	
U1 pin 8	serial data out	
U1 pin 4	0.2V	select row 0
U1 pin 4	4.8V	row 0 not selected
U1 pin 9	0.2V	column 0 active
U1 pin 9	4.8V	column 0 inactive

Table 5.4.6 Keypad Switch Assignments

Switch No.	Function
S1	Inc
S2	Dec
S3	Datum up
S4	Max/Min
S5	Rise/Fall
S6	RMS
S7	Position Datum
S8	Select Trace
S9	Cursor right
S10	TV Mode
S11	Capture & Repeat
S12	Capture
S13	Y Mag
S14	Restore
S15	F
S16	Datum left
S17	Datum right
S18	Datum down
S19	Save Lower Limit
S20	Save Upper Limit
S21	Test Limit
S22	Set Average
S23	Frequency
S24	Area
S25	Cursor left
S26	Filter

51 Internal Plotter Option

This assembly consists of two printed circuit boards and a printer mechanism. The larger of the two boards contains all the control logic and drive circuits. The control is performed by a dedicated microprocessor, a programmed 6801, which receives data from the 1604 processor via a TTL level serial link, see circuit block 41.

All character generation, line drawing, pen selection and general graphics are controlled by U1, which produces the necessary voltage levels and pulses to drive the printer mechanism. These signals are buffered by U2 to drive the X and Y stepper motors, and by the discrete circuit to drive the pen up/down solenoid.

See Figure 5.4.13 Internal Printer Interface Timing

Measurements:

U1 pin 16	TTL level serial data
U1 pin 13	0V ready for data
U1 pin 13	+5V busy
U1 pin 2	0V power-on reset

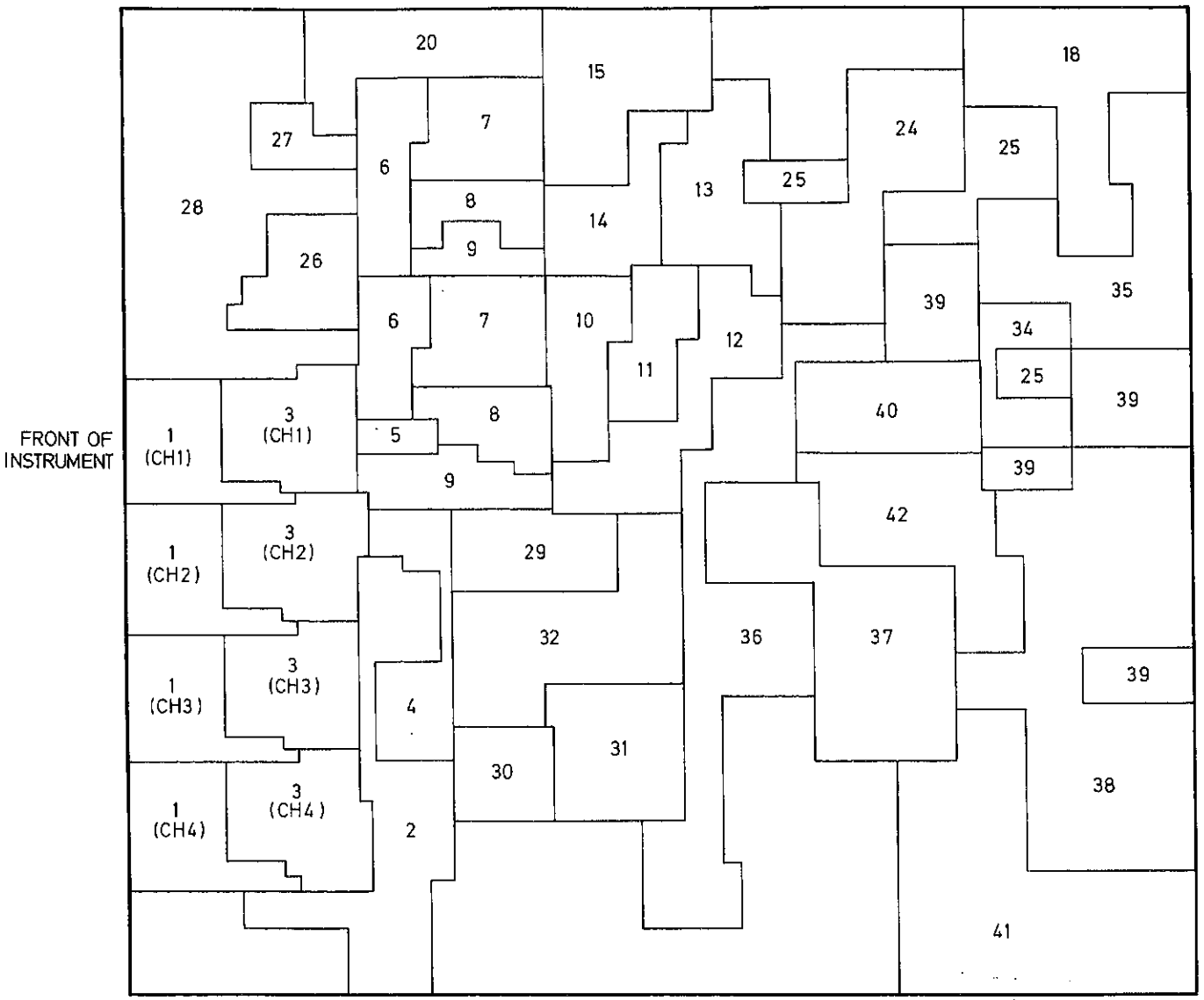
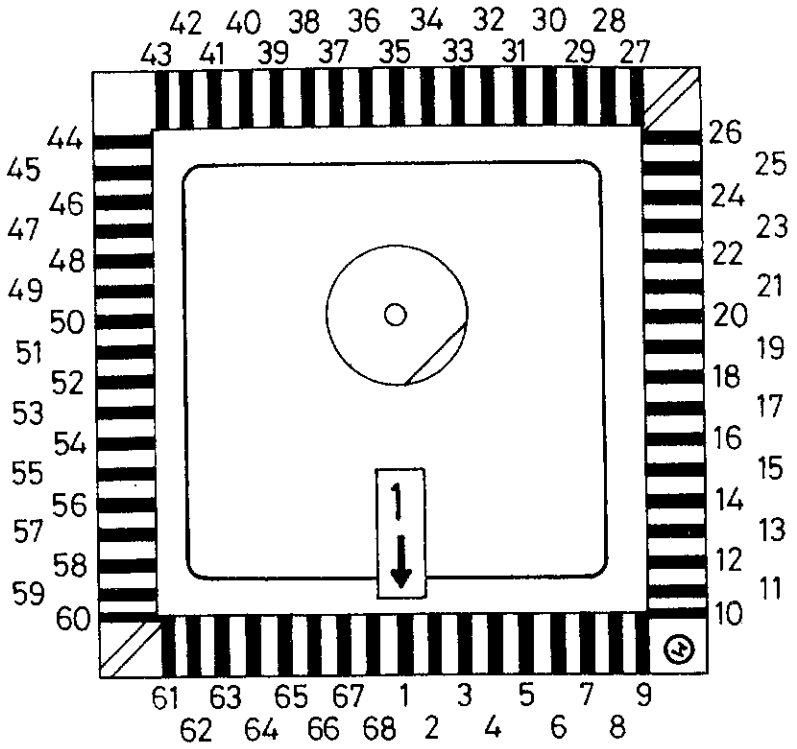


Fig. 6.1 Main PCB Circuit Block Areas



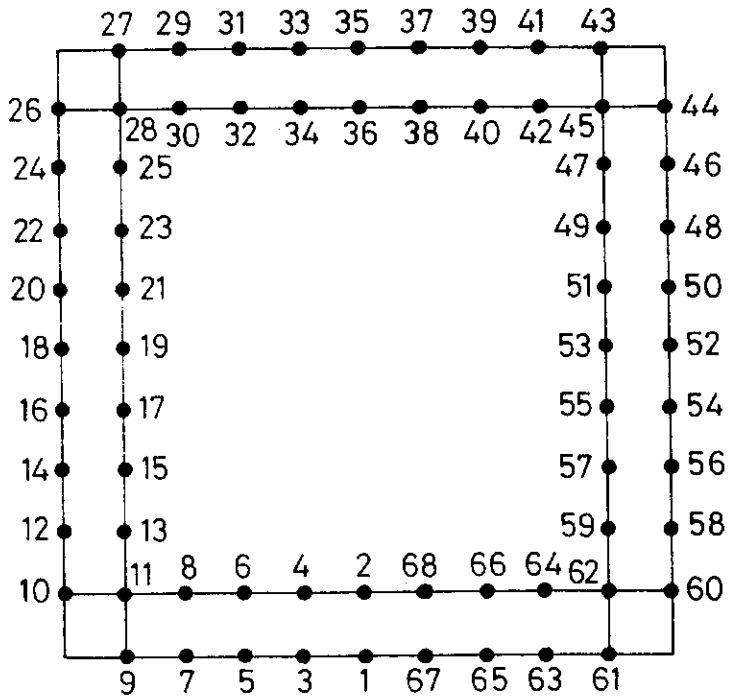


Fig. 6.2 68 Pin PLCC Socket Numbering

MAIN BOARD 1604

Cir Ref	Description	Tol%+/-	Rating	Grid	Part No.
RESISTORS					
R2	1k	5	1/8W	C10	44226
R3	4k7	5	1/8W	E8	44232
R4	47k	5	1/8W	E8	44242
R5	100k	1	1/8W	F7	455476
R6	10k	5	1/8W	E8	44235
R7	10k	5	1/8W	F3	44235
R8	10k	5	1/8W	E3	44235
R9	10k	5	1/8W	D3	44235
R10	3k3	5	1/8W	C9	43358
R11	10k	5	1/8W	C9	44235
R12	270R	5	1/8W	G6	43716
R13	1k	5	1/8W	E6	44226
R14	10k	5	1/8W	E12	44235
R15	3k9	5	1/8W	E12	44231
R16	2k7	5	1/8W	E11	44230
R17	3k9	5	1/8W	E11	44231
R18	1M	5	1/8W	E12	44258
R19	4k7	5	1/8W	A3	44232
R20	10k	5	1/8W	B14	44235
R21	2k2	5	1/8W	D6	43357
R22	10k	5	1/8W	A13	44235
R24	270R	5	1/8W	D10	43716
R47	1k	5	1/8W	D6	44226
R48	100R	5	1/8W	E5	43150
R49	2k2	5	1/8W	F5	43357
R73	10k	5	1/8W	G6	44235
R74	10k	5	1/8W	G8	44235
R75	3k3	5	1/8W	G8	43358
R76	3k3	5	1/8W	G8	43358
R77	10k	5	1/8W	E11	44235
R79	10k	5	1/8W	E10	44235
R80	10k	5	1/8W	E9	44235
R81	150R	5	1/8W	G11	43714
R100	100R PCP			07	455932
R102	680R	5	1/8W	07	44224
R103	680R	5	1/8W	07	44224
R104	68R	5	1/8W	08	43148
R105	33R	5	1/8W	07	43144
R107	220R	5	1/8W	N6	43359
R108	1M	5	1/8W	M6	44258
R109	10R	5	1/8W	M6	43138
R110	10R	5	1/8W	M7	43138
R111	50R PCP			M6	455931
R112	47R	5	1/8W	K3	43146
R114	470R	1	1/8W	L3	455420
R115	470R	1	1/8W	L3	455420
R116	2k7	1	1/8W	K2	455438
R117	2k7	1	1/8W	K2	455438

Cir Ref	Description	Tol%+/-	Rating	Grid	Part No.
R118	1k8	1	1/8W	N6	455434
R119	10R	5	1/8W	J2	43138
R120	10R	5	1/8W	K3	43138
R121	1k	5	1/8W	L2	44226
R122	1k	5	1/8W	L2	44226
R123	270R	5	1/8W	M6	43716
R124	10R	5	1/8W	J2	43138
R125	910R	1	1/8W	M6	455427
R126	910R	1	1/8W	M6	455427
R127	10k	5	1/8W	N6	44235
R129	12k	5	1/8W	K2	43246
R130	68R	1	1/8W	K2	455400
R131	100R PCP			K2	455932
R132	150R	5	1/8W	K2	43714
R133	3k	1	1/8W	K2	455439
R134	2k7	1	1/8W	K2	455438
R135	100R	5	1/8W	J3	43150
R136	100R	5	1/8W	J3	43150
R137	47R	5	1/8W	J3	43146
R138	47R	5	1/8W	J3	43146
R139	680R	5	1/8W	J2	44224
R140	470R	5	1/8W	J2	44222
R141	5k6	5	1/8W	J2	44233
R142	4k7	5	1/8W	K3	44232
R143	470R	5	1/8W	J3	44222
R144	1k	5	1/8W	J2	44226
R145	10R	5	1/8W	L4	43138
R146	10R	5	1/8W	L6	43138
R147	22R	5	1/8W	L3	43142
R148	4k7	5	1/8W	K3	44232
R149	22R	5	1/8W	L3	43142
R150	1k	5	1/8W	L13	44226
R151	22R	5	1/8W	K4	43142
R152	910R	1	1/8W	J3	455427
R153	100R	5	1/8W	J4	43150
R154	390R	1	1/8W	K3	455418
R155	390R	1	1/8W		455418
R156	2k	1	1/8W	J3	455435
R157	910R	1	1/8W	J3	455427
R158	390R	1	1/8W	J3	455418
R159	390R	1	1/8W	J4	455418
R160	2k	1	1/8W	J3	455435
R161	100R	5	1/8W	J3	43150
R162	680k	5	1/8W	N7	44256
R163	82k	5	1/8W	M7	44245
R164	470k	5	1/8W	K4	44254
R165	1M	5	1/8W	K4	44258
R166	10R	5	1/8W	J2	43138
R167	10R	5	1/8W		43138
R168	10R	5	1/8W		43138
R169	10k	5	1/8W	J4	44235
R170	10k	5	1/8W	J4	44235
R171	47R	5	1/8W	K3	43146
R172	10R	5	1/8W	K14	43138
R173	47R	5	1/8W	K2	43146