DIGITAL STORAGE OSCILLOSCOPE OS4000

Instruction Manual

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Contents

ILLUSTRATIONS

Introduction

Section 1

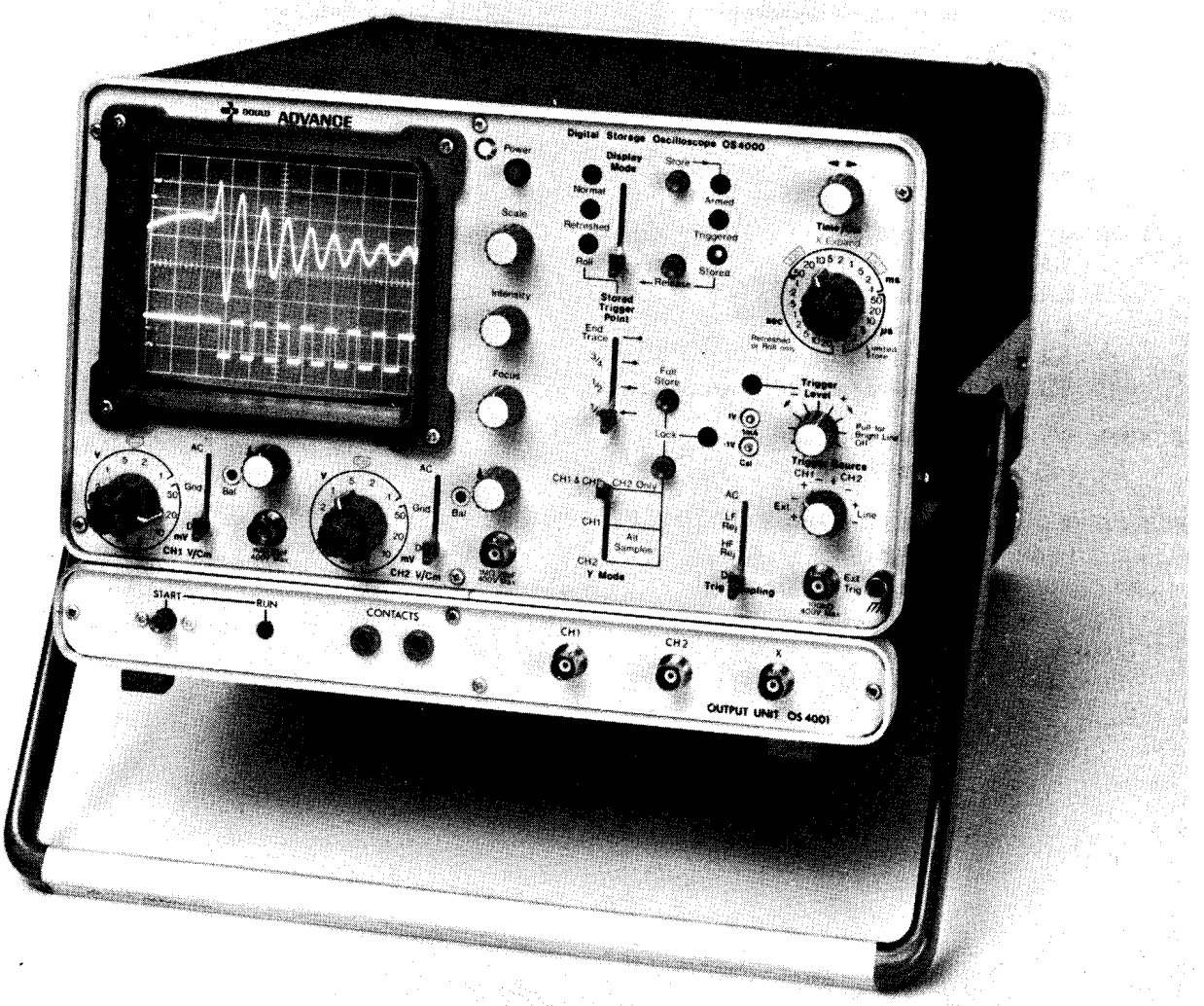
The Gould Advance OS4000 Digital Storage Oscilloscope is a versatile instrument which combines conventional 10MHz oscilloscope performance with a digital storage system, capable of storing signals up to 450kHz. The digital method of storage offers several advantages over the more common tube storage, notably the facility of pre-trigger viewing, the simultaneous viewing of a stored and a real-time display, absence of deterioration of the stored display with time, completely flicker free, low frequency performance, and the abolition of the very expensive storage tube.

Careful attention to the ergonomic design allows the OS4000 to be operated in the same way as a conventional oscilloscope with the addition of the minimum number of additional controls for the storage functions.

APPLICATIONS

The OS4000 is ideally suited for viewing:

1. Transient waveforms, e.g. in Medical, dynamic testing, vibration, pulse testing application.
2. All LF applications where the 'Refresh' mode eliminates flicker. The slowest sweep speed of 200s maximum allows the instrument to be used for new classes of viewing application.
3. Normal (real time) viewing with the 10MHz real time performance.
4. Comparisons between stored and real time waveforms.



Specification

Section 2

DISPLAY
8 x 10 cm rectangular CRT operating at 4kV
Illuminated graticule

VERTICAL DEFLECTION
Two identical input channels

Bandwidth: DC-10MHz in the Normal mode

Sensitivity: 5mV/cm to 20V/cm in 12 ranges
Uncalibrated fine gain control gives between range sensitivity adjustment

Accuracy: ± 3% in calibrated positions

Input Impedance: IM/28pF

Input Coupling: AC-GND-DC

Maximum Input: 400V DC or pk AC

HORIZONTAL DEFLECTION
Timebase: 1μs/cm to 20 sec/cm in 23 ranges

Accuracy: ± 3% X10 ± 5% As instructed over phone by MR MCGREGOR, service eng..

X Expansion: Continuously variable from 1X to 10X with calibrated stops at each end

TRIGGER
Source: CH1±, CH2±, Ext±, or line±

Coupling: AC, LF Rej., HF Rej, DC

Sensitivity: Internal 2mm approx., DC-2MHz (1cm at 10MHz)
External IV approx. DC-2MHz (5V at 10MHz)

Bright Line: Available on normal operation only

DISPLAY VIA STORE
Store size: 1024 x 8 bits

Vertical Resolution: Approx. 200 for 8cm display, i.e. 25 steps per cm

HORIZONTAL RESOLUTION
Single Trace: Approx. 1000 samples for complete scan (100 samples/cm)

Double Trace or Alt. Lock: Approx. 500 samples for complete scan (50 samples/cm)

Maximum Sample Rate: 1.8MHz (0.55μs)

FASTEST RISE TIME
For step response: 0.55μs single trace
1.1μs dual trace or Alt. Lock
(Equivalent Bandwidth 600kHz and 300kHz)

Maximum Storage Frequency – 3 db: 450kHz single trace
225kHz dual trace or Alt. Lock

Limited Store: For timebase speeds faster than 50μs/cm the number of samples per cm is reduced in proportion to the sweep rate. For speeds slower than 50μs/cm the maximum stored bandwidth is reduced in proportion to the sweep rate

Dot Joining: The expanded display appears as straight lines joining consecutive samples rather than as distinct dots

ACCESSORIES SUPPLIED
Handbook PN 36240
2 x Lead PL44 BNC-clip
2 x Lead PL43 BNC-BNC

Supplies: 115V, 220V, 240V ± 10%
45–400Hz, 55W

Size: 17.8 x 31.2 x 41.7 (7" x 12⅜"x 16½")

Weight: Approx. 11 kg (24¼ lb)

Temperature Range: Operating 0 to 50°C
Full spec. 15 to 35°C

OPTION 4001
This add-on option provides analogue outputs to allow the trace to be recorded on strip chart, X Y or T Y recorders and digital outputs for further processing of the recorded data. (See data sheet.)

Operation

Section 3

3.1 SUPPLIES

The instrument is normally despatched from the factory with the supply range switch on the rear panel set to the 240V (± 10%) range. Check that this is set correctly before connecting to the supply. Note that the correct fuse for the two high voltage ranges, 220V and 240V, is 500mA Slo-Blo (20mm) Advance Part No. 33685. If the 115V range is selected the fuse should be changed to a 1A Slo-Blo Advance Part No. 34790.

NOTE:
DO NOT CHANGE THE SUPPLY RANGE SWITCH WITH THE INSTRUMENT CONNECTED TO THE SUPPLY.

While the instrument does not rely on forced air circulation, it should not be operated at elevated temperatures if the natural connection cooling is restricted, particularly at the rear of the instrument.

The instrument is switched on by pressing the POWER button when the associated neon indicator should light. The button is self locking and the instrument is switched off by pressing the button again.

3.2 C.R.T. CONTROLS

These controls are grouped to the right of the c.r.t. display.

Intensity This is used to set optimum trace intensity depending on ambient lighting conditions.

Focus Used to obtain finest possible trace width.

Scale The un-illuminated graticule is easily visible under normal lighting conditions. Graticule illumination is usually only required under low ambient light conditions or when photographically recording the display. The intensity will depend on the film speed, aperture and exposure time being used. The graticule has 0, 10, 90, 100% lines marked to assist in rise time measurement.

3.3 Y CHANNEL CONTROLS

These controls are grouped beneath the c.r.t. display. The input signal is applied to the CH1 or CH2 BNC input socket.

Coupling

For direct connection of the input signal, set the associated AC-Ground-DC input lever switch to DC.

For capacitive coupling of the input signal through an internal 0.1μF 400V capacitor, set the lever switch to AC.

NOTE:
When examining low amplitude a.c. signals superimposed on a high d.c. level, the lever switch should be set to AC and the sensitivity of the Y amplifier increased.

To locate the baseline, set the lever switch to the 'ground' setting. At this setting, the input signal is open circuit and the input of the amplifier is switched to ground.

Sensitivity

Set the VOLTS/CM switch to a suitable setting. To minimise pick up at sensitive settings, it is essential to ensure that the ground lead connection is near to the signal point.
If necessary, adjust the concentric VARIABLE control.

NOTE:
The range of the VARIABLE control is approximately 3.1 so that its full adjustment overlaps the adjacent lower sensitivity range. Except at the CAL setting, the VARIABLE control is uncalibrated. At the CAL setting, the calibration corresponds to the setting of the VOLTS/CM switch.

Shift

For vertical shift of the trace, adjust the Y shift controls (identified with vertical arrows).

Bal.

The preset balance should be adjusted to minimise verticle movement of the CH1 or CH2 traces when the inputs are grounded and the attenuator switch is moved between the 0.5V/cm position and the 0.2V/cm position: This should only be done after a reasonable warm up time of say 15 minutes and should only require infrequent adjustment thereafter.

Y Mode

This three position switch allows single channel display of the selected channel CH1 or CH2, or dual channel display when CH1 & CH2 is selected.

3.4 TIMEBASE AND TRIGGER

All controls associated with the Timebase and Trigger facilities are grouped together on the right hand side of the panel.

Time/cm, Expand and Shift

The timebase sweep speed (i.e. the time scale of the horizontal axis) is determined by the setting of the TIME/CM switch.

X Expand

The time scale can be adjusted to any intermediate setting by use of the concentric X EXPAND control. This provides a calibrated sensitivity at the X1 and X10 detent positions at the ends of travel with a fully variable uncalibrated range between. The X shift control, identified with horizontal arrows is used to centre the display or locate any part of the trace in the expanded condition. This is a dual action control, providing fine adjustment over a small angle of rotation and coarse adjustment over the full rotation.

Trigger

The TRIGGER SOURCE switch selects one of the four signals, internal CH1, internal CH2, External or line.
The TRIG COUPLING selects wideband DC or AC coupling.
The AC coupling cuts off at approx. 1.5Hz.
The L.F. reject position limits the trigger sensitivity below approx. 15kHz while the HF reject is AC coupled

but limits sensitivity above approx. 34kHz. The source switch also selects the slope, positive or negative going, to cause trigger when the signal passes through the level set by the TRIGGER LEVEL control.
The associated L.E.D. indicates when trigger signals are present. This will flash at low repetition rates and remain on at faster rates. However it may not indicate trigger signals above 5MHz.
In the Normal mode of operation, the timebase will free run automatically in the absence of trigger signals. This provides a "bright line" display to assist in trace location. With this facility operating, false triggering may occur if the trigger frequency is less than approx. 40Hz. It is disabled in the Refreshed or Roll modes and can be disabled in the Normal Mode by pulling the Trigger Level Knob.

3.5 STORE CONTROLS

All controls associated with the storage facility are grouped together and distinguished with blue coding. The DISPLAY MODE lever switch selects the three modes of operation NORMAL, REFRESHED or ROLL, the associated L.E.D. indicating the operating mode.

Normal

In this mode the instrument operates as a conventional oscilloscope and the store controls do not influence the display. This mode of operation is available for all medium and fast sweep rates, 0.5s/cm to 1μs/cm, but if slower sweep rates are selected, the instrument operates automatically in the Refreshed mode.

Refreshed

If the instrument is displaying a trace in the Normal mode and the mode switch is moved to REFRESHED, the display essentially will be unchanged. However in this mode and in ROLL, the display is generated via the digital signal path and a small amount of step structure may be detected on the trace. This is visible in the form of small vertical steps, less than ½ mm on slow rising or falling traces. Also with the full X 10 expansion fast rising or falling traces will appear as a series of sloping lines (approx. 10/cm in the X direction) rather than as a smooth curve.
The display is triggered as in the Normal mode but in the absence of trigger the previously stored trace is displayed continuously. This has the advantage of providing a flicker-free display of signals with low repetition or trigger rates even if a fast sweep is selected. The display is updated or refreshed by each trigger signal which would cause a sweep of trace in the Normal mode. A further advantage over Normal operation is the availability of very slow sweep rates with continuous flicker-free display of the sweep as it is written or re-written.
The Refreshed mode can be used over the full range of sweep speeds but as the internal sampling rate is limited to 2MHz, the horizontal sample density decreases in proportion from the normal 100/cm when operating at sweep rates above 50μs/cm.

Roll

Selection of this display mode provides a form of free running time-base not found on a conventional oscilloscope. Incoming data is fed continuously to the store so that the display from the store at any instant is a back history of duration determined by the time/cm speed control. As the display is continuously updated from the right, the trace appears to be moving or rolling to the left similar to the view through a 10cm window of a strip chart recorder trace.
This mode of display is most suited to direct display of low frequency signals using comparatively slow sweep speeds.
As with the Refreshed mode, the Roll mode can be used on all sweep speed ranges but with limited horizontal sample density at the faster sweep rates.

Store and Release

These buttons operate in the Refreshed and Roll modes. Operation of the STORE button in the Refreshed mode retains any current sweep or the next full triggered sweep as a stored display, unaffected by subsequent trigger signals. L.E.D. lamps indicate the single shot sequence followed. The Armed lamp shows that the circuitry has been primed by operation of the button. This lamp goes off and the Triggered lamp comes on during a sweep. Finally this indication is replaced by the Stored lamp coming on when the stored sweep is complete. The sequence and resultant display is similar to operation of the single shot facility on a conventional storage oscilloscope after erasing any previous trace. The OS4000 has no need for an erase facility as the entry of new data into the store automatically rejects previous data.
Even in the Stored mode it is possible to use the X EXPAND control with adjustment of the X shift control for detailed examination of any part of the trace.
Subsequent operation of the Store button will repeat the single shot storage cycle, updating the display as required.
Operation of the Release button will return the instrument to the Refreshed mode of operation.

Pre-Trigger Storage

The effect of operation of the STORE button in the ROLL mode depends on the setting of the STORED TRIGGER POINT SWITCH. With this switch in the top (End Trace) position, the rolling trace will continue after operation of the STORE button until a trigger is received when the display will be frozen. Thus it shows a full trace of signal prior to trigger, i.e. trigger is at the end of the trace, not at the beginning as on a conventional oscilloscope, storage type or otherwise.
Operation of the STORE button at the ¾ trace setting of the STORED TRIGGER POINT switch allows the display to roll on for ¼ of a sweep beyond the next trigger. The resultant frozen display shows ¾ of the trace occuring before trigger and ¼ after trigger.
The actual trigger point on the waveform, ¾ from the

left hand side of the screen, is shown by a bright-up spot. It may be necessary to reduce the Intensity setting to obtain contrast to see this spot.
Selection of the ½ or ¼ trace position of the Stored Trigger Point allows the proportion of pre-trigger display on subsequent storage cycles to be varied accordingly.
The ability to display a trace of the incoming waveform prior to or about trigger, can be used up to sweep speeds of 50μs/cm, irrespective of the trigger rate.
For this function, the Roll mode is advantageous on fast changing signals and at fast sweep speeds. These present a meaningless display which in the free running Roll mode but are relevant when stored.
The X EXPAND facility can be used with the X shift control in this Stored mode for detailed examination of any part of the trace. It should be noted that the bright-up dot actually occurs approx. 0.2% of trace before the actual trigger point and this can be seen as a 2mm difference on X 10 expand.
The Armed, Triggered and Stored lamps associated with the STORE button, operate in the Roll mode similarly to that described for Refreshed. At the End Trace setting, the triggered state is omitted as the display is held in the Stored Mode immediately upon receipt of trigger.
After storage, operation of the RELEASE button will return the function to Roll. Alternatively further operation of the STORE button will return the function to Roll but primed for another storage cycle. In either case previously stored data has to roll out of the store as new data is fed in. A new trigger signal will be accepted only when this mixed display condition has cleared.

Lock Full Store

Operation of the LOCK FULL STORE button prevents change of the data held in the store. It can be used usefully in the Roll mode to freeze the display at once if a feature of interest appears on the screen. Alternatively the store can be locked in the Refreshed or Stored modes. Subsequently the instrument can be used as a conventional oscilloscope in the Normal mode but the original locked display is recalled when returned to the Refreshed mode. The Lock Full Store button latches mechanically. To enable the instrument to update the store as usual the button should be pressed again. An LED indication warns that the Lock Full Store or Lock Alternate Samples button is pressed. It should be noted that movement of function switches after a display has been locked in the Roll mode, can disturb the display, particularly shifting the start point of the trace and the bright up trigger marker spot if relevent. This disturbance is not corrected when the function switch is returned to Roll.

Lock Alternate Samples

All the store functions described above operate irrespective of the setting of the 'Y' Mode switch. This is, they apply equally to the single trace display of CH1 or CH2 and the dual trace display of CH1 & CH2. This is not so for the LOCK ALT. SAMPLES button. When this condition is applied in the Refreshed mode for single trace displays (CH1 or CH2), the effect is to produce a dual trace display. One trace is stored and the other free to follow updating signal inputs. This simultaneous display of stored and the incoming signal can be used to compare 'before' and 'now' traces or even to compare traces taken at different sweep speeds, (once a trace is stored its display is not altered by the setting of the Time/cm switch except above 50μs/cm). Operation of the LOCK ALT. SAMPLES in the dual trace, CH1 & CH2, mode has the effect of freezing the CH2 trace, leaving CH1 free to respond to current signals.
It should be noted that it is possible in this condition to see a narrow vertical transient appearing on the CH2 trace at the point where the CH1 trace is being refreshed. This effect can be removed by switching from CH1 and CH2 to CH1 once CH2 has been frozen.
Once the LOCK ALT. SAMPLES button is pressed, it is possible still to go from Refreshed to Store and then to Release to Refreshed with the free trace following the mode selected, but the frozen trace remaining as when that lock button was pressed. Operation of the LOCK ALT. SAMPLES button in the ROLL mode is less meaningful than in the Refreshed mode. Half of the display is frozen as before, giving a dual trace effect to single channel displays or locking CH2 only on dual trace displays. However the trace continues to move across the screen from right to left with data lost from the left appearing at the right.

3.6 ALIAS EFFECTS

In the Refreshed and Roll modes, the instrument uses a sampling system to examine the incoming waveform. Any such system can give misleading results known as alias effects if the input signal has a significant component with a frequency approaching or above the sampling frequency.
Fig. 1 shows the effect of the sampling process on a triangular input waveform (trace A).
Trace B shows the effect of sampling at a frequency close to four times that of the input if the display is formed by a series of dots. It will be seen that this can become a meaningless jumble. However trace C shows the same sampled waveform reconstructed with the dot joining system employed in the OS4000. Thus the display is formed by a series of straight lines, joining the successive sampled levels rather than a dot at each level, usually used on reconstructed displays. The dot joining approach is seen to retain the essential nature of the input waveform without ambiguity. This is particularly important as the horizontal dot density is much closer than that shown on the diagram. However if the sampling rate is reduced further, the essential nature of the waveform will be lost. Trace D shows the effect of a sampling rate close to half the input frequency and Trace E the effect when the frequencies are nearly equal. In the latter case the display appears as the input form but at reduced frequency. The frequency division is the

principle on which sampling oscilloscopes operate, and can cause confusion in this case.
The OS4000 takes approx. 1000 samples per sweep. These are shared between traces on dual channel or alternate locked modes of operation. Assuming that the sampling rate should exceed the input signal frequency by a factor of between 4 or 5, the following table shows the maximum frequency which can be viewed on each range.

Time/cm Range	Single Channel	Dual Channel or Alt. Locked
50 μs/cm	400kHz	200kHz
0.1ms/cm	200kHz	100kHz
0.2ms/cm	100kHz	50kHz
0.5ms/cm	40kHz	20kHz
1 ms/cm	20kHz	10kHz
2 ms/cm	10kHz	5kHz
5 ms/cm	4kHz	2kHz
10 ms/cm	2kHz	1kHz
20 ms/cm	1kHz	500Hz
50 ms/cm	400Hz	200Hz
0.1 s/cm	200Hz	100Hz
0.2 s/cm	100Hz	50Hz
0.5 s/cm	40Hz	20Hz
1 s/cm	20Hz	10Hz
2 s/cm	10Hz	50Hz
5 s/cm	4Hz	2Hz
10 s/cm	2Hz	1Hz
20 s/cm	1Hz	0.5Hz

At sweep speeds faster than 50μs/cm the sampling rate remains at 1.8MHz and the storage capability is reduced. Thus the usable frequency remains at 400Hz or 200kHz. In practice there is little advantage is using the storage modes above 50μs/cm.
The above table shows the order of frequency which can cause mis-leading displays. The actual amount of distortion depends on both the frequency and the wave-shape involved. Individual peaks of sinusoidal signals can be −3db at a frequency approx. 10% above those shown above.
If alias effects are suspected, it is recommended that the fastest possible sweep speed is selected. Repetitive signals are best viewed in the normal mode if possible, before comparison with a refreshed trace.
It should be noted also that the sampling system will not detect narrow transients which occur between samples.

3.7 ADDITIONAL FACILITIES

Cal

These pins provide d.c. coupled positive-going square waves of 0.1V and 1V ± 2% amplitude at approximately 1kHz frequency for calibration checks, (2kHz when Time/cm set 50μs/cm or faster). Shorting between the CAL pins will produce a square current wave-form of 1mA in the shorting link. This can be used for current probe calibration.

Use of Optional Passive Probe

A x 10 passive probe may be used to extend the voltage range and increase the input impedance of the Y amplifiers. The input resistance of a Y channel is 1MΩ shunted by approximately 28pF. The effective capacity of the input lead must be added to this and the resultant impedance will sometimes load the signal source. Therefore it is advisable to use a 10MΩ, x 10 probe. This reduces the input capacity and increases the input resistance, at the expense of the sensitivity. The probe contains a shunt RC network in series with the input, and forms an attenuator with the input RC of the Y channel. To obtain a flat frequency response it is necessary to adjust the capacitance of the probe to match the input capacity of the Y channel as follows:-

1. In the Normal Mode, set the Y channel VOLTS/CM switch to 20mV/cm, and the TIME/CM switch to .2ms/cm.
2. Connect the probe to the CAL 1V pin.
3. Set the adjustable capacitor in the probe tip or termination with a small screwdriver for a level response with no overshoot or undershoot visible on the display.

3.8 FUNCTIONAL CHECKS

This section describes a test routine which checks that the instrument is functioning correctly in its main modes of operation, but it also provides examples of how to set and use the instrument.

Normal Mode

Switch on, put Display Mode switch to normal.
Put timebase switch to 1ms/cm; CH1 and CH2 attenuators to 0.2V/cm; Trigger Lever Control knob pushed in; CH1, CH2 and X shift controls central; Y Mode switch to CH1 & CH2; Input coupling switches to GND; Trigger source switch to CH1; Trigger Coupling to A.C.
Turn Intensity control to clockwise end. Adjust CH1 and CH2 shift controls to obtain two traces. Adjust Intensity and Focus control to obtain finest possible traces.
Rotation of the Trigger Level control through the central position will cause trigger L.E.D. to flash once.
After about 15 mins. warm up, check that on both channels the vertical trace movement caused by turning the attenuator switches from 0.2V/cm to 0.5V/cm is less than 0.5cm. If not adjust the BAL. pre-set for that channel. Set input coupling switch to DC.
Apply sine wave at approx. 1kHz to CH1 and select CH1 as trigger source. Adjust CH1 attenuator and/or signal amplitude to give about 5cm Y deflection. Adjust level control to obtain stationary trace – check trigger L.E.D. is illuminated. Pull out Trigger level control to disable Bright Line facility and turn until trigger is lost; trace should disappear. Trace should re-appear free running when Level control is pushed in. Reset Level control for stationary trace.

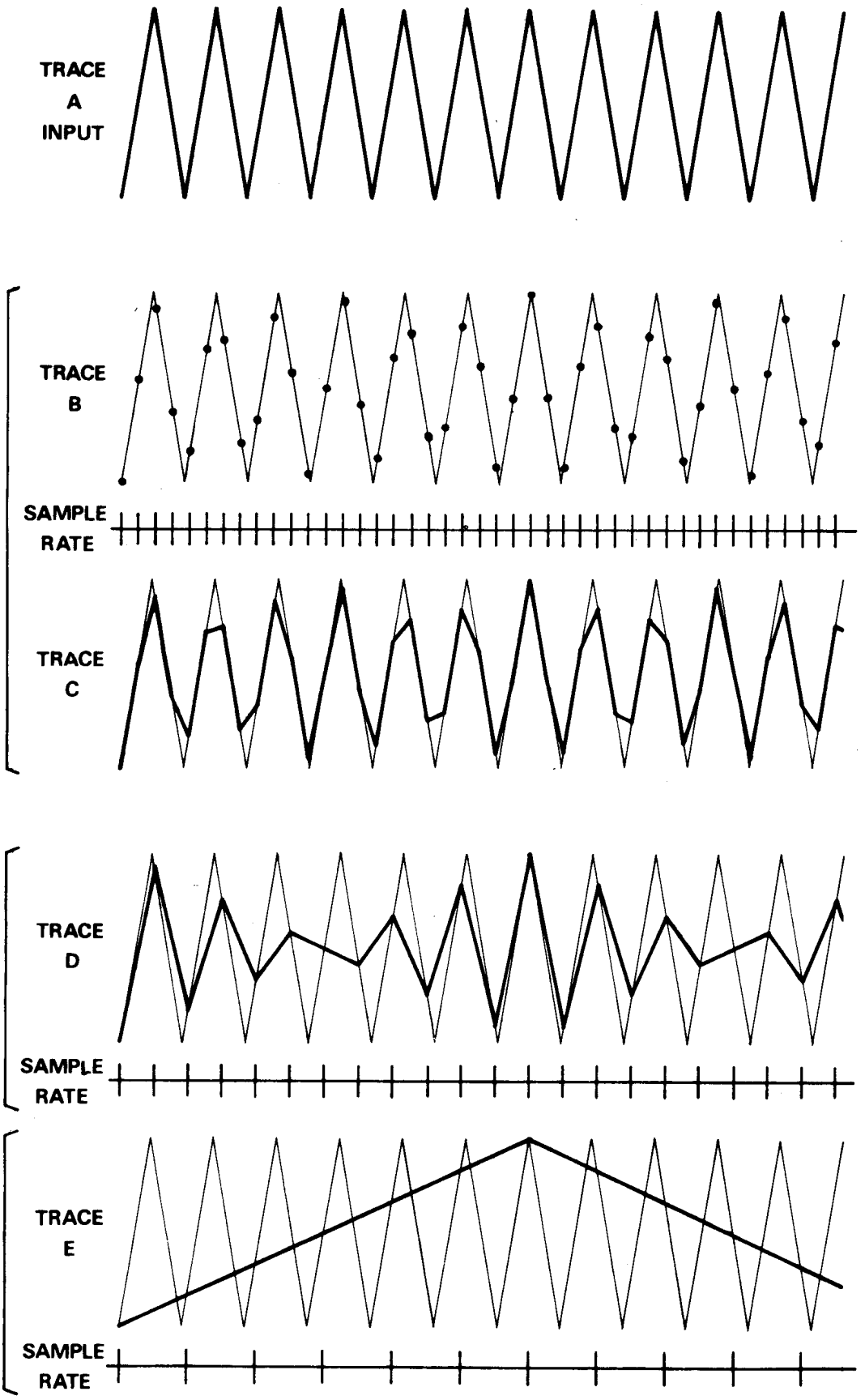


Fig. 1 Alias Effects

Refreshed Mode
Apply approx. 1kHz with the timebase on the 0.5ms/cm range. Obtain a stable display. Switch the Display mode to Refreshed. The Display is now being obtained from the store. Removal of the signal by disconnecting the input or switching the input coupling switch to the GND will cause the last "sweep" to be preserved in the store and displayed indefinitely. This sweep may include the break of signal. Apply a 1 to 10 Hz sine wave and adjust the timebase range switch accordingly. Adjust the level control to light the trigger L.E.D. The refreshing sweeps through the store can be clearly seen as the timebase range is switched up or down.

Store
If the signal is removed and the Store button pressed, on re-applying the signal the sequence-trigger-store can be followed by watching the status indicators, and the store will have been completely updated when the store L.E.D. is lit. The sequence may be repeated by pressing the Store button again.

Lock Full Store
Select CH1 only, with CH1 as trigger source. Apply approximately 1kHz signal and adjust the Trigger Level so that refreshing sweeps are occuring. Push Store button and when the store L.E.D. is lit, push the Lock Full Store button. On returning the Display mode switch to the normal position, conventional oscilloscope operation is possible – i.e. the input attenuators and timebase range can be altered, another signal can be observed, but on returning the mode switch to the Refreshed position, the original stored display will be obtained, irrespective of the current input and setting of the sensitivity and sweep speed controls (50μs/cm or slower). Release the Lock button.

Lock Alt. Samples
With the display mode switch in the refreshed position again, apply the same signal as before and adjust trigger level to obtained refresh sweeps. Store the trace then press the Lock Alt. Samples button. On returning to the refreshed mode (pushing Release button) it will be found that operating the CH1 shift control, results in two traces being generated – one which responds to the input signal, shift, attenuator and timebase controls, the other a fixed display of the original store contents. On uplatching the Lock ALT. Samples button a single trace is again displayed.

Select CH1 & CH2 (Dual trace), CH1 trigger, and apply approximately 1kHz signals to CH1 and CH2. Adjust trigger level so that refresh sweeps are occuring. Push Store button and wait for store L.E.D. to light. If the Lock Alt. Samples button is operated on returning to the refreshed mode, one trace (CH1) will respond to the CH1 shift and input signal, the other trace (CH2) is locked. Returning to the normal mode will not destroy the CH2 information held in the store until the Lock Alt. Samples button is un-latched.

Roll Mode
Switch display mode to Roll. Select a low sweep speed such as 1 sec/cm. Select CH1 only. Offset trigger level to one end, and check Hold and store L.E.D.'s are off. Movements of the CH1 shift control will now be seen to draw a trace on the screen similar to a strip chart recorder, with the "pen" at the right hand side of the screen, and the trace moving towards the lift at the sweep speed selected. This movement can be arrested at any time by pressing the Full Lock button.

Pre-trigger Storage
Apply a low frequency signal of approximately 1Hz and with trigger coupling in the D.C. position adjust the trigger level control until the trigger source L.E.D. flashes continuously. The display will continue to move to the left. Remove the signal and press the Store button. On re-applying the signal the sequence, triggered-stored will be followed resulting in a stationary display. The length of time spent in the triggered condition and therefore the final waveform position is dependent upon the setting of the stored trigger point switch, and can be changed from zero to three quarters of the full sweep time. At normal to low settings of the brilliance control a bright dot can be observed marking the point of trigger (it is displaced approximately 0.2 cm on X10 expansion to the left of the true trigger point). After a stationary display has been obtained, if the signal is not removed, but its frequency is changed by say 2:1, on pressing the store button again, the sequence, triggered-stored will be followed, resulting in a stationary display again. It will be found that the new display contains none of the "old" frequency, because the store will automatically take in just enough new information before becoming sensitive to trigger such that the next stored waveform consists of new information entirely.

4.1 SYSTEM DESCRIPTION

With the MODE switch in the NORMAL position the instrument operates in a conventional manner. Referring

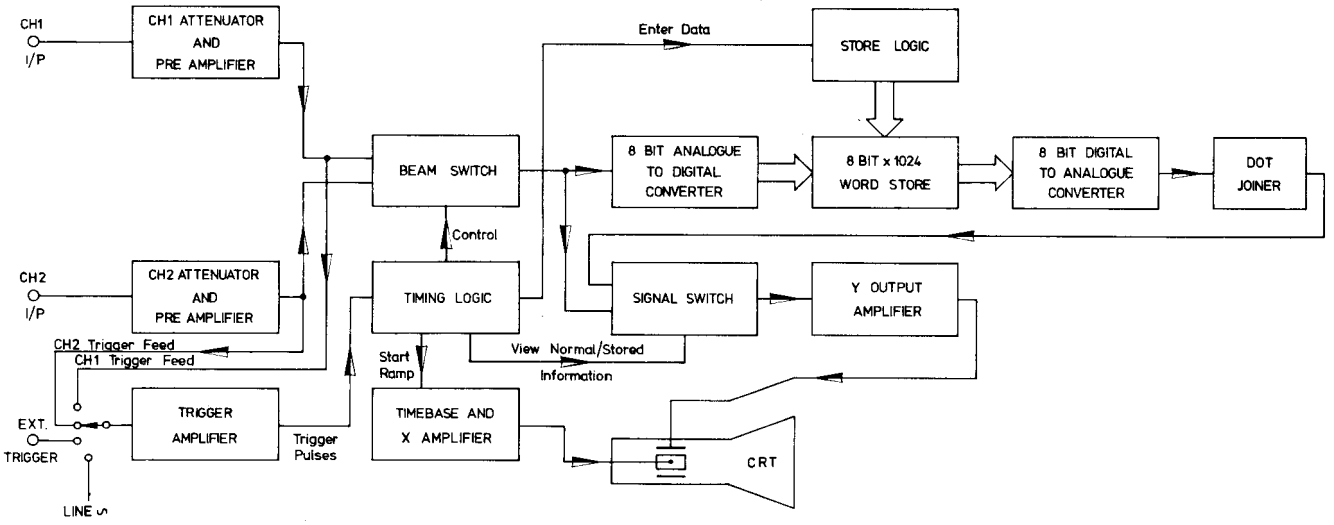


Fig.2 Block Diagram of Instrument

to fig.2., input signals are applied to two identical pre-amplifiers which incorporate the sensitivity controls, both variable and switched, and also the Y shift and input coupling controls. The outputs of these pre-amplifiers are applied to the beamswitch and also to the trigger selector switch. The beamswitch selects one or other of the two channels and on dual trace, is operated either in a chopped or alternate sweep mode, dependent on the setting of the timebase range switch. The output of the beamswitch is applied via the signal switch to the Y output amplifier which drives the vertical deflection plates of the c.r.t. A trigger signal is selected by the trigger selector switch and shaped into fast pulses by the trigger amplifier which contains the trigger level, slope and coupling controls. These trigger pulses are supplied via the control logic to the timebase and initiate a linear ramp, the duration of which is determined by resistors and capacitors switched by the timebase range switch in the usual manner. This ramp is applied via the X amplifier to the horizontal deflection plates of the c.r.t. A bright line facility is available such that when no trigger signal is being received, the timebase is made to free run, producing a visible base line.

When the MODE switch is in the REFRESHED position, the signal switch is changed over so that the output from the Dot Joiner is routed to the Y output amplifier.

Analogue signals from the beamswitch are applied to the Analogue to Digital Converter (ADC) which produces an 8 bit binary code (word) representing the instantaneous signal level at 550 nanosecond intervals.

The data produced by the ADC can be loaded into a store under the control of the timing logic. The store can hold 1024 such 8 bit words and the data is entered at a rate such that the information contained in the whole store represents one complete sweep. This data is then continuously read out (non-destructively) at a fixed rate and reconstituted as an analogue signal by the Digital to Analogue Converter (DAC), and applied to the Y output amplifier to give a continuous display of the store contents. Since the output from the DAC is in the form of discrete levels, a dot joiner is included to join up these levels and provide a continuous display.

The timebase section provides continuous sweeps at a fixed rate of 100μs/cm irrespective of the setting of the timebase switch, and synchronised to the store read out cycle.

Note that the trigger amplifier is now entirely dissociated from the timebase since the latter is running continuously. The function of the trigger amplifier is to initiate a read-in cycle, when a screen full of new information will be entered into the store. The rate at which new data is entered determines the effective timebase rate of the viewed signal; the 1024 available store locations represent approximately 11.3 cms. of trace length, thus there are 91 samples per cm. A data entry rate of 0.91 MHz would correspond to 100μs/cm. and 91 Hz to 1s/cm. and so on.

The data entry rate is determined by a programmable digital divider controlled by the timebase range switch. This divider operates on the basic clock frequency of 1.82MHz which corresponds to 50μs/cm, the fastest sweep rate available in the digital mode.

Dual trace operation in the REFRESH mode is catered for by operating the beamswitch in the chop mode at half the data entry rate, thereby storing samples of each trace in alternate store locations. Since the store is being read out at a relatively fast rate, however, the alternate sweep technique is used during read out, with store

locations relevant to one trace being read out on one sweep, and the remaining location on the next sweep. The STORE control provides a conventional single shot facility to enter one triggered sweep of data into the store, while the LOCK STORE controls inhibit immediately the entry of any new data.
The ROLL mode of operation is similar to the REFRESHED mode except in the way in which new data is entered into the store. Instead of waiting for a trigger pulse to initiate a new data input cycle, data is continuously entered into the store. Thus, if data entry is made to stop on receipt of a trigger pulse, the contents of the store will be information stored before the trigger pulse, rather than after it as in a conventional trigger sequence. To expand this facility, which operates only in conjunction with the single shot store controls, a switched delay is incorporated marked STORED TRIGGER POINT which allows the input of new data to continue after a trigger is received, for a time corresponding to ¼, ½ or ¾ of the store length. This allows the amount of pre-trigger and post trigger information retained in the store to be varied to suit the application.

Circuit References
Each component in the instrument is specified by a circuit reference consisting of a letter prefix and a number. The number also indicates which printed circuit board assembly the component is mounted on as shown below:-

Circuit Reference No.	
0 – 99	Main Frame Components
100 – 399	Analogue to Digital Converter Assembly
400 – 499	E.H.T. Board
500 – 599	Power Supply Board
600 – 699	Store Logic Board
700 – 799	Timing Logic Board
800 – 899	Output Unit 4001 – Fitted as an option. See separate handbook for details.
900 – 1099	Timebase Board.

The location of the various assemblies is shown in Figs.14, 15 and 16.

4.2 POWER SUPPLIES

4.2.1 GENERAL
Referring to Fig.20 all the power supplies for the instrument are derived from the transformer, T51. Two tapped primary windings are switched by S52 to allow for three supply voltage ranges and fuse FS51 provides fault protection. The supply indicator neon, NE 51, is supplied via limiting resistor R58 from the 115 volt tap on the transformer.

4.2.2 LOW VOLTAGE SUPPLIES
Five separate secondary windings supply bridge rectifiers, BR51–BR55, mounted on the transformer and provide unregulated supplies of +170V, +26V, –26V, +18V, –10V and +8V across the reservoir capacitors, C509A, C510, C511, C512, C502 and C51, respectively. Note that the –10V and +8V supplies are floating with respect to ground due to the action of the regulators. The +170V supply is further smoothed by R540 and C509B and protected by fuse, FS501. The + 26V, –26V, + 18V and –10V supplies are fed to high performance integrated circuit regulators, IC503, IC504, IC501 and IC502 respectively to provide stabilised lines of +20V, –20V, +12V and –6V. These devices contain all the circuitry necessary for a conventional series regulator, together with current limiting and thermal shutdown facilities to protect the device against overloads arising from short circuits, etc. Note that the two 20V lines are in fact provided by 15V regulators in conjunction with zener diodes, D503 and D504.
The +8V supply feeds a discrete series regulator comprising transistors, TR505–TR510, and associated components, to provide a stabilised +5V line. The long tailed pair, TR505 and TR506, compares the output voltage with the voltage across the zener diode, D505, and provides an error signal which is passed via the emitter follower, TR509, to the series pass transistor, TR510. A second long tailed pair, TR507 and TR508, senses the voltage drop across the current sensing resistor, R522, and if the supply current rises above 3 amps will shut down the regulator by reducing the reference voltage at the base of TR505. The resistor network, R518, R517 and R520, determines the limiting current and also provides a 'foldback' limiting characteristic by reducing the permissible output current of the regulator as the output voltage falls. This prevents excess dissipation in the series pass transistor under short circuit conditions. The zener diode, D506, prevents the output voltage of the regulator rising excessively high under fault conditions and thus protects from damage the integrated circuits supplied from this line.

4.2.3 E.H.T. SUPPLIES
The two remaining secondary windings are associated with the cathode ray tube (c.r.t.) supplies. The 6.3V winding feeds the c.r.t. heater and the 850 volt winding provides the –1kV and the +3kV supplies. Stabilisation of both lines against supply voltage variations is achieved as follows. One end of the 850V winding feeds the rectifier diodes in the normal manner, the other end passes to ground via a bridge rectifier, BR401. The alternating current in the winding passes through R406 and TR402 as direct current developing a steady voltage across C402. This voltage, controlled by the conduction of TR402, is effectively subtracted from the peak voltage available at the 'hot' end of the winding and thus by varying the base-emitter voltage of TR402, the rectified high voltage supplies can be controlled. The average value of the base-emitter voltage of TR402 is established by the voltage at TR403 emitter. This in turn is controlled by the voltage at TR403 base set by the feedback resistor, R411, from the –1kV supply line and the combination of R409 and R410, thus establishing a closed feedback loop. A small current also flows from the base of TR403 via R407

to the unregulated −26V supply. Since this voltage changes with the line voltage, this trims out any remaining fluctuations in the E.H.T. supplies due to supply variations. The −1kV supply is derived by the diodes, D404, D405 and D406, feeding the reservoir capacitors, C404, C407 and C406. The voltage is smoothed by R413, R414 and C405, C408 and C409 and applied to the grid of the c.r.t. The cathode potential of the tube is held positive w.r.t. the grid as determined by the brilliance control, R419, and the second anode potential is set by R416 to optimise the focus. Small positive voltages set by R417 and R408 are applied to the third anode and interplate shield to minimise raster distortion.

4.2.4 GRATICULE ILLUMINATION

The graticule is illuminated by two lamps, ILP1 and ILP2. The supply for these lamps is derived from the emitter follower, TR401, and controlled by the potentiometer, R402. This circuit is supplied from the 8 volt winding of the transformer via diodes, D53 and D54.

4.2.5 THE TRACE ROTATION COIL

A coil, L51, fitted round the neck of the c.r.t. inside the magnetic shield, is used to align the trace with the horizontal graticule lines. The current for this coil is taken from the pre-set potentiometer, R529, through R530 on the power supply board. The direction of rotation can be reversed by interchanging the coil connections at the power supply board.

4.3 THE Y AMPLIFIER

4.3.1 THE Y PRE-AMPLIFIER

The attenuator and pre-amplifier in Channel 1 are identical to those in Channel 2. Accordingly only Channel 1 will be described. Referring to Fig.21 the input signal is applied to the front panel socket, SKV, and then to the 3 position lever switch, S1, via R22. This switch selects AC or DC input coupling by including or by-passing C20 in the signal path. On the middle position of the switch, the input socket is disconnected and the input to the amplifier is connected to ground. Input sensitivity selection is performed in two stages; the six lowest ranges, 5−200mV/cm, are obtained by switching the gain of the amplifier as described later. The 0.5−20V/cm ranges are provided by switching in a ÷100 attenuator section before the amplifier and repeating the gain switching. This attenuator is formed by R24 and R351 with C305 to set the h.f. response. C303 is adjusted to maintain the total input capacitance of the highest ranges equal to the lower ranges. Diodes, D301 and D302, limit the peak signal voltage at the amplifier input to approximately 8 volts and in conjunction with R26, protect the instrument against damage from inputs of up to 400 volts peak.

The input stage consists of the field effect transistor, TR301, connected as a source follower driving the emitter follower, TR305, via R303. The operating current of TR301 is defined by TR302 which is an identical transistor mounted in a common package with TR301 to ensure close matching and good thermal tracking. TR302 is self biased such that the operating current will develop a voltage across R308 equal to the gate-source potential. Since this same current flows in TR301 and R303 is identical to R308, the voltage at the base of TR305 is equal to the gate voltage of TR301. The drain-source voltage of TR301 is maintained constant by 'boots-rapping' with TR304 and D303. The drain-source voltage of TR302 is also maintained constant by the cascode transistor, TR303. Diode, D304, prevents the base-emitter junction of TR305 becoming reverse biased under overdrive conditions. The voltage at the gate of TR302 can be varied by R373 to balance out small variations in matching characteristics.

The signal at the emitter of TR305 is applied via the switched resistor network, R28/34, and the common base stage, TR306, to the shunt feedback amplifier formed by TR307, R312 and R311. This can be regarded as a 'virtual earth' amplifier with R311 as the feedback resistor and the R28/R34 network as the input resistor. Thus, the overall gain of the stage is selected by S3B to provide the six basic input sensitivities of the instrument. The common base transistor, TR306, is interposed to balance the d.c. offset voltage introduced into the signal path by TR305. Diode D305 is fitted to protect TR306 from reverse base-emitter voltages. The output from the collector of TR307 is taken via R315 to the base of TR309, which, together with TR310, forms a long-tailed pair. Transistors, TR315 and TR308, are connected in a similar fashion to TR306 and TR307 and provide a balancing d.c. voltage at the base of TR310. The mutual conductance of the long-tailed pair is determined by series combination of R319, R320 and R3. Resistor, R3, is the variable sensitivity control and is shorted by S13 when in the 'CAL' position. The preset potentiometer, R319, sets the overall gain of the pre-amplifier and C309 provides h.f. compensation.

Movement of the displayed trace will occur when the variable sensitivity control, R3, is operated unless the voltages at the emitters of TR309 and TR310 are equal (except for the input signal) and this balance is set up using potentiometer, R369. The collector current of TR309 feeds into a load resistor on the timebase board to provide an internal trigger signal.

4.3.2 BEAM SWITCH

The collector current from TR310 is passed through a cascode transistor, TR317, to the emitter of the beam switch transistor, TR319. A d.c. current determined by the shift control potentiometer, R1, and the series resistor, R387, is injected at the emitter of TR317 to provide a shift range of ±12 cms. If the base of TR319 is held high (approx. 3.3 volts) the signal current will pass through the forward biased diodes, D313, D315 and D316, to the load resistor, R389. If the base voltage of TR319 is low (approx. 0.4 volts) the signal current will flow through TR319 to ground and D313 will become reverse biased isolating Channel 1 from the common load resistor, R389. An identical beam switch circuit controls the output of

the Channel 2 pre-amplifier but the drive to transistor, TR320, is the complement of that to TR319.
For dual trace operation the beam switching technique employed depends upon the main operating mode switch. In the NORMAL mode the channels are switched on alternate sweeps when the timebase range switch is set to 2 msec./cm. or faster. On the lower timebase ranges the beam is chopped at a 225kHz rate. In the REFRESHED and ROLL modes the channels are always chopped at a rate dependent on the setting of the time-base range switch. On the 50μsec./cm ranges and above, the chopping rate is 0.9MHz; below this the chopping rate decreases pro rata i.e. at 5msec./cm, it is 9kHz and at 5 seconds/cm. it is 9Hz.

4.3.3 SIGNAL SWITCH

The combined input from both channels appears across R389 at a level of approximately 37mV/cm. This signal is taken via R201 to the Analogue to Digital convertor (section 4.4) and also via emitter follower, TR321, to the signal switch formed by diodes, D317 to D320. This determines whether the signal passed to the Y output stage is the direct signal from the pre-amplifiers (NORMAL mode) or the stored signal from the Digital to Analogue convertor (REFRESHED and ROLL modes). In the NORMAL mode, transistor TR324 is turned off and its collector is at a high level thus turning TR325 fully on. The voltage at the junction of diodes D319 and D320 will be low and both diodes will be reverse biased. The two diodes, D317 and D318, will be forward biased and conducting however, and a signal at the emitter of TR321 will be transferred to the junction of D318 and D319, and via R379 to the Y output stage. When a high level is applied via R362 to the base of TR324, this transistor is turned on, TR325 becomes cut off and the situation is reversed with D317 and D318 reverse biased and the signal from TR322 emitter transferred to the output stage. The stored signal from the Digital to Analogue convertor is applied via R355 to the base of TR322. To compensate for the dc level shift introduced into the signal path by the emitter followers, TR321–TR322, a bias supply is provided for the output stage by transistor, TR323, which is operating under quiscent conditions identical to transistors, TR321 and TR322. The collectors of all these three transistors are supplied via R391 and clamped by D321 to approximately −0.7V in order to reduce dissipation in the devices.

4.3.4 Y OUTPUT AMPLIFIER

The Y output amplifier shown in Fig.20 is a conventional two stage differential amplifier. Input signals from the signal switch are applied via SK.U to the base of TR409 and a bias signal at the same d.c. level (approx. +0.6 volt) is fed to the base of TR408. These two transistors form a long-tailed pair with the gain determined by the resistor combination, R437 and R438, in conjunction with the collector load resistors, R441 and R442. The two resistor-capacitor combinations, R443, C424, C426 and R448, C430 provide pulse response correction. The zener diodes in the collectors, D411 and D412, set the collector-emitter voltage across each transistor so that variations in power dissipation (and hence junction temperature) of the transistor with signal amplitude, are minimised. The output signal from this stage is applied to the bases of a second long-tailed pair, TR406 and TR407, which are connected in cascode configuration with TR404 and TR405, respectively.
The c.r.t. deflection plates are driven from the collectors of TR404 and TR405 with inductors, L401 and L402, providing shunt compensation. The networks, C419, C420, R425 and C421, R427 across the gain setting resistors, R426 and R435, provide h.f. compensation to ensure good pulse response.

4.3.5 BLANKING AMPLIFIERS

There are two separate blanking amplifiers producing intensity modulation of the c.r.t. display and these operate with three separate input signals viz:

i) The Sweep Blanking signal. This cuts off the beam except when a timebase sweep is in progress.
ii) Chop Blanking. This is a short duration blanking pulse applied in the NORMAL mode only when the beamswitch is being switched from one channel to the other at the fast chopping rate.
iii) Trigger Point Bright-Up. This is a short duration bright-up pulse applied once per sweep when a trace has been stored in the ROLL mode of operation.

The Sweep Blanking signal is amplified by a d.c. coupled amplifier comprising TR513 and associated components. The sweep blanking signal is derived from a TTL. logic gate (IC902a) in the timebase via R971 (see Fig.24). When no sweep is in progress the sweep blanking signal is at a low level (<0.4 volt) and transistor TR513 is cut off. The collector voltage in this condition is determined by the resistor chain, R526, R527 and R528, at approx. 90 volts. This voltage is applied to the second grid electrode (blanking electrode) of the c.r.t. and the beam is cut off.
When a sweep is initiated the sweep blanking input from the timebase rises to a high logic level (approx. 4 volts) turning on transistor TR513. The base drive to this transistor is limited by D507 becoming forward biased to avoid saturating the transistor and the collector voltage falls to 4 volts, thus unblanking the c.r.t. beam.
The remaining two input signals are amplified by the circuit comprising TR514, TR515 and TR516. Both the Chop Blanking (CB) and Trigger Bright-Up (TBU) signals are produced by TTL logic devices situated on the Timing Logic board and the Store Logic board respectively (see Fig.23). For detailed information on the timing of these signals see section 4.5
The Trigger Bright-Up signal is inverted by the common emitter stage, TR514, and applied to the base of TR515 via R508. The Chop Blanking signals are applied directly to the base of TR515 via R507 and the speed-up capacitor, C505. The signal at the collector of TR515 is fed to the base of TR516 via the d.c. level-shifting network, D508 and C519. The pulses occurring at the collector of

TR516 are a.c. coupled to the grid of the c.r.t. by C506. The resistor, R533, serves to isolate the c.r.t. grid from the relatively low output impedance of the power supply and the clamping diode, D509, prevents the grid from being driven positive w.r.t. the supply, and thus possibly positive w.r.t. the cathode.

4.4 ANALOGUE TO DIGITAL CONVERTOR

4.4.1 BLOCK DIAGRAM DESCRIPTION

The function of the Analogue to Digital Convertor (ADC) is to quantise the instantaneous signal magnitude into one of 256 levels. These levels are represented by an 8 digit binary code (8 bit word) and the conversion is performed once every 550 nanosec.

Referring to the block diagram Fig.3 the input is applied, via a scaling amplifier, to a sample-and-hold circuit. This samples the signal level every 550nSec. and presents this level to the first row of comparators. These compare the signal against 3 fixed voltage levels corresponding to ¼, ½ and ¾ full scale input voltage. The output states of these three comparators are then decoded to give the first two most significant bits of the output data, D1 and D2. A 'remainder' signal is produced by subtracting from the original signal the voltage represented by the two bits already decoded. This operation is performed by a summing amplifier, A1, and a 2 bit Digital to Analogue Convertor (DAC). The reference voltages for the comparators are generated by the precision resistors, R, and the current source, I1. These voltages correspond exactly to the voltages subtracted from the input signal in the summing amplifiers. Typical waveforms are shown in Fig.4.

This process is then repeated using a row of 7 comparators to decode the next 3 bits of data and a further DAC and summing amplifier to drive the final row of 7 comparators.

4.4.2 SCALING AMPLIFIER

Referring to the circuit diagram Fig.22 the analogue input signal from the beamswitch is applied via R201 to the base of TR201. TR201 and TR202 are a Darlington connected pair which, together with TR203 and TR204, form a conventional long-tailed pair amplifier. The output signal is taken from the collector of TR203 via the emitter-follower, TR205, and fed to the base of the sample-and-hold input transistor, TR206. The gain of the scaling amplifier (approximately x12) is determined by applying negative feedback via the potential divider network, R211, R207 and R208. Potentiometer, R217, and resistor, R209, introduce a d.c. offset into the amplifier output by drawing current through the feedback network. The diodes, D215 and D216, are normally reverse biased and clamp the output signal of the amplifier to within the working range of the ADC.

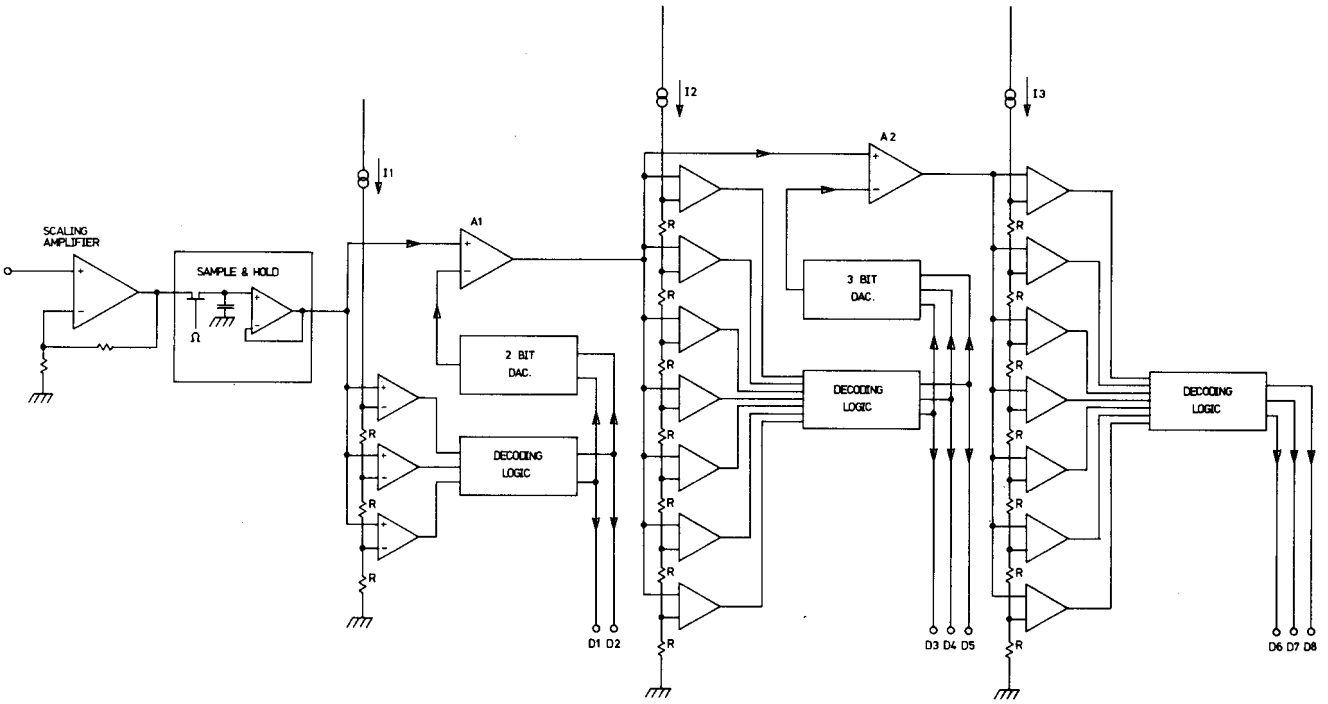


Fig.3 Block Diagram of ADC

4.4.3 SAMPLE-AND-HOLD

The signal from the scaling amplifier is presented via the emitter follower, TR206, to the sampling transistor, TR208. This is a junction f.e.t. and it's gate is controlled by the monostable circuit formed by TR209, TR207, TR210 and TR212.

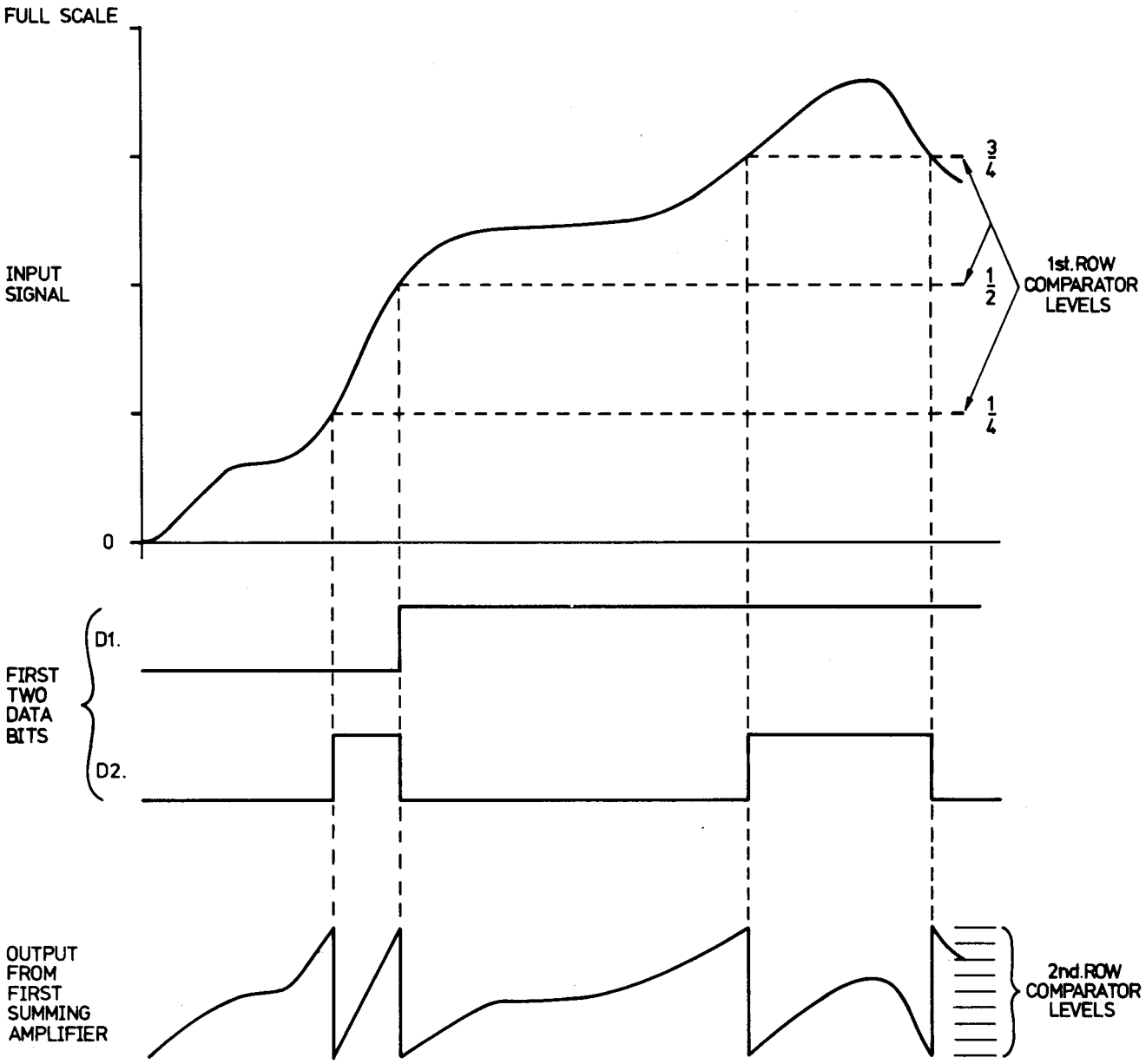


Fig.4 Typical Signal Waveforms (ADC)

The sample-and-hold cycle is initiated by a timing pulse from the ADC logic board applied to the base of emitter follower, TR226. This is amplified by the common emitter amplifier, TR227, and differentiated by C214. The negative going edge of this pulse appears at base of TR209 and turns off the transistor. The collector voltage of this transistor rises and turns on TR210 via emitter follower, TR207, and the potential divider, R222, R226. The negative-going signal at the collector of TR210 is fed back via emitter follower, TR212, D207 and C212 to the base of TR209 thus maintaining the circuit in this state until C212 charges up via R218, and TR209 turns on again.

In this way a large positive-going pulse, approximately 100nSec. long, appears at the gate of TR208. During this time TR208 conducts and charges C210 to the input signal voltage present at the emitter of TR206. The injection effect of the gate-drain capacitance in TR208 is compensated by driving TR211 gate with the inverse of the signal fed to TR208 gate. Similarly the drain-source capacitance of TR208 is balanced by an antiphase signal applied via C206. The voltage stored across C210

is buffered by a voltage follower comprising TR213, TR214 and TR215. TR213 is a source follower driving the emitter follower, TR215. The operating current of TR213 is defined by an identical transistor, TR214, operating in a manner similar to the Y Pre-Amplifier input stage as described in section 4.3. The low impedance output at the emitter of TR215 is fed to the first row of comparators, IC111 and IC112, and also to the first summing amplifier, IC102a.

4.4.4 COMPARATORS AND DECODING LOGIC

The comparators are very high gain integrated circuit differential amplifiers. The signal is applied to the non-inverting input and a reference voltage to the inverting input. If the signal voltage is less than the reference voltage the output of the comparator will be at its low limit. When the signal rises above the reference voltage the output goes to its high limit. The gain of the device is sufficiently high to ensure that the output will be at one limit or the other under most practical circumstances. The reference voltages for the comparators are generated by chains of precision resistors, R266–R268, R278–R284 and R146–R152, in conjunction with constant current source circuits. Since the digital to analogue convertors shown in the block diagram also employ current sources, these are grouped together and described later.

The outputs of the comparators are taken to the decoding logic. This provides binary coded output data corresponding to the state of the comparators, and is implemented with standard 74 series T.T.L. integrated circuits. Since the signal applied to each row of comparators is dependent on the state of the previous row, the full 8 bit conversion is carried out in a 'ripple through' fashion with a time lag between each of the three sections to allow for the settling time of the comparators and summing amplifiers.

The timing signals for the system are derived from a 9.09MHz oscillator driving a divider which generates the basic 5 phase 1.82MHz clock. This circuitry is included on the store logic board (see Fig.23). The waveforms and relative timing are shown in Fig.5 and the method of deriving them is explained in section 4.5.3. The five subsidiary clock pulses are labelled P1 to P5 and these are gated with the original clock frequency in various combinations to derive the timing signals for the decoding logic as shown.

The outputs of the first row of three comparators are applied to the latching bistables, IC120 a, b, c, which are clocked approximately 100nSec. after the end of the sample-and-hold pulse to allow the comparators to settle. Binary decoding is performed by IC121 b, c and the decoded outputs applied to the first two switched current sources which perform the function of the first DAC in the block diagram Fig.4.3.1.

The outputs of the second row of comparators are latched in two stages. The three outputs necessary to obtain the two most significant of the three bits of data available from this stage are latched in IC123 a, b and IC124 a. The outputs of these three latches are decoded in a manner similar to the first row of comparators, by IC122 c, d. The decoding of the third data bit is carried out directly from the comparator outputs by IC122 a, b, IC121 a, d and IC125 a. The decoded output is then latched by IC124b. To allow for the delay incurred by these gates, the clocking pulse to IC124b is delayed with respect to that applied to the other three latch bistables,

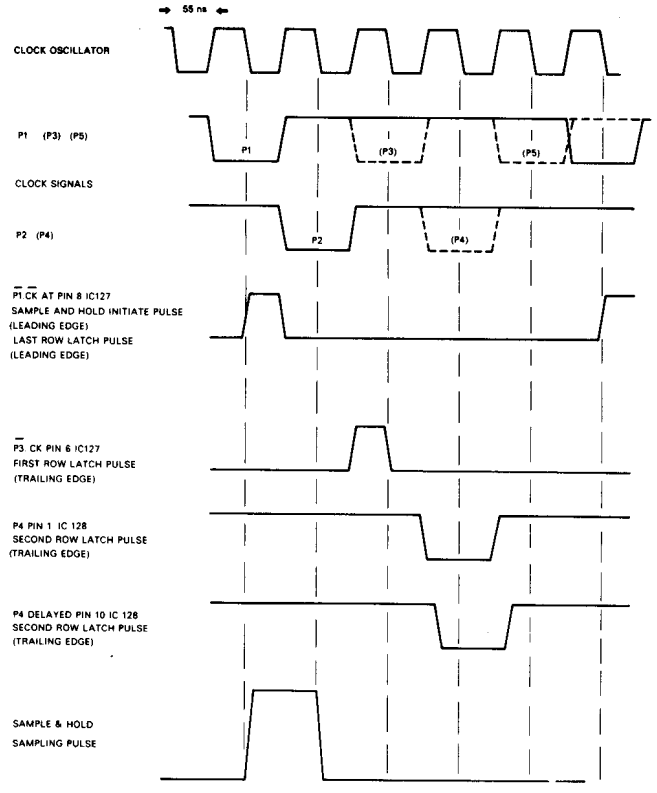


Fig.5 Timing Signal Waveforms (ADC)

by the four invertors, IC128 a, b, e, f. The decoded binary outputs are applied to the remaining three switched current source circuits and remaining undecoded fraction of the analogue input signal applied to the final row of seven comparators. The decoding logic for the final row is identical to that for the second row, except that the least significant of the three decoded bits is not latched at all hence there is no need for a delayed clocking pulse to this section.

The relative timing of the various operations performed during each cycle is shown in Fig.6.

4.4.5 CURRENT SOURCES

Within the A–D convertor circuit, Fig.22, there are a total of eight current source circuits. Three are employed supplying a fixed current to each of the resistor chains which define the reference voltages for the comparators.

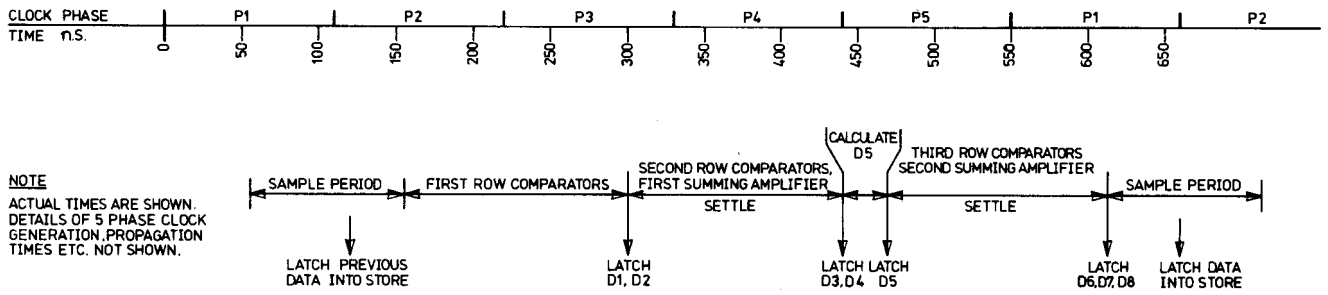


Fig.6 Timing Chart (ADC)

The remaining five are switched by the data outputs from the decoding logic. A common reference voltage is supplied to all of the current source circuits by the voltage regulator, IC101. The bases of the p.n.p. current source transistors, TR132, TR136, TR139, TR141, TR144, TR147, TR150 and TR151, are connected to this reference line and precision resistors in the emitter circuit define the collector current in each transistor.
The regulator, IC101, establishes the common reference line by comparing the voltage across R107, R266, R267 and R268 which is proportional to the output current of the first current source, with its own internal stable voltage reference. This internal reference, which is available at pin 4 of IC101, is attenuated to a suitable level by the potential divider chain, R104, R105 and R106, and applied to one input of the error amplifier, pin 2. The other input of the error amplifier on pin 3 senses the voltage across the resistor chain mentioned. In this way the regulator compensates for the effects of supply line drift, temperature sensitive transistor characteristics, etc. A current limit facility is provided by the regulator: When the voltage drop across the series resistor, R103, exceeds one forward base emitter drop (approximately 0.6 volt), the regulator is shut down preventing overdissipation.
Two of the current sources, TR132 and TR141, feed buffer transistors, TR133 and TR140, respectively, in order to supply the relatively high currents required by the first two comparator voltage reference chains.
The switched current sources are all identical with regard to circuit operation. Taking TR136 as an example, the base of TR134 is driven by the most significant bit data output at standard T.T.L. logic levels. A high level at this point causes collector current to flow through the load resistor, R113, and the catching diode, D101, turning off TR135. The current source transistor, TR136, then operates in the normal manner with it's emitter current defined by R114 and R115. A low level at TR134 base turns off the transistor and R113 pulls TR135 base positive, turning this transistor fully on and robbing TR136 of it's emitter current.
The currents of the first two switched current source transistors, TR136 and TR139, flow into a low impedance mode in the first summing amplifier and the remaining sources, TR144, TR147 and TR150, into a similar point in the second summing amplifier.

4.4.6 SUMMING AMPLIFIERS

The two summing amplifiers employed in Fig.22 are identical except for the value of the feedback resistor fitted. The component references mentioned in the following description apply to the first amplifier which drives the second row of comparators. IC102 is an integrated circuit array of five closely matched transistors, two of these forming a long-tailed pair differential input stage with a third acting as a current sink for this stage. A p.n.p. common emitter stage, TR219, amplifies the signal developed across the collector load resistors, R237 and R246, and an emitter follower, TR221, provides a low output impedance. These stages form a high bandwidth, differential input amplifier with negative feedback applied via R249 to the inverting input at the base of IC102 b. The analogue input signal from the sample-and-hold output transistor, TR215, is applied to the non-inverting input at the base of IC102 a, and appears at the output of the amplifier at the emitter of TR221 by virtue of the unity voltage gain feedback arrangement. However, the current from the switched current sources is injected into the inverting input of the amplifier at the base of IC102 b and flows through the feedback resistor R249 developing a negative offset voltage at the output, proportional to the total current injected. Thus the output signal from the amplifier represents the analogue input signal minus the first two bits of data already detected, which correspond to ¼, ½ or ¾ of the full scale input. The signal fed to the second row of comparators and the second summing amplifier input, ranges from zero to one quarter full scale.
The second summing amplifier operates in an identical manner except that the feedback resistor, R256, is one quarter of the value of R249. This affects only the magnitude of the injected currents which represent the three bits of data detected by the second row of comparators, that is $\frac{1}{32}$ to $\frac{7}{32}$ full scale.

4.5 CONTROL LOGIC AND STORE

Circuit details of the control logic are on Fig.23.

4.5.1 OPERATION IN THE REFRESHED MODE

A block diagram is shown in Fig.7. The 8 x 1024 bit store is connected to two 8 bit data latches, data in and data out, a ten bit address latch, and the Read/Write control. If the R/$\overline{W}$ line is high (read), when a new address is set up by the address latch on the ten store address lines, the eight bit data word stored at this address appears on the store 'data out' line and is held by the 'data out' latch. The ten stage binary read address counter is clocked continuously through all its 1024 states, each state being held in the store address latch. Therefore the total information held in the store is read out in sequence. As the readout is non-destructive it can cycle indefinitely. The D.A C. generates an analogue current output corresponding to the 8 bit code presented to it, and the dot joiner circuit removes the step transistions from the reconstructed signal before feeding this to the Y Output Amplifier via the signal switch. An output from the last stage of the read address counter is used to start a displaying X sweep, such that all 1024 8 bit words are read out in the time taken for the X sweep to scan approximately 11 cm on the c.r.t.

The clock generator feeds pulses to the range divider the division ratio of which is set by the timebase range switch in a 1, 2, 4 sequence between 1:1 and 1:400,000. The range divider output pulses cannot pass into the write address counter unless the 'enter data' line is high.

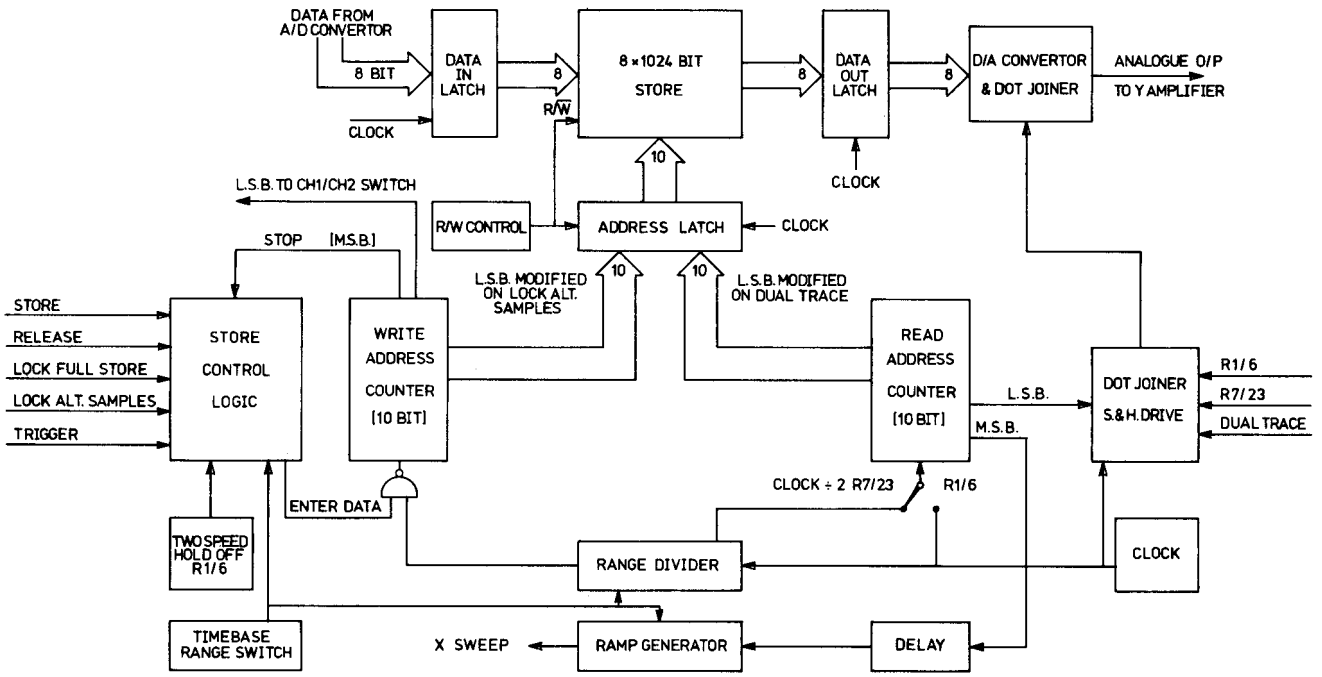
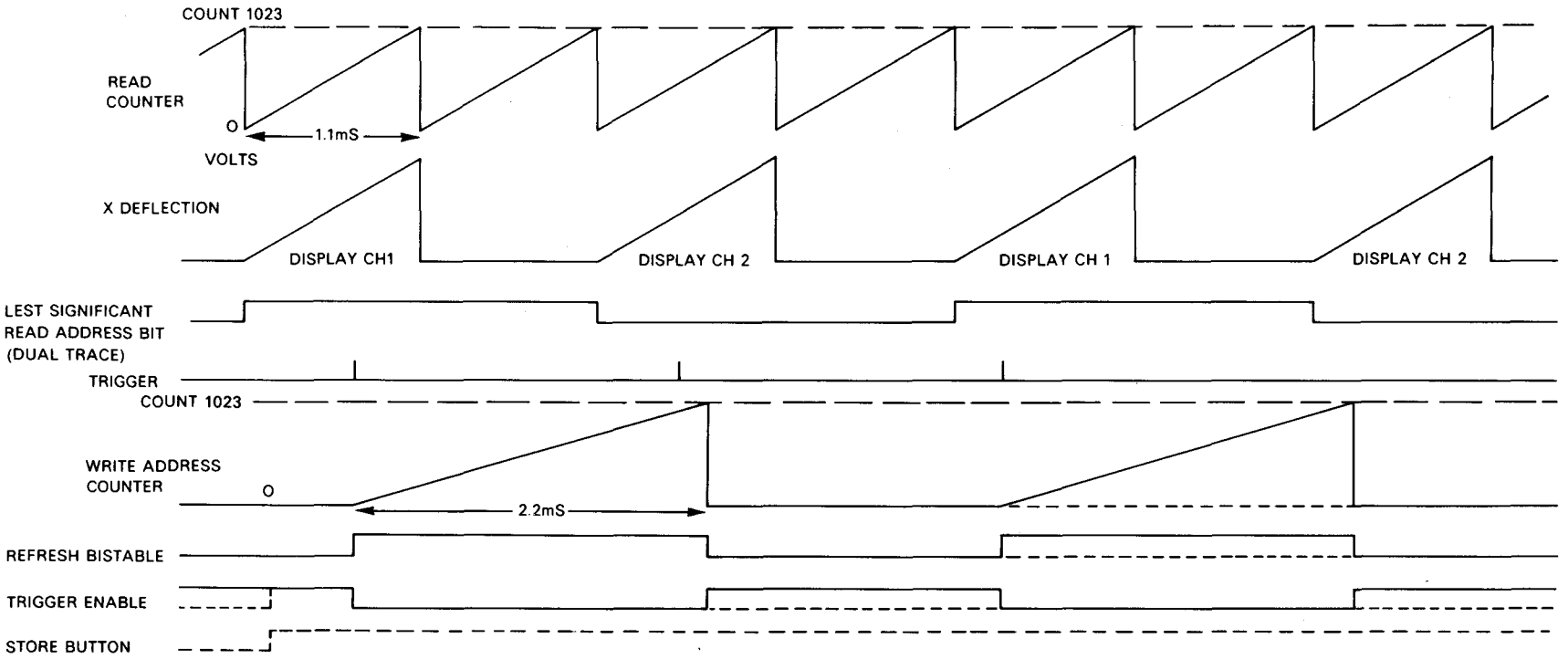


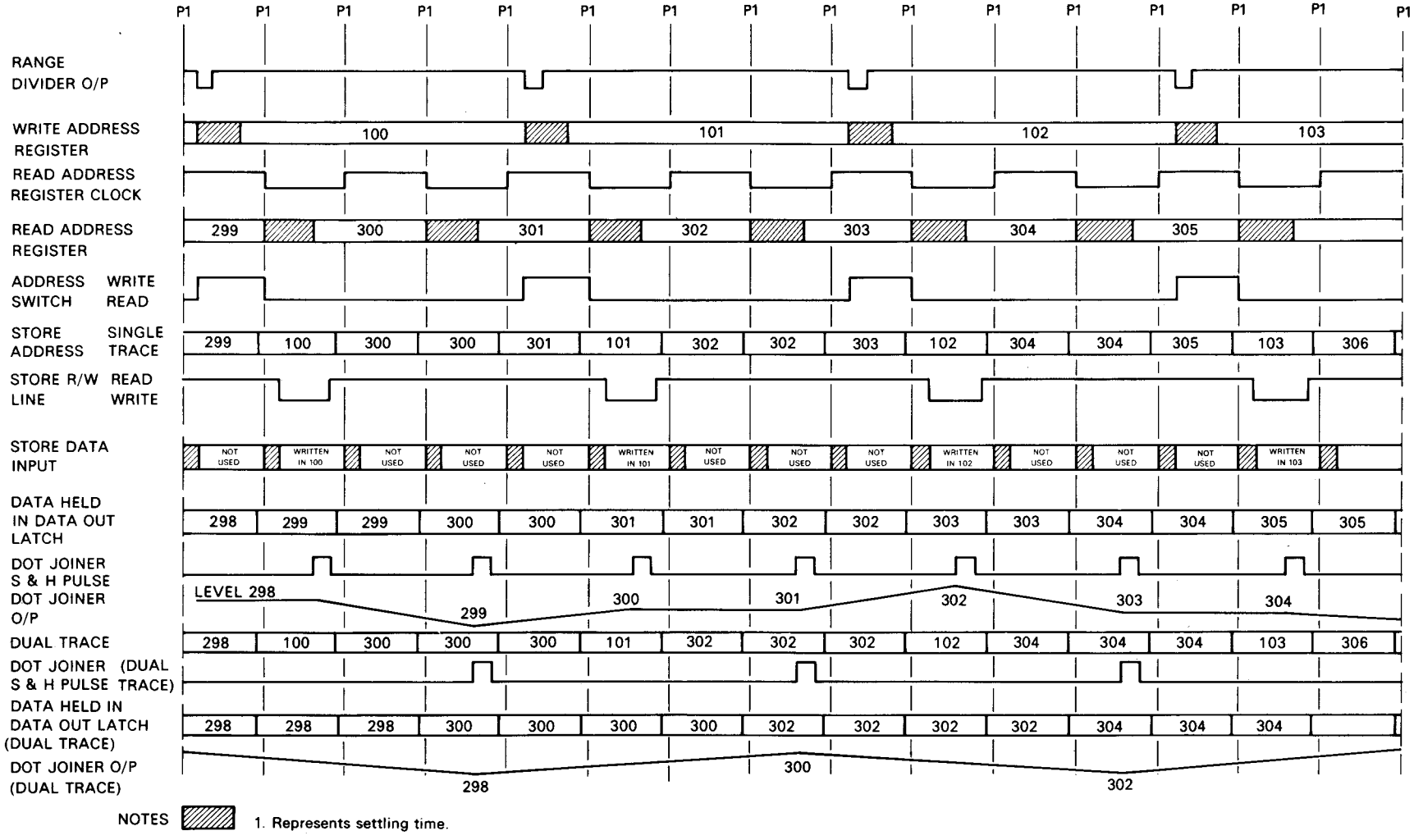
Fig.7 Logic Block Diagram: Refreshed Mode

Assume that the write address counter is at zero and that the control logic condition is such that an incoming trigger pulse has just driven the 'enter data' line high. The first pulse through the gate will increment the write address counter by one count and R/$\overline{W}$ will go low (write). The store address selector will cause the write address to be latched in the store. Data held in the 'data in' latch is then written into address 1 of the store. On the next clock cycle the R/$\overline{W}$ control is reset, the read address counter regains control of the address lines and the R/$\overline{W}$ line goes high. Subsequently data is written into successive addresses of the store every time the range divider generates an output until the write address counter state is 11,1111,1111. The next divider output pulse will cause all ten stages to go the 0 state. The 1 to 0 transition of the last stage (store full) acts on the control logic so as to drive the 'enter data' line low and prevent further clocking of the counter. In the Released mode of operation, the control logic is then ready to accept the next trigger signal to initiate a further write sweep.



Notes
1. Counting of the address registers is represented by ramps but exist only as digital signals.
2. Dotted lines represent operation after the STORE button has been operated.

Fig.8 Timing Diagram: Refreshed Mode



NOTES 1. Represents settling time.

Fig.9 Timing Diagram: Address Sequence

If the STORE button is pressed, the control logic is locked at the next 'store full' signal and the effect of further trigger pulses is inhibited. If the STORE button is again pressed the control logic allows one single triggered write sweep but if the RELEASE button is pressed, the trigger inhibition is removed completely. Typical operation is shown in Fig.8 for the 200μs/cm range. The increasing count in the address counters is represented as a ramp. The read/write interlace applies for time base ranges 100μs/cm to 20s/cm. Alternate clock pulses are used for read, leaving the remaining alternate periods available for write entry if called for by the range divider. Fig.9 shows this sequence for range 8.(200μs/cm). The initial addresses for this diagram are chosen at random but the subsequent sequence is relevant.

On range 6 and faster, the maximum writing speed of the store is used (550μs per address), and the control of the store address lines is passed to the write address counter for the time required to enter the 1024 new data words. The read system then holds-off trigger pulses until two reading sweeps have taken place.

4.5.2 OPERATION IN THE ROLL MODE

A block diagram of the system in the Roll mode is shown in Fig.10. The read and write counters are clocked as for the refreshed mode, and the 'data in' latch, store, data and latch, and address selectors function in exactly the same way as for the Refreshed mode. The essential differences are:

a) The display sweep is started from parity between the read and write address rather than from zero read address. This gives the effect of a moving display.

b) Data is entered continuously and trigger pulses have no effect until operation of the STORE button enables a trigger pulse to initiate a STOP sequence.

To generate the concidence signal which initiates the display sweep, the 10 address lines of the write and read address counters are connected to an eight bit and two bit comparator whose outputs are taken to a two input NAND gate. When the same address is present on the counters the gate output goes low and after a short delay the display ramp is started. As can be seen

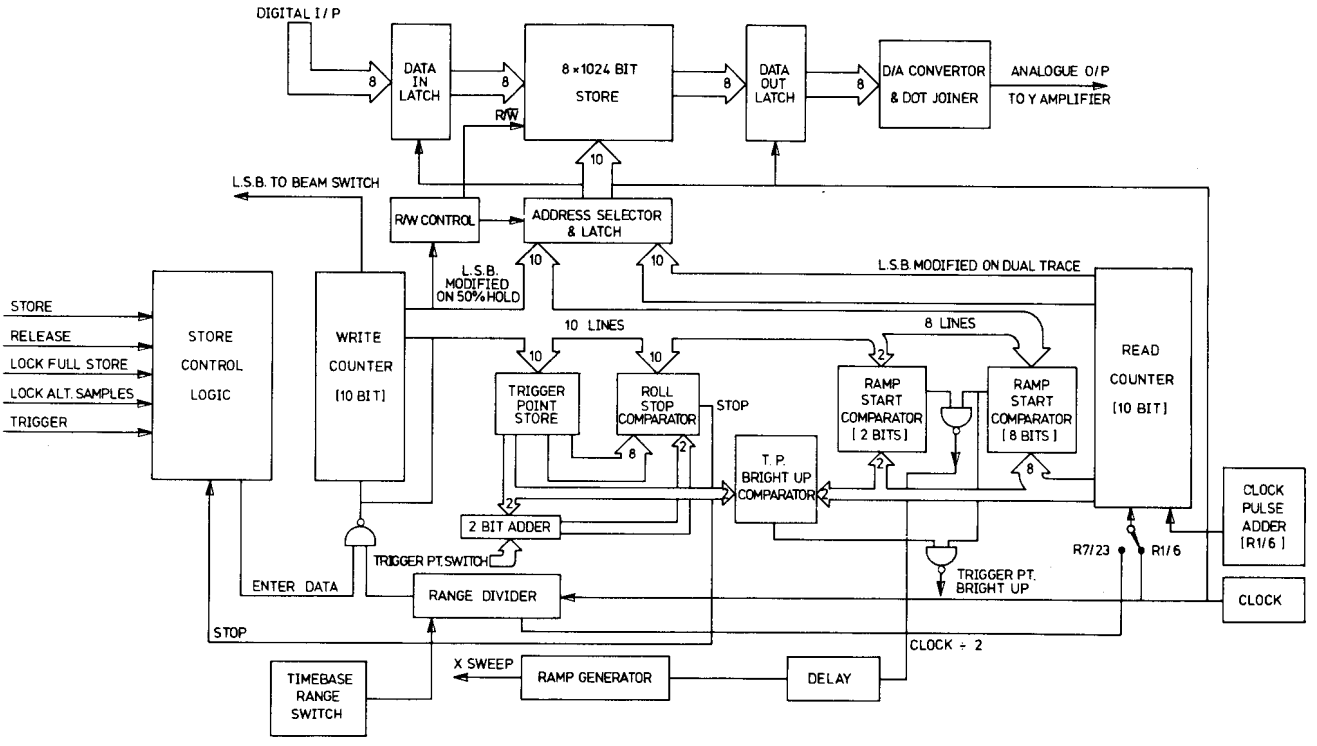


Fig.10 Logic Block Diagram: Roll Mode

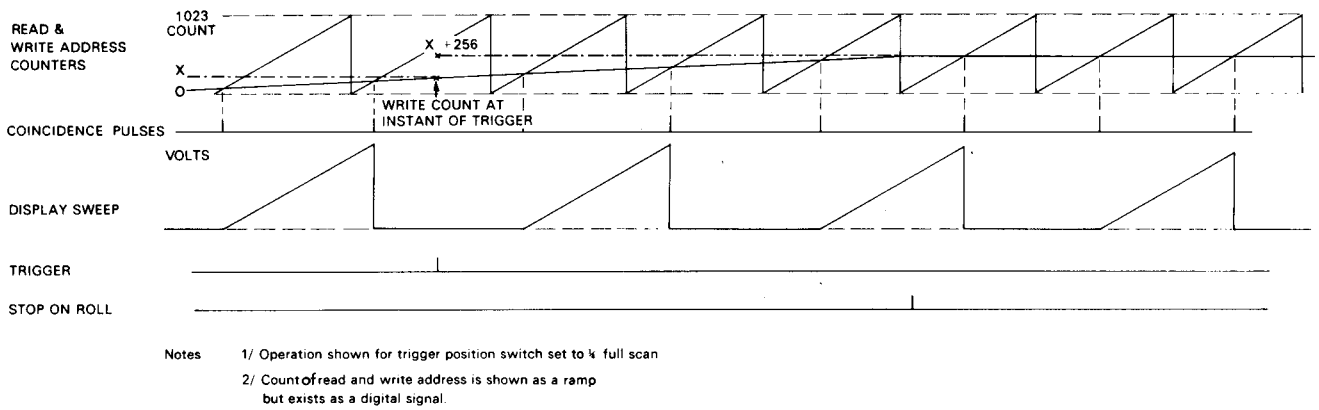


Fig.11 Timing Diagram: Roll Mode

from Fig.11, the write address counter is stepped-on at a slow rate determined by the range divider while the read address counter is stepped at a fixed fast rate. The comparator output occurs at the address where new information is being written into the store, and the displaying sweep started at this point (after a short delay) will display the oldest information first (left hand side of display) and the newest last (R.H.S.) When the Roll mode is selected while released, the store control logic drives the 'enter data' line high, trigger pulses have no effect on the operation of the system and the display follows the incoming data. If the STORE button is now pressed, the store control logic can accept a trigger signal and the address present in the write address counter at the instant of trigger, is held in the ten bit Trigger Point Store latch. The eight least significant bits in the latch are compared with the eight least significant bits of the write address counter. The two most significant bits held in the latch are added in a 2 bit binary adder to a two bit number set up by the Stored Trigger Point switch, before being passed to a two bit comparator to be compared with the most significant two bits of the write address counter.

If the number set up by the switch is 00 the comparator gives an output immediately after Trigger, which acting on the store control logic, drives the enter data line low, stopping any further information being written into the store. If the number set up by the switch is 01 (¼ full count), 10 (½ full count) or 11 (¾ full count), the write address counter must count on this amount before the comparator will generate an output and stop the entry of information. As the write address counter is now stable, every display sweep will be started at the same store address, and therefore the displayed waveform will be stationary.

4.5.3 CLOCK GENERATOR

The clock oscillator consists of TR602–TR603 connected as an emitter coupled oscillator, C601 being adjusted to set the frequency to 9.09MHz. TR601 is a buffer enabling the oscillator to drive the clock lines of the two dual bistables, IC's 610, 602. These are connected as a four stage shift register, but with the first input (pin 2, IC610) controlled from the output of a four input NAND gate, IC603 b, whose inputs are connected to all four bistables. Therefore the input to the shift register cannot go high until all Q outputs are low, and will go and remain low while a single high state is propagated down the shift register. The outputs from the bistables are inverted by IC611, and called P1, 2, 3, 4. P5 is taken directly from pin 8 IC603. The width of a P pulse is 110ns and the period is 550ns.

4.5.4 READ AND WRITE COUNTERS

The write counter consists of two four bit binary counter integrated circuits, IC655, 647 and a dual J.K. bistable package, IC639, connected as a two bit divider. Outputs are labelled B1 (least significant bit) to B10 (most significant bit) on the circuit diagram.

The read address counter consists of two four bit binary dividers, IC's 656, 648, and the dual bistable, IC640, connected as a two bit binary divider. The clock pulse for this counter comes from IC707c, which together with IC707d, a, and IC720b select the P1 pulse on ranges 50μs/cm and above, or the output from the first stage of the range divider on the lower ranges. The least significant bit of this counter (C1) is applied to the selector, IC719, whose output (C1') is connected to the store address selector. If a single trace mode is chosen the $\overline{\text{DUAL TRACE}}$ line operating on IC719 allows C1 to pass to the output. In the dual trace mode, C1 is blocked and the output of gate, IC719a, is determined by bistable, IC723a. This bistable is clocked by the display ramp bistable, such that on alternate sweeps odd and even read addresses are selected.

4.5.5 STORE, INPUT, OUTPUT AND ADDRESS LATCHES

The timing diagram Fig.9 includes details of the events in the 1.1μs period taken by a write and read cycle in the store. First, the ten address lines for the store must

be set and held at a new number, then new input data is set and held on the 'data in' lines. To write in data at this address the R/$\overline{W}$ line is taken low after 110ns for 330ns. True 'data out' is available 500ns after a new read address in set up.
The 'data in' latches consist of IC's 618, 619, which are clocked by the $\overline{P1}$. The address latches (IC's 652, 644, 636) are controlled by a pulse which is positive-going during the last half of the P5 period.
If a write cycle is to take place (Q of IC620a is high) the store R/W line is taken low from the beginning of P2 to the end of P4 period by the P2 and P5 pulses acting on the bistable formed by IC625 c, d. Output data appearing on pin 12 of the R.A.M.'s is held in the 8 bit 'data out' latch consisting of IC650, 659, by the leading edge of a positive-going pulse which is the address latch pulse inverted by IC625.

4.5.6 COMPARATORS

Three comparators are required. These are for 'stop on roll', 'trigger point bright-up' and 'display ramp start'. The circuits used are all quad exclusive NOR two input gates (8242 or equiv.) with open collector outputs. By connecting outputs together, two n bit binary numbers may be compared, and when they are equal the output will go high. These comparators function only in the roll mode.
The 'display ramp start' pulse is generated by exclusive NOR gates, IC654 a, b, c, d, IC646 a, b, c, d, which compare the eight least significant bits of the read and write counter, R618 is the common load resistor and IC638 c, d, compares the two most significant read and write address bits, with R617 as the load. The two outputs are then applied to two inputs of the 3 input NAND gate, IC632C, together with the $\overline{P4}$ pulse which acts as a strobe, allowing the state of the read and write counter to settle before the result of the comparison can pass to the output of IC632C.
The 'stop on roll' output is generated either immediately on receipt of trigger or after the write address counter has counted another quarter, half or three quarters of its full count. This is controlled by the front panel lever switch STORED TRIGGER PT. S602. When a trigger signal is received, the P5 pulse immediately following the trigger signal is gated by IC605d, and acts as a clock pulse on the ten bit latch, IC613, 621, 629, the inputs of which are connected to the write address counter. Therefore the write address set up at the instant of trigger is held in this latch.
The eight least significant bits held in the latch (outputs IC613, 621) are compared with the eight least significant write address bits, by IC614, a, b, c, d, IC622, a, b, c, d, whose common load is R627. The two most significant bits stored in the latch are applied to the two bit binary full adder, IC631, together with a two bit binary number derived from the front panel switch, S602. The result of this addition is applied to the comparators, IC623, a, b, and compared with the two most significant bits of the write address register. IC623d which compares the P1 pulse with 0V is also connected to the common output load R627. If the number set up by S602 is 00 there will be an immediate equality between the write address number and the latch number, so that during P1 period the comparator output will go high. If S601 sets up 01 so that the number held in the latch is increased by one quarter of the full count before being applied to the comparators, the write address counter will have to count on for a quarter of its full count to generate an output. Similarly the output is delayed by half or three quarters full count for the other positions of S602.
The number set up by S602 can be reduced to zero by gates IC606, b, c, when their inputs are driven high. This is done during the trigger enable sequence described in section 4.6.3.
To generate the 'trigger point bright-up' the read counter is compared with the number held in the trigger point store. The eight least significant bits are already compared in IC654, a, b, c, d, and IC646, a, b, c, d. The two most significant bits are compared by IC638, a, b, with R619 as the common load. The output of IC654, 646, and the output of IC638, a, b, are taken to two inputs of a three input NAND gate, IC632b, the third input of which goes high when both inputs of IC630a are high. The trigger point is only marked when the roll mode is selected and the STORE l.e.d. is illuminated.

4.5.7 RANGE DIVIDER

The divider consists of a multi-decade divider package, IC711 (Mostek 5009), and a dual distable, IC722, connected as a $\div 2 \div 4$ stage. P1 and P4 pulses applied to the cross-connected gates IC728 a, b, cause the output of 728a to go high from the beginning of P1 to the beginning of P4. The output of 728b is complementary. Output 728a is used to clock 722a, a J.K. bistable with J. and K. high, changing its output on the negative going edge. The Q output of 722a is used to clock 722b where J. and K. input are also high. Therefore the Q output of 722a is a square wave of half the P pulse frequency (0.909MHz) and the Q output of 722b is a square wave of one quarter the P pulse frequency (0.455MHz). The outputs from 728b, 722a, 722b, are applied to the selector, IC717c, IC706 a, b, c, which is driven from the timebase range switch via the inverters, IC705d, e, f.
The state of the three control lines, 9L, 12L, 15L, for all ranges is shown in the following table. For example when the timebase switch shorts 9L to ground, output 705d goes high enabling the output from 722a (0.909MHz) to pass to IC717. Only one line out of three is shorted on any range, the other two being high. In this particular case, outputs 705f, e, will be low and will drive the output of 706b, c, high. Therefore only the 0.909MHz signal will appear at output IC717c. This output is used to clock the decade divider, IC711. This is an M.O.S. device and requires a −12V line which is derived from the −20V line via R795 and D711. The division ratio of this IC is set by the three lines controlled by the timebase switch, (16L, 10L, 6L) as shown in table overleaf.

Range	Range No.	Range Divider Ratio	Range Divider Control Lines L16	L10	L6	L15	L9	L12
1μs/cm	1	1	0	0	0	0	1	1
2μs/cm	2	1	0	0	0	0	1	1
5μs/cm	3	1	0	0	0	0	1	1
10μs/cm	4	1	0	0	0	0	1	1
20μs/cm	5	1	0	0	0	0	1	1
50μs/cm	6	1	0	0	0	0	1	1
100μs/cm	7	2	0	0	0	1	0	1
200μs/cm	8	4	0	0	0	1	1	0
500μs/cm	9	10	1	0	0	0	1	1
1ms/cm	10	20	1	0	0	1	0	1
2ms/cm	11	40	1	0	0	1	1	0
5ms/cm	12	100	0	1	0	0	1	1
10ms/cm	13	200	0	1	0	1	0	1
20ms/cm	14	400	0	1	0	1	1	0
50ms/cm	15	1000	1	1	0	0	1	1
100ms/cm	16	2000	1	1	0	1	0	1
200ms/cm	17	4000	1	1	0	1	1	0
500ms/cm	18	10,000	0	0	1	0	1	1
1s/cm	19	20,000	0	0	1	1	0	1
2s/cm	20	40,000	0	0	1	1	1	0
5s/cm	21	100,000	1	0	1	0	1	1
10s/cm	22	200,000	1	0	1	1	0	1
20s/cm	23	400,000	1	0	1	1	1	0

The output from the decade divider is taken via the buffering inverters, IC705, a, b, to the clock input of the bistable, IC718a. The output of the range divider takes various positions relative to the system clock depending on the division ratio selected. IC718, a, b, is used to reclock the divider output pulse at P2. The decade divider output makes IC718a Q go high, driving high the J.and K. inputs of IC718b. The next P2 pulse allowed through the gate IC706d, will set Q IC718b high, $\overline{Q}$ IC718b low thus clearing IC718a. IC718b is cleared by the P3 clock pulse. Therefore IC718b Q is high for the P2 time after an output pulse from the range divider. These pulses are applied through gate, IC732c to the write address counter.

4.5.8 DISPLAY RAMP START AND STOP

Ramp Start Selection

The ramp start pulse is generated either by the most significant read address bit (Refreshed Mode) or by the ramp start comparators, IC654, 646, 638 acting on IC632c (Roll Mode). One of these two signals is selected by the selector, IC740, a, b, c, d, and appears at the output of IC740d. Selection is controlled by IC728c and IC717a. In the refreshed mode the ROLL line is low, driving the output of IC728 high and passing the most significant read address bit through the gate, IC740. The other input to IC728 controlled by IC717, can have no effect. In the Roll mode, for the output of IC728c to go low and select the signal from the ramp start comparators, the output of IC717a must also be high. It can be seen from the input connections of IC717a that on the fastest ranges (1/7) if the STORE l.e.d. is not lit and the 100% HOLD button not pressed, the output of IC717a will be low, forcing IC728c output high, resulting in the ramp start being derived from the read counter. This is necessary since on the fastest ranges the read and write counters are being clocked at the same frequency and therefore would never become coincident. When the STORE l.e.d. is lit or the Lock Full Store button pressed, the write address counter is not counting and coincidence pulses will again occur and can be used to start the displaying ramp.

Ramp Start Delay

The selected output is used as the clock input to the monostable pulse generator circuit consisting of a J.K. flip flop, IC741a, TR715, R771/772 and C718. In the quiescent state, Q of IC741a is low, TR715 is off and its collector load, R772, pulls the 'clear' input of IC741a high. Conditions around IC741a are:- Clear and 'preset' are high, J is high and K is low. A negative transistion on the clock input will cause the Q output to go high and the $\overline{Q}$ output to go low. This negative step is transmitted via C718 to the base of TR715, driving it negative by about 3V w.r.t. ground, but the current through R771 charges C718 eventually pulling the base of TR715 above ground potential and turning on TR715. The delay time is therefore set by R771 and C718. The collector of TR715 goes low, applying a 'clear' input to IC714a to drive $\overline{Q}$ high and Q low. C718 is rapidly charged via the base-emitter junction of TR715, but as the charging current falls to zero, TR715 again turns off, thus returning the circuit to its original condition.
Monostable, IC741a, does not perform a delaying function. In the ROLL mode, because the result of the comparison between read and write counters is strobed by P4 to allow for settling times, but the read counter is being clocked on most ranges at one half the clock frequency, the ramp start output consists of a pair of pulses. The delay set by IC741a is sufficient to ensure that the second pulse of the pair is ignored.
The negative transistion at $\overline{Q}$ IC741a caused by the first ramp start pulse, is used as the clock input to an identical circuit, IC739a, TR717, R794, R793, C714, which generates a pulse width of approximately 2μs.

Ramp Stop

The Q output of IC739a acting through IC717b and IC728d turns on TR718 for this period, driving the 'clear' input of the display ramp bistable on the timebase p.c.b. (IC903b) low, thus ending the displaying ramp if it is running at that time.

Ramp Start

The negative transition at Q–IC739a when it returns to the quiescent state, clocks IC739b, a J.K. flip flop connected as a divide by two. Assume that the clock pulse drives Q–IC739b from low to high. The 'clear' inputs to IC741b and IC742b are now removed and IC742b can respond to pulses on its clock input. These are the gated P4 pulses used as sample-and-hold pulses for the dot joiner circuit, and can be at full clock rate, half clock rate or quarter clock rate depending on timebase range and single/dual trace operation. The first P4 pulse incident on the clock input of IC742b after the clear input has been removed, will drive Q–742b high, and the second will drive Q–742b low, $\overline{Q}$–742 high $\overline{Q}$–741b low, which makes the J & K inputs of IC742b

both low, preventing further clock pulses having any effect. The low/high transition of $\overline{Q}$–IC742b acts as the ramp start pulse through connection N/M16 and gate, IC904d, on the clock input of the ramp start bistable, IC903b.
The next ramp start pulse from the read counter or comparator system will, via monostable, IC741a, drive IC739a to the opposite state, i.e. Q high to low. Thus $\overline{Q}$–IC741b is returned to the high state, $\overline{Q}$–IC742b is held in its high state and cannot generate a ramp start signal. Therefore the ramp start signals are divided by two, but the ramp stop signals are not. The generated sequence of signals is:- STOP START – STOP – STOP START – STOP – STOP START, etc. The STOP signal immediately prior to the START signal has no effect as the displaying ramp is not running at that time.

Read Counter Clock Pulse Adder
On ranges 1/6 in the Roll mode before the STORED condition is reached, the write address counter is in control of the store address lines and the read address counter does not determine the address of the information read out into the 'data out' latch. The information held in this latch is that which has just been written into the store. If the front panel controls have been set to call for dual trace operation (CH1 and CH2 operation or LOCK ALT. SAMPLES) the dot joining circuit will receive a sample-and-hold pulse at one half the clock rate (the least significant bit of the read address counter acts on gates, IC725a, b, and IC732a, to allow only every other P4 pulse through to drive the dot joiner sample-and-hold cct). To prevent this pulse from sampling the information in the same set of alternate addresses on every displaying sweep, an extra clock pulse is inserted into the read address counter input after every other full count. This ensures that the sample-and-hold pulse samples even address information on one displaying sweep, and odd address information on the next sweep and so on. This extra pulse is generated by IC721, and IC720.
Bistable, IC721a, is connected as a binary divider, with the clock input taken from the most significant read address bit. On every other full count output from the read address counter, Q–IC721a goes low clocking the binary divider, IC721b, driving its Q output high, and allowing the next P3 pulse via IC720a to pass gates, IC720c, IC720b and IC707c, to appear as a clock pulse at the input of the read address counter. The following P5 pulse acts on the 'clear' input of IC721b to return its Q output to ground and close gate, IC720c.

4.6 MODE CONTROL

4.6.1 DISPLAY MODE LOGIC

The switch, S601, has three positions, Normal, Refreshed and Roll. When the timebase range switch is set between the 500ms/cm and the 1μs/cm range the pole of S101a is connected to ground via S6, so that in the up position the l.e.d. indicating normal operation, D601, is lit, the centre position illuminates D602 (Refresh indicator) and the bottom position illuminates the roll indicator, D603.
When the timebase is set between ranges 1s/cm to 20s/cm the pole of S601b is grounded so that in the up position, D602 is illuminated indicating that the refreshed mode is operating. Outputs from this switch to the control logic are on 7H ($\overline{NORM}$) and 5H ($\overline{ROLL}$).
One of the l.e.d.'s, D601, 602, 603, is always lit unless the STORE l.e.d., D717, is on, in which case the base drive to the p.n.p. transistor, TR701, is removed and no current can flow through R609 to these l.e.d.'s.

4.6.2 HOLD

Output pulses from the range divider must pass through the three input gate, IC732c, to the input of the write address counter. The Lock Full Store push button, S703a, drives a slave bistable, IC702a, d, for switch de-bouncing. When the button is pressed the input of invertor, IC727d, goes high, putting a low on one input of IC732c, cutting off this gate.
The LOCK ALT. SAMPLES button, S704a, driving a similar bistable, IC701a and d, puts a low on IC707c, blocking the signal from the least significant write address bit (B1) and driving the least significant write address line ($\overline{B1}$) permanently high. Half the contents of the store cannot now be addressed by the write counter, but will continue to be displayed. Action of the dot joiner requires that if single channel operation is in progress, two display traces must be established, one the held information and the other the current information.
IC701a and d, drives high both inputs of the open collector gates IC735, so that the DUAL TRACE line is pulled low. This causes the least significant bit of the read address to come under the control of the display ramp bistable such that alternate sweeps display odd and even store locations as for any dual trace display.

4.6.3 STORE AND RELEASE

Fig.12 shows a simplified section of this part of the complete circuit of Fig.23.

Operation in the Refreshed Mode
Assume that the RELEASE button has been pressed. Bistable, IC708a and IC726a, are cleared, $\overline{Q}$–IC726a is high so that the ARMED l.e.d., D716, is off, and Q–IC708a is low applying a low input to the two gates, IC733a and IC732b, driving their outputs high, so that the TRIGGERED and STORED l.e.d.'s are off. The output of IC732b (high) drives on TR701 via IC702b so that l.e.d., D602, controlled by the mode switch, S601, is lit. The gate, IC731c, has two high inputs, $\overline{Q}$–IC708a and the $\overline{ROLL}$ line, so that its output is low. This turns off IC713b so that its output will rise if the "wired or" gate, IC713c, is also off. This gate is controlled by the two sweep hold off system, IC723a, b (described later) and may be assumed to be off in this section. Consequently the trigger enable line is always high after the RELEASE button has been pressed.
When the STORE button is pressed bistable, IC726a, is clocked such that $\overline{Q}$ goes low turning on the ARMED l.e.d. Gate, IC731b, now has two high inputs, Q–IC726a and Q–IC726b (this bistable is held preset by the ROLL

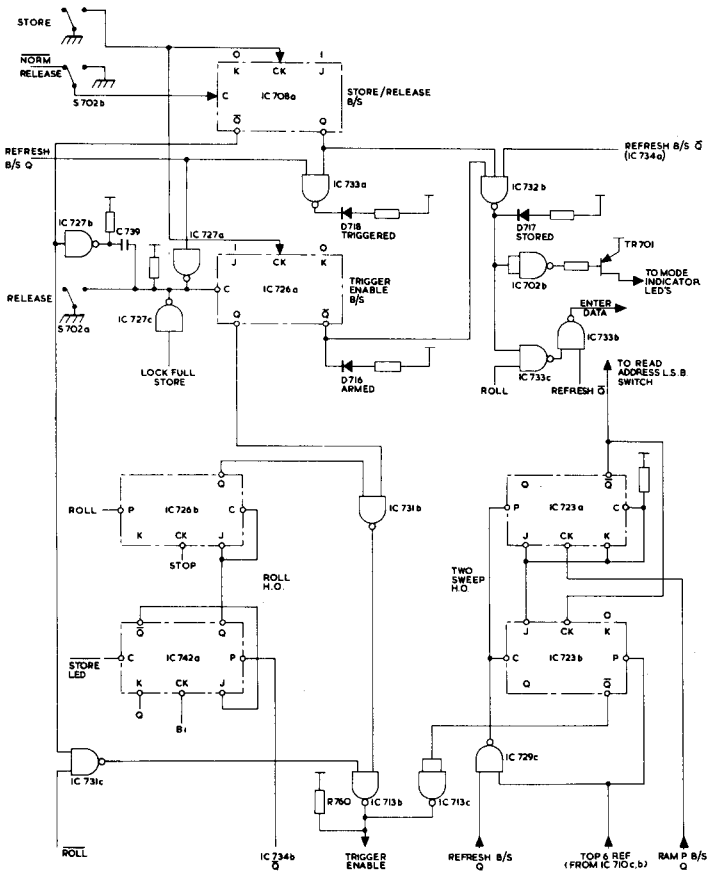


Fig.12 Simplified Control Logic

line being low), and so its output is low. This, acting on IC713b, holds its output high as before. The action of pressing the STORE button also clocks bistable, IC708a, such that the $\overline{Q}$ goes low driving high the other input to IC713b via IC713b. The result is that the trigger enable line is still high but this is now conditional on the state of the trigger enable bistable, IC726a. The gate controlling the TRIGGERED l.e.d. now has one high input (Q–IC708a) and one low input (Refresh B/S–Q) so that this l.e.d. is still off. The gate controlling the STORED l.e.d. has two high inputs (Refresh B/S–$\overline{Q}$ and Q–IC708a) and one low input ($\overline{Q}$–IC726a) so this l.e.d. is also off.
When a trigger signal occurs, the refresh B/S–Q goes high and this operating through invertor, IC727a, on the 'clear' input of IC726a, resets it, turning off the ARMED l.e.d., D716. The gate controlling D718 now has two high inputs so this l.e.d. (TRIGGERED) is lit. The gate controlling the STORE l.e.d., IC732b, now has two high inputs (Q–IC708a and $\overline{Q}$–IC726a) and one low input ($\overline{Q}$–Refresh B/S), so the l.e.d. is off.
On completion of a writing sequence the RefreshQ output will go low, turning off D718 and turning on D717, the STORED l.e.d. It also turns off TR701 and extinguishes the Refreshed Mode indicator l.e.d. D602. Q of IC726a going low, drives the trigger enable line low via the two invertors, IC731b and IC713b.

Pushing the STORE button again will clock Q–IC726a to the high state, so driving the trigger enable line high until another trigger signal is accepted. Pushing the release button sets $\overline{Q}$–IC708a high, driving the trigger enable line permanently high via gates, IC731b and IC713b.

Two Sweep Hold-Off Circuit

This circuit only operates in the refreshed mode on the timebase ranges 50μs/cm to 1μs/cm.
On these timebase ranges it is necessary that the writing sequence interrupts the reading sequence (this is described in section 4.5.1). If the system were allowed to respond to rapid trigger pulses, no full reading of the store would occur resulting in a blanked display. To prevent this, after every writing sequence the trigger enable line is held low until two reading sweeps have taken place.
Under all other conditions the line, TOP6 REF, will be low, presetting bistable, IC723b, and applying a permanent low to IC713c turning off this half of the "wired or" gate, so that the state of the trigger enable line is controlled only by IC713b.
When the TOP6 REF line is high, the preset input is removed from IC723b. When the refresh B/S–Q is set high by a trigger signal at the start of a writing sequence, the output of gate, IC729c, will now go low setting the $\overline{Q}$ output of IC723b high and the Q output of IC723a high. IC713c is now turned on and the trigger enable line pulled low. The display ramp B/S–Q will go low on the completion of the current reading sweep, but this cannot clock IC723a because of its preset input.
No more display ramp sweeps take place until the end of the writing sequence. When the refreshed Q goes low, displaying sweeps can again occur. The output of IC723a will change at the end of every display sweep (this output is used to generate the l.s.b. of the read address when dual trace operation is called for), and after two sweeps, the $\overline{Q}$ output of IC723a going negative acts as a clock pulse on IC723b setting $\overline{Q}$ low and therefore making the trigger enable line high by turning off IC713c.

Operation In The Roll Mode

Operation of the ARMED, TRIGGER, and stored l.e.d.'s is the same as for the refreshed mode previously described.
The action of the trigger enable is as follows:-
Assume the RELEASE button has been pressed so that $\overline{Q}$–IC708a is high, $\overline{Q}$–IC726a is low, and also that the output of the roll hold-off circuit, $\overline{Q}$–IC726b, is high (this is described later). The $\overline{\text{ROLL}}$ line being low drives high the output of gate, IC731c, and Q of IC726a acting through inverter, IC731b, also applies a high input to IC713b, turning on this gate and driving low the trigger enable line. As the STORE l.e.d. is off, IC733c has two high inputs thereby applying a low input to the 'enter data' gate, IC733b, forcing its output high so that data is written into the store continuously. Trigger signals will have no effect until the STORE button is pressed. This sets Q–IC726a high, and via the two inverters, IC731b and IC713b, sets the trigger enable line high. The ARMED l.e.d. is also illuminated. When a trigger signal sets the refreshed B/S–Q high bistable, IC726a, is reset

by inverter, IC727a, turning off the ARMED l.e.d. and returning the trigger enable line to the low state. The TRIGGERED l.e.d. is illuminated as previously described until a STOP signal from the store sets the refreshed B/S–Q low. This causes the TRIGGERED l.e.d. to be extinguished and the STORE l.e.d. to be lit. IC733c now has one low input, driving its output high, and the 'enter data' gate, IC733b, has two high inputs making its output (the ENTER DATA line) low. Loading of the store is therefore prevented, until either the RELEASE button or the STORE button is pressed. If the RELEASE button is pressed, IC708a is cleared driving one input of gate, IC732b, low and so turning off the STORE l.e.d. Gate, IC733c, now again has two high inputs, and its output acting on IC733b drives high the ENTER DATA line. If the STORE button is pressed, IC726a–$\overline{Q}$ is set low driving low an input to IC732b, extinguishing the STORE l.e.d. and causing the ENTER DATA line to go high.

Roll Hold-Off

When the sequence ARMED, TRIGGERED, STORED, has occurred the $\overline{\text{STORE LED}}$ line acting on the 'clear' input of bistable, IC742a, sets its Q low, applying a 'clear' to bistable, IC726b, setting its Q output low. This, acting through inverters, IC731b and IC713b, ensures that the TRIG. ENABLE line is held low when the STORE button is again pressed. Data will be loaded but the refresh B/S will not respond to trigger signals. The bistables, IC726b and 742a, provides hold-off such that when a trigger is eventually accepted and the store generates a STOP signal, the final display consists entirely of information loaded after the last pressing of the STORE button. Without this hold-off, a trigger signal could be accepted immediately and if the stored trigger point switch was set to its top position (100% pre-trigger), the display would consist almost completely of old (previously stored) information. When the STORE button is pressed, the write address counter is clocked and the least significant write address bit (B1) is used to clock IC742a, setting Q high, and this applies a high to the J input of IC726b, and also removes the low on its 'clear' input. This bistable can now respond to the store STOP output acting on its clock input. This will be generated by the next equality to occur between the number generated by the write address counter and the number held in the trigger print store. (This is not modified by the two bit adder circuit since the number set up on the stored trigger point switch, S602, is made 00 by the gates, IC606c, d, turning on when the refreshed $\overline{Q}$ line is high.) The clocking of IC742a by B1 ensures that IC726b is not cleared immediately by an existing equality between the write address counter and the trigger point store (S602 previous set to END TRACE position). When the STOP signal occurs, Q–IC726b, is set high enabling gate, IC731b, and allowing the TRIGGER ENABLE line to go high.

4.6.4 NORMAL MODE BEAM SWITCHING AND CHOP BLANKING

When S601 is set to normal, the read and write counters and the store continue to operate but their precise functioning in this mode is not important. Normal oscilloscope operation will be maintained as long as the timebase switch is set to range 18 or faster. Selecting a range below this will automatically bring in the refreshed mode.

In the normal mode the logic must provide several functions:-

1. Beam switching pulses ('Chop' and 'alternate' depending on timebase range).
2. Chop blanking pulses.
3. Trigger enable.
4. Connect the composite signal from Y input to Y output stage.

The inputs of the quad open collector NAND gate, IC710, are driven from the range switch and the mode switch to provide in normal operation, two lines which are used to obtain the required function.

a) A high on ranges 12/23 + normal line (BOT. 12 NORM).
b) Its inverse (O/P IC710d).

A "low on norm" line is obtained from S601. The timebase range switch connects 8L to ground on ranges 17/1 and hence S601 will ground cathode of l.e.d., D607, the anode of which is fed via the saturated transistor, TR701, from the +5V supply. D601 is therefore lit, indicating normal operation.

Beam Switching

CH1, CH2, or dual trace operation is selected by S603 acting on gates, IC736c and d. When input 10 of IC736c is set low, its output is set high, selecting CH2. When input 12 of IC736d is set low, output IC736c is set low, selecting CH1. If neither 10, or 12 of IC736 is set low, control of channel selection is passed to 13 of IC736d, which is connected to the output of the signal switch, IC709a, b, c, and d. In the normal mode, the "$\overline{\text{NORM}}$" line acting on 9, 10 and 4 of IC709, prevents the signal from the write address counter (12 of IC655) from passing through, and enables the signal from Q of IC708b to control the beam selection. This bistable is switched in two ways depending on the range setting, low sweep speeds select CHOP, high sweep speeds select ALTERNATE.

On ranges 12/17, the $\overline{\text{BOT. 12. NORM}}$ line acting on the 'clear' input of IC708b drives Q low, $\overline{Q}$ high. However the 'preset' input is driven from the gate, IC729a. As 2 of IC729a is high (BOT. 12. NORM line), the signal on the output of IC729a which is obtained from the second stage of the read counter, will control the state of the 'preset' input of IC708b. When the 'clear' is low and 'preset' high, Q is low, $\overline{Q}$ high. When 'clear' is low and 'preset' is low, $\overline{Q}$ is high and $\overline{Q}$ is high. Therefore, although the bistable does not change from one stable state to the other, the output at Q changes under the control of the second stage of the read counter. On the ranges 12/18 therefore the beam switch is operated at a frequency of 227kHz (chop mode). On ranges 11/1 the $\overline{\text{BOT. 12. NORM}}$ line drives the 'clear' high, and its inverse, acting through gate, IC729a drives high the 'preset' of bistable, IC708b. Therefore this bistable is

able to respond to pulses on its clock input, and with J & K high will change state for every –ve transition on its clock input, which is driven via 11/M, N by the display ramp Bistable Q output. Therefore at the end of every sweep, the beam switch will change over.

Chop Blanking

This signal obatined at the common output of three two-input open collector NAND gates IC713a and d and IC716a, with R703 as the common load. Chop blanking is only required in normal mode on the ranges, 12 to 18, when displaying two channels. The $\overline{\text{BOT 12}}$ line acting through IC713d will disable the chop blanking on the top ranges. The CH1, CH2 selection lines are applied to both inputs of gate, IC716d. Therefore if only one channel is selected, the output of this gate will be high, and IC716a acting as an inverter, will disable the chop blanking. As the beam switch in the 'chop' mode is driven from the 2nd stage of the read address counter, the blanking waveform must have a frequency of twice this. Therefore the output of the first stage of the read address counter is taken through an inverter, IC727f, to one input of IC713a, the other input being driven from the clock input to the read counter. Output of IC713a will be a waveform which is low for one system clock period (550ns) and high for three periods.

NOTE: When IC713d and 716a pull the blanking output permanently low, the display is not blanked because the blanking amplifier is a.c. coupled.

4.7 TRIGGER AND TIMEBASE

A clock diagram of the timebase and its control is shown in Fig.13 and the full circuit in Fig.24.

4.7.1 TRIGGER ENABLE

The logic system controls the state of the trigger enable line, 10M/N, to the timebase, which must be high to enable trigger.

In the normal mode, the $\overline{\text{NORM}}$ line acting through S702b (the release switch) on the clear input of IC708a, makes IC708a $\overline{Q}$ high. This is connected to one input of IC731c, a two input NAND gate, the other input of which (driven from the display mode switch) goes low only in ROLL. Consequently its output is low in the normal mode. This output drives one input of open collector NAND gate, IC713b, the output of which is common with IC713c, with R760 as a common load. The inputs of IC713c are driven from $\overline{Q}$–bistable, IC723a, which is disabled in the normal mode (preset low) with its $\overline{Q}$ low. As both IC713b and c outputs are therefore 'off' the trigger enable line is always high in the normal mode.

The state of the Input/Output lines on connector M/N, which connects the logic system to the timebase, is shown below for normal operation.

M/N			
	1	9	
	2	10	Hi
	3 Low during fly back.	11	Hi during sweep
	4	12	Lo
	5 Hi ranges 7/23, Lo 1/6	13	Hi during sweep
	6 Lo	14	
	7	15	Lo
	8	16	

4.7.2 TRIGGER CIRCUIT

The Line, CH1, CH2, and Ext. trigger signals appear on R912, 913, 914 and 915 respectively. R59, mounted on

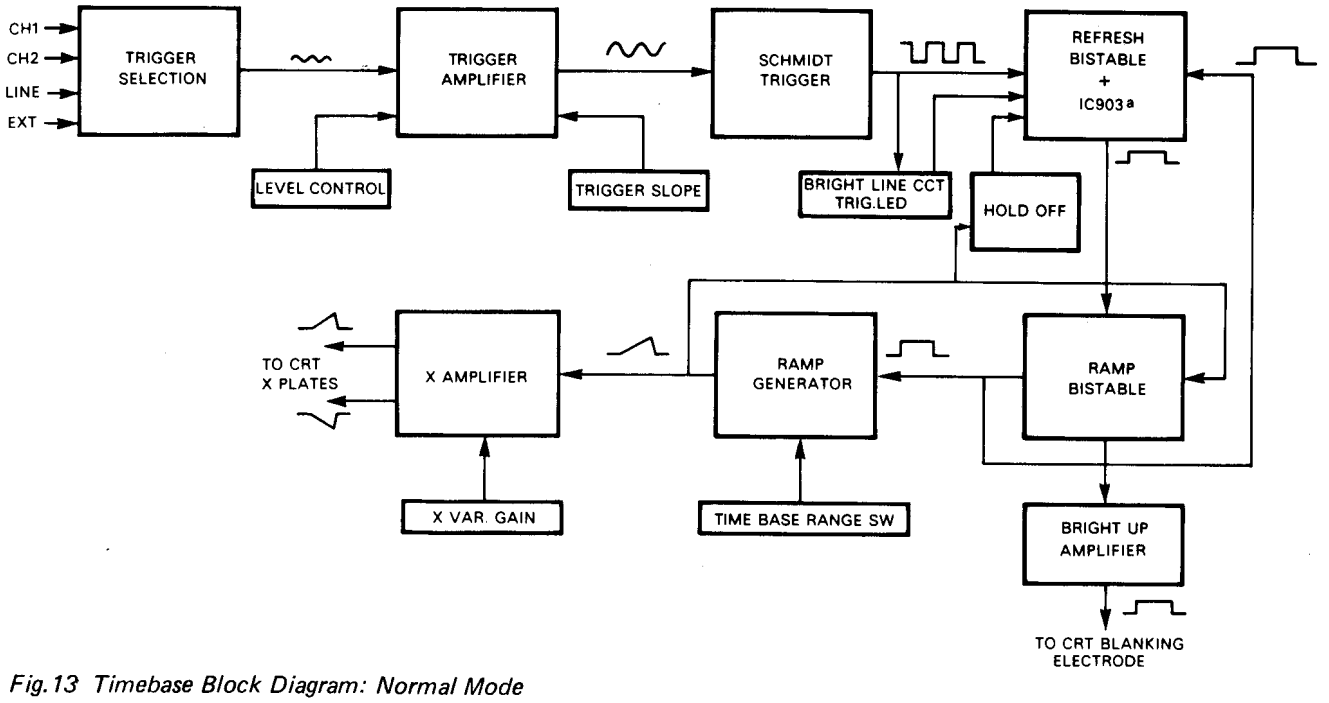


Fig.13 Timebase Block Diagram: Normal Mode

the transformer and connected to the low voltage winding, forms one arm of a potential divider with R912, resulting in a ± 50mV line frequency waveform appearing on R912, R913 and R914 are the collector loads of each TR309, in CH1 and CH2 preamplifiers. One centimeter of Y deflection results in a signal of approximately 25mV on these loads. R90 and R915 form an approximately 200:1 attenuator to external trigger signals. R1010, R1011, and R1008, R1009 are adjusted to take the collector currents which flow in the CH1, CH2 trigger leads, thus maintaining the voltage across R913 and R914 near zero in the absence of Y signals. One of these signals, selected by S900aR, the trigger source and slope switch, is passed to S901, the trigger coupling switch, and from there to the base of TR914. There are four possible signal paths, A.C. coupled via C907, H.F. rej. via C907 and R916 with C909 bypassing h.f. signals to ground. (fco ≙ 15kHz), LF. rej. via C908 with R917 bypassing l.f. signals to ground (fco ≙ 15kHz) or D.C. coupling.

TR914, acting as an emitter follower, passes the trigger signal to the amplifier pair, TR915 and TR916, the potential derived from the level control R7 being passed via emitter follower, TR917, to the base of TR916. Thus the amplified trigger signal appearing between the collectors of TR915 and TR916 contains a d.c. component determined by the setting of R7. The gain of this amplifier is determined by R919, 925, 920 and is approximately 4X. The signal is passed via S900bR to the input of amplifier, TR901/TR902. If CH1, CH2 or EXT are selected the collectors of TR915 and 916 are connected to the bases of TR901/902 for positive slope, and TR902/901 for negative slope. If line trigger is selected, the slope switching is reversed since the line trigger signal is in antiphase to the a.c. supply. TR901/902 form a differential amplifier whose output on the collector of TR902, drives the Schmitt trigger circuit TR903/TR904. The gain of amplifier TR901/902 is approximately 20 and the output d.c. voltage is adjusted with the common emitter resistor, R1012.

The function of the trigger circuit, TR903/904 is to generate a fast negative edge at the collector of TR904, independent of the rate of change of the applied signal. The signal appearing on the collector load of TR903/R932, is coupled via the network, R933, C902 and R935 to the base of TR904, whose emitter is connected to the emitter of TR903 and to the emitter resistor, R934. The emitter coupling introduces positive feedback which results in a latching action as follows:-

When the base of TR903 is at a low voltage, TR903 is off, its collector potential is high, therefore the base potential of TR904 is high turning on TR904. The emitter potential of TR904 is now higher than the base potential of TR903. When the base of TR903 goes more positive than the emitter of TR904, TR903 starts to take some of the emitter current of TR904, causing a reduction in its collector voltage which is communicated to the base of TR904 thus causing a further reduction in the current flowing. This effect is regenerative finally leaving TR903 on and TR904 off. The base potential of TR904 is now below that of TR903. As R932 is small, the change in base potential of TR904 is small (≙ 600mV between these two conditions) so that an a.c. signal of greater amplitude than this applied to the base of TR903 (if its d.c. level is adjusted) will cause the circuit to alternate in state. Thus the output of the circuit for any input above a minimum will consist of a series of equal amplitude pulses. C903 is a speed-up capacitor used to reduce the fall times of the output waveform.

4.7.3 BRIGHT-LINE AND TRIGGER INDICATOR

The waveform appearing at the output of the Schmitt circuit is coupled via R937/C904 to the detector circuit, D901, TR905 and C906. Positive going transitions on the Schmitt output result in C904 charging up via D901. Negative transitions result in the base of TR905 being driven negative, and C906 is charged negative by the emitter current of TR905. If no more negative inputs are applied, C906 charges slowly positive through R939, until the base-emitter junction of TR906 is forward biased. TR906 is then turned on and pulls the base of TR909 negative via R948, turning off TR909, and switching off the l.e.d., D916. If a trigger signal amplitude or level is altered such that the Schmitt trigger generates pulses again, C906 will be charged negative, TR906 is turned off and TR909 is turned on causing D916 to be lit. TR906 also controls the emitter current of TR911 via D903. The base biasing network, R950/R949, of TR911 is controlled by the $\overline{\text{NORM}}$ line via TR910. When $\overline{\text{NORM}}$ is low, TR910 is on, and the base voltage of TR911 is approximately 4V positive with respect to the emitter of TR906, hence when TR906 turns on and saturates, current will flow in TR911 and its load R970, such that TR911 will saturate. Its base voltage under these conditions is approx. 1.5V w.r.t. the emitter of TR906. When $\overline{\text{NORM}}$ is high, TR910 is off and the base voltage of TR911 is equal to the emitter voltage of TR906, therefore no current will flow in TR911 when TR906 is turned on. TR910 can be held off by S7 ("Pull for bright line off" on front panel). The current drawn by TR911 through R970 acts as a d.c. trigger on the timebase bistable in the absence of Schmitt trigger pulses and is only allowed in the normal mode when S7 is open.

4.7.4 TIMEBASE BISTABLES (REFRESH AND RAMP BISTABLES)

The refresh bistable consists of TR912 and TR913, cross coupled via R951 and R955 with C915 and C916 as speed-up capacitors and R953 and R954 as collector loads. The collector of TR913 drives the inverter, TR908, via network, R952. C914, R947 and D900, with the load resistor of TR908, R944, connected to the + 5V logic supply line. Thus the output at the collector of TR908 is in phase with the collector of TR912 and is a T.T.L. compatible signal designated "REFRESH Q" in the logic diagram. A T.T.L. signal on R946 will control the state of TR907 via network, R946/R945. The collector load of TR907 is connected to the base of TR912, hence a low on R946 will cause TR907 to turn on and therefore the

timebase bistable TR912 and TR113 will be reset into the condition of TR912 on, TR913 off. The driven end of R946 is designated as the 'clear' input of the refresh bistable on the logic diagram. This bistable can be set (Q output high) by the occurrence of a negative edge at the output of the Schmitt trigger (collector TR904) via C905, and D904 allows the negative pulse to pass if the junction of R938/R963 is near ground potential. If the junction of these resistors is at approximately + 5.5V, D904 is reverse biased sufficiently to prevent (hold-off) the trigger pulses from reaching the bistable input. (See section 4.7.5 on Hold-Off.) The bistable can also be set (Q output high) by the d.c. trigger current from the bright line circuit via R970. (See section 4.7.3 on Bright line.) This current is also blocked by the hold-off voltage while junction R938/R963 is high.

Assume that the bright line circuit is off, (no current in R970), the hold-off voltage is low, TR912 is on, TR913 is off and the Q output of IC903b (Ramp B/S) is low. A single negative transition at the output of the Schmitt trigger will cause TR912 to go off, TR913 to go on, and the Refresh Q output to go high. This output acts on three gate inputs, IC904c, IC906c and IC902d. For normal operation the table in section 4.7.1 shows that IC902d and IC906c have one input low (12N) therefore their outputs are permanently high and Refresh Q has no effect. Only IC904c is enabled (IC904d + IC904c form a 2 line to one line selector controlled by the $\overline{\text{NORM}}$ line) consequently when 10 of IC904 goes high, the common output (load R968) is pulled low causing a negative edge on the clock input of bistable, IC903b (Ramp B/S). Preset of 903b is always high, 'clear' is controlled by TR919 and is high until the end of sweep, J and K inputs are both high (low on 12N drives the output of IC906 high). These are the conditions required to cause outputs Q, $\overline{Q}$ of IC903b to reverse on a negative going clock edge. Q output therefore goes from low to high, and driving through inverter, IC905a, turns off TR920 (voltage across base resistor, R961, falls to zero). The timing capacitor selected by the timebase range switch is now free to charge positively (see section 4.7.5 for Ramp Generator). The Q of the ramp B/S (IC903b) also acts on two other gates, IC902c and IC902b, both two input NAND gates. (Operation of IC902b is described in the HOLD-OFF section.) Because 12N is low, the output of IC902d will be high, so one input of IC902c is high. When Q–IC903b goes high the output of IC902c goes low, driving IC902a output high. This supplies current to the bright-up amplifier (mounted on the Power Supply p.c.b.) via R971 and a coaxial lead, causing the c.r.t. beam to be unblanked at the start of sweep.

The ramp generator output (emitter of TR923) goes positive at a rate determined by the time base range switch, reducing the negative base voltage on TR919 via the potential divider R973/R974, and eventually when the emitter of TR923 reaches + 11V, TR919 is turned on, pulling the 'clear' input of IC903b low, causing Q to go low and $\overline{Q}$ high. ('clear' input of IC903b is connected to N3 into the logic system but no pull-down input occurs on this line in the normal mode.) When Q goes low, TR920 is turned on via IC905a, discharging the timing capacitor. The $\overline{\text{NORM}}$ line (6N) connected to IC905b causes its output to be high (high on NORMal), enabling three gates, IC902b, IC904b and IC904c. This output also turns on the hold-off circuit via TR918.

The output of IC904b (load resistor, R909) goes low when the Ramp B/S is reset, clocking IC903a. Conditions on IC903a are 'clear' high, 'preset' high (see note) J high, K low and $\overline{Q}$ high. The negative transition of the clock input will cause $\overline{Q}$ to go low, turning on p.n.p. transistor, TR907, via R946, and so pulling the base of TR912 positive, turning TR912 on, TR913 off, and Refreshed Q output low. This is connected via 13N to the logic system, and controls the 'clear' inputs of bistables, IC734a and b. When Q Refreshed goes low, IC734a and b are cleared and the Q output of IC734a drives the 'clear' input of IC903a low via interconnection 14N, returning it to the quiescent state.

NOTE: On all ranges below 50μs/cm to the slowest available range on normal (200ms/cm), a reset pulse will occur on 15M prior to the end of sweep. This positive-going pulse acting via inverter, IC904a, causes IC903a $\overline{Q}$ output to go low, thus resetting the Refresh B/S. which in turn clears bistables, IC734a and b, driving Q–IC734a low and via interconnection 14N, clearing IC903a. The clear input is still preset when the ramp B/S IC903b is reset by TR919 and therefore the clock pulse generated by IC903b cannot set IC903a again.

4.7.5 HOLD-OFF CIRCUIT

The $\overline{\text{NORM}}$ line is inverted by IC905b (output high on normal), turning on TR918, connecting one side of the hold-off capacitor (selected by S6dB) to ground, and making an input (5) of the NAND gate, IC902b, high. The other input of this gate is driven high by the Ramp B/S Q output when the ramp is running. Therefore the output of the IC902b goes low during the sweep and the output of IC901a will be driven high, cutting off D912 and diverting the current passing through R962 into D902. This current will charge the hold-off capacitor selected by S6dB, moving the junction of R963, D902 and R938 positively so that D912 and D911 are turned on when the capacitor voltage reaches + 5V plus two diodes forward bias potentials. (+ 6.2V approx.) This voltage acting through R938 drives the junction of C905 and D904 positively so preventing trigger pulses from the Schmitt trigger reaching the refresh bistable. At the end of sweep the Q output of the ramp bistable goes low, and drives the output of IC901a low. D902 is cut off and the hold-off capacitor is discharged slowly from + 6.2V until at approximately 0 volts, D902 again conducts. Therefore trigger pulses are prevented from starting another sweep for a time sufficient to enable the timing capacitor to discharge completely.

4.7.6 RAMP GENERATOR

This can use two timing networks, R1007 and C923 or the resistor and capacitor selected by the time base range switch, S6. The selection is controlled by the TOP 6 and

$\overline{\text{NORM}}$ lines acting on IC905c. In normal mode operation, $\overline{\text{NORM}}$ is low and IC905c output is high. The state of $\overline{\text{TOP 6}}$ has no effect. TR931 is turned on and TR930 is turned off by the differential signal applied from IC905c/905d via level shifting networks, R1002/R1003 and R1006/R1005. TR931 pulls the gate of f.e.t., TR929. low (−10V approx.) turning it off, and gate of f.e.t., TR928, is held by D909 and R1000 at a potential near its source voltage, so that this f.e.t. is turned on. This connects the R and C selected by the timebase range switch, S6, to the input of the ramp generator. Timing network, R1007 and C923, is selected in 'refreshed' and 'roll' operation on ranges, 7/23, by $\overline{\text{NORM}}$ and $\overline{\text{TOP 6}}$ being high. However $\overline{\text{TOP 6}}$ goes low on ranges, 1/6, so that the timebase range switch R and C is always used on these ranges. The ramp generator is a bootstrap circuit consisting of TR921, TR922, TR923 and D905. The timing resistor is connected from the junction of D905 and R978 to the timing capacitor, the other end of which is earthed. The junction of the resistor-capacitor timing network is connected to the base of TR921 via TR928 or TR929.

The voltage difference between the base of TR921 and the ramp O/P, TR923, is about + 0.6 volts, and D905 is a 8.2V zener diode whose bias current is supplied by R977. Consequently there is a voltage difference across the timing resistor of approximately 10V. The current flowing in this resistor will flow into either TR920 (if it is turned on) or the timing capacitor. If TR920 is on (Q ramp B/S is low) the timing capacitor cannot charge and the ramp output (emitter TR923) remains at approx. + 0.6V above earth. When TR920 turns off at the start of sweep, current flowing in the timing resistor starts to charge the capacitor positively. As the voltage gain between the base of TR921 and the emitter of TR923 is very nearly 1, the voltage across the timing resistor will remain essentially constant, thus maintaining a constant charging current into the capacitor and therefore a linear increase of voltage against time at the output of the circuit. At the end of sweep when the ramp O/P voltage is approx. + 11V the Q of the ramp B/S goes low. TR920 is turned on and rapidly discharges the timing capacitor, bringing the ramp output voltage back to + 0.6V.

4.7.7 X OUTPUT AMPLIFIER

TR924 and TR927 form a p.n.p. differential amplifier whose gain is controlled by the network, R987, R988, R6, R990 and R991. The base of TR924 is driven by the ramp generator and the base potential of TR927 is controlled by the X shift potentiometers, R8A and R8B. Preset controls, R988 and R990, are set so that as R6 is varied from maximum resistance to minimum, the gain is changed by 10 times. As the dynamic range of this amplifier is then only approx. 1.5V under these conditions, D913 and D914 are required to protect TR924 and TR927. The mixed sweep plus shift signal produced by this stage at its output loads, R983 and R998, drives the differential high voltage amplifier, TR925/TR926, whose collectors are connected via R985/R992 to the X plates of the c.r.t.

4.7.8 OPERATION IN THE REFRESHED MODE

Conditions at Logic/timebase interface M/N are:

1		9	
2		10	Hi after release Lo after 'Store' and trigger
3	Low during display ramp fly back	11	Hi during display ramp
4		12	TOP6. REF. $\overline{\text{LOCK 100\%}}$
5	$\overline{\text{TOP6}}$	13	Hi after trigger Lo after 'Stop'
6	Hi	14	
7		15	Stop (Storefull) signal
8		16	Ramp start signal

In this mode the display ramp B/S, IC903b, is controlled from the store, but the refreshed bistable, TR912/3, is under control of the incoming trigger signals as in the normal mode.

Assume that no trigger signals are occurring. The ramp start signal from the store on M/N 16, passes through gate, IC904, to the clock input of the display ramp B/S, setting Q high and via IC905a, drives off the ramp gate transistor, TR920, and starts the sweep.

The $\overline{\text{NORM}}$ line being high selects timing component's R1007, C923 via IC905c, d and TR928 to 931. This is a sweep of 100μs/cm. A RAMP $\overline{\text{RESET}}$ signal from the store will occur on M/N3 before the analogue ramp reset transistor, TR919, is turned on by the increasing ramp voltage. This reset pulse acting on the 'clear' input of IC903b drives Q−IC903b low, thus turning on TR920 and discharging the timing capacitor, C923. On timebase ranges 1μs/cm to 50μs/cm, the $\overline{\text{TOP6}}$ line (M/N5) acting via IC905c, d, and TR928 to TR931, selects the normal timing R's and C's, and therefore the sweep speed is that set by the timebase range switch. The analogue ramp reset transistor, TR919, may now be turned on by the increasing ramp voltage before the store generates a ramp reset signal. Thus only a portion of the store contents may be displayed on the c.r.t. on these ranges.

If a trigger signal occurs, the refresh bistable, TR912/3, is triggered as in the normal mode, by a negative step on the output of the Schmitt trigger driving off TR912 and, setting the refresh bistable Q (collector TR908) high. This removes the 'clear' inputs to the dual D type bistable, IC734a and b, making IC734b sensitive to the next $\overline{\text{P4}}$ pulse on its clock input. This drives Q−IC734b high, the $\overline{\text{Q}}$ of IC734a going low drives the output of gate, IC734b, high. This is the ENTER DATA line. Pulses from the range divider can now pass through gate, IC732, to clock the write address counter and also generate store write cycles. Q−IC734a going high removes the 'clear' input from IC903a making this bistable sensitive to the STOP signal generated by the store after 1024 new data words have been loaded. This signal acting via IC904a on the preset input of IC903a, sets $\overline{\text{Q}}$ low, turning on TR907

which in turn, pulls the base of TR912 positive thus resetting the refresh bistable, TR912/3. The refreshed bistable Q output (collector TR908) going low clears bistables, IC734a and b, driving $\overline{Q}$–IC734a high, and this acting via gate, IC733b, drives the ENTER DATA line low, inhibiting the entry of new information into the store. This cycle will repeat for every trigger signal until the STORE button is pressed and starts a single shot sequence. This is described in section 4.7.1.
In the refreshed mode the hold-off time delay is not required. TR918 is turned off by the NORM line (output of IC905b) going low, and this effectively disconnects from ground C90, 91 and 92, the hold-off capacitors.
Read/Write interrupt on ranges 50μs/cm to 1μs/cm. The changing of the display ramp generator timing components on these ranges has already been described. Another special condition applying to these ranges is that the read cycles must be interrupted to enable information to be written into the store. On slower timebase ranges (100μs/cm and below) read cycles taking 550ns occur every 1100ns and write cycles taking 550ns can occur no more frequently. Therefore read and write cycles can be interlaced. On the 50μs/cm to 1μs/cm ranges the write cycles occur every 550ns, leaving no time for read cycles. The system adopted is to read the store at a higher speed (550ns/address) until a trigger signal requires the store to accept new information.
The store then writes 1024 new data words at 550ns/address, and immediately after this two complete reading sweeps occur before another trigger signal is allowed to initiate a new writing sequence (see section 4.6.3).
On the ranges 50μs/cm to 1μs/cm in the refreshed mode with LOCK FULL STORE button out, the TOP6 REF. LOCK 100% line M/N12 will be high. If the Q output of the refreshed bistable, TR912/3, is low (no write cycles occurring) the output of gates, IC902d and 906c, will be high as on the slower timebase ranges. Therefore as IC906c drives high and J and K inputs of the display ramp bistable, this bistable will continue to respond to ramp start pulses from the store. However when a trigger signal switches the refresh bistable Q high during a display sweep, the output of gate IC902d is immediately driven low, causing the removal of the display ramp bright-up via IC902a and c. This is required since the write address counter will now have control of the store so that store data out will not be relevant to this displaying sweep. Also on completion of the display sweep, all three inputs to gate, IC906c, will be high, driving its output low and inhibiting any further displaying sweeps until the Q output of the refresh bistable goes low on the completion of the write sequence.

4.7.9 OPERATION IN THE ROLL MODE

Conditions at timebase/logic interface M/N are as for the refreshed mode. (See 4.7.8.)
The display ramp bistable, IC903b, is under the control of the store previously described for the refreshed mode. The hold-off circuit, C90, 91 and 92 is disabled as in the refreshed mode and the timing R and C are R1007 and C923. Until the STORE button is pushed, the trigger enable line is held low preventing operation of the refreshed bistable, TR912/3, (data is written into the store because input 5 on IC733b is low, driving the ENTER DATA line high). After the STORE button is pressed, the first trigger signal will drive the Q output of the refreshed bistable, TR912/3, high, removing the 'clear' input to bistable, IC734a and b. The first P4 clock pulse after this drives the Q outputs of IC734a and b, high, and the next P4 pulse drives Q output of IC734b, low. Further P4 pulses have no effect. The one clock period wide pulse from Q–IC734b acts on IC605d to allow through one P5 pulse from IC605c which acts as a clock to the trigger point store, IC613, IC621 and IC629, causing the state of the write address counter at the instant of trigger to be held in this store.
When a stop signal is generated by the store, this resets the refreshed bistable as previously described for the refreshed mode. (See 4.7.8.)

Ranges 100μs/cm to 1μs/cm

The TOP6 line acting through IC905c and d, and TR928 to 931, selects the normal timing components for these ranges. The display ramp bistable is reset by the analogue ramp reset transistor, TR919, and set by the ramp start signal from the store. Operation of the refreshed bistable is not effected. The sweep time is insufficient (except on the 50μs/cm range) to display the total contents of the store, and the stored trigger point marker may not be displayed.
On timebase range 7 (100μs/cm) after the RELEASE button has been pressed, the read and write counters are both clocked at 0.909MHz rate, so that the read and write addresses are never coincident. This is also true on timebase ranges 50μs/cm to 1μs/cm where the read and write counters are clocked at 1.818MHz. To generate a display on these ranges, the display ramp start is generated from the read address counter most significant bit until the STORE condition is reached. The write address counter then stops counting so that coincidence pulses are again generated and can be used to start the display ramp.

4.8 D/A CONVERTER AND DOT JOINER

Referring to the circuit diagram, Fig.25, the D/A converter is provided in a single integrated circuit, IC745. The latched eight bit binary outputs from the store, D1 to D8, are applied to the inputs, pins 5 to 12, and determine the output current from pin 4 as a proportion of the input reference current to pin 14. The reference input is fed through R729 from the zener diode, D701. R730 provides fine adjustment of this current to set the full amplitude of the analogue output.
The output from the D/A convertor is in the form of a step waveform which follows each successive change of digital input. The purpose of the subsequent dot joiner circuit is to convert this into a series of straight lines joining these successive levels.
As the D/A output level settles to a new value, amplifier IC744 detects its difference from the dot joiner output, and sets a voltage via sampling switch, TR707, on a storage capacitor, C707. This voltage is sufficient to drive

the integrating amplifier, IC743, to correct the error by the time the next sample is taken.
In more detail, the gain of IC744 and of the complete system is defined by the input resistor, R799, the shunt feedback resistor, R736 and the voltage divider, R751, and R734. The preset potentiometer, R774 with R733, provides a zero setting control to centre the displayed waveform. The output of IC744 is buffered by emitter follower, TR704, to drive the 'hold' capacitor C707 through the sample switch, TR707.
The data from the store is latched by P5 pulses, and the D/A converter and IC744 are allowed to settle before TR707 is switched on during a P4 pulse. These pulses are a.c. coupled by C709 into the base of the saturated switch, TR705. This transistor is normally conducting so that D702 holds the gate of TR707 near to −10V. TR707 is thus non conducting. During the P4 period the drive to C709 goes negative, TR705 is turned off and its collector rises toward + 5V. The emitter follower, TR706, takes the gate of TR707 rapidly toward + 5V until its collector-base junction clamps at 0V. In this condition TR707 conducts. At the end of the P4 period, TR705 is turned on and D702 returns the gate potential rapidly to −10V. TR709 and TR708 generate a similar but inverted drive waveform which is applied via C712 to C707 to compensate for the inherent gate to source capacitance of TR707 which injects an unwanted portion of the gate switching signal into the storage capacitor. The −10V line is defined by the zener diode, D703.
The integrator formed by TR743 can be considered to operate in its simplest form when f.e.t. switch, TR712, is open. In this condition the rate of change of output voltage for a given input voltage is determined by the input resistor, R750, with R785 and the feedback capacitor, C714. The input voltage from C707 is buffered by the emitter follower, TR710. R785 is used to adjust the output slope so that the detected error is reduced to zero at the next P4 sample period. If R785 is mis-set, the output will overshoot or undershoot in response to a step change of input but when set correctly the system will balance in one sample period.
The above condition with TR714 on and TR712 off, holds for the display of single trace information on the top 6 timebase ranges. In this mode, readout is taken on every clock pulse, P4 pulses are applied directly to C709 and the slope defined by C714 and R750 corresponds to 1 clock period.
For dual trace operation on the top 6 ranges or single trace operation on the slower ranges, the readout is taken from alternate clock pulses. The P4 input via C709 is gated accordingly and TR712 made to conduct. This introduces C715 into the integrator to slow the output slope by a factor of two and C713 provides slope adjustment for this mode.
For dual trace operation on the slower timebase ranges, readout is taken on one clock pulse in four, the P4 input to C709 is gated accordingly and TR714 is switched off. R752 and R768 are introduced into the circuit to halve the rate of change of integrator output voltage again, R774 providing balance adjustment.
Switches, TR712 and TR714, are controlled by TR713 and TR711 respectively. When on single trace operation and on the top 6 ranges, both inputs to the base of TR713 are high and TR713 is biased off and R759 holds the gate of TR712 at −10V. When either input goes low, TR713 conducts and its collector voltage is + 5V. D707 clamps the gate of TR712 at 0V for conduction.
TR717 operates similarly to turn off TR714 in all but the top 6 ranges and dual trace operation, but hold it on, either in single trace operation or on the top six ranges. Single trace operation with LOCK. ALT. SAMPLES is equivalent to dual trace.

4.9 CALIBRATOR

This consists of the adjustable current source, TR934, and current steering pair, TR933 and TR932. The most significant bit from the read address counter (11 on IC640b) is applied to the base of TR932 via 4N. The read address counter is clocked continuously at 1.82MHz on range 1/6 and 0.909MHz on ranges 7/23. The 10 bit counter divides these rates by 1024 giving frequences of 1.78kHz and 8.89kHz at TR932 base and also at the output. The drive to TR932 causes the current from TR934 to be switched between TR932 and TR933, where it flows into R1019 and R1020. R1017 is adjusted to give 1V across R1019 and R1020 in series, (1kΩ) and therefore 100mV across R1020 (100Ω). The current required to do this is 1mA so that shorting the 1V and 100mV cal. out pins together will cause 1mA to flow in the link.

5.1 GENERAL

The instrument is electrically protected by two fuses as follows:-

1. The supply line fuse, FS51, mounted on the rear panel by the line voltage switch. The rating is 500mA Slo-Blo (Part No.33685) for 220/240 volt supplies and 1A Slo-Blo (Part No.34790) for 115 volt supplies.
2. The + 170V fuse, FS501, mounted on the Power Supply board at the rear of the instrument. Access is by removing the bottom cover and the fuse rating is 250mA (Part No.32338).

The following sections give information allowing access to, and removal of, the various printed circuit boards and assemblies as may be found necessary during fault finding procedures.

If during fault finding, a component needs replacing it may be cut from the printed circuit board as close as possible to the component, leaving the wires protruding through to the component side of the board. The new component can then be soldered into position by attaching it to these protruding wires. This protects the copper track from damage.

If a fault on a printed circuit board cannot be cleared, it is recommended that the instrument is returned to the manufacturer for repair. When faults have been cleared it is recommended that the test procedure be implemented to ensure that the instrument conforms to the specification.

5.2 MECHANICAL ASSEMBLY

5.2.1 LAYOUT

Figures 14 and 15 illustrate the internal layout of the instrument and show the positions of the majority of preset components when the top and bottom covers have been removed. Each cover is retained in position by four latch fasteners. Each fastener is released by turning it one quarter of a turn clockwise or counter clockwise.

The POWER SUPPLY board contains the low voltage power supplies and also the blanking amplifiers. It is mounted across the rear frame of the instrument behind the c.r.t.

There are two identical Y PRE-AMPLIFIER boards (note that components have identical circuit reference numbers on each of these boards) mounted as 'daughter' boards at the front of the large ANALOGUE TO DIGITAL CONVERTOR (ADC) board. This board is secured underneath the c.r.t. and has two other 'daughter' boards associated with it: the CURRENT SOURCE board which is on the left hand side nearest the frame, and the DECODING LOGIC board on the right hand side.

The E.H.T. board incorporates the high voltage power supplies for the c.r.t. and also the Y OUTPUT AMPLIFIER. The INTENSITY, SCALE and FOCUS controls are directly mounted on this board, which is adjacent to the c.r.t. and one of four boards mounted vertically.

The STORE LOGIC is next to the EHT board.

The TIMING LOGIC board contains also the DOT JOINER circuit and is the third vertical board.

The TIMEBASE BOARD is mounted on the right hand side of the instrument and includes also the INTERNAL CALIBRATOR circuit.

The construction of the instrument has been arranged so that individual boards and assemblies can be checked and components changed so far as possible without completely removing the assemblies from the mainframe or disconnecting cableforms. In the case of the two logic boards this has been achieved by making them easily withdrawn from inside the mainframe to be mounted on top of the instrument, as shown in Fig.16. The instrument is then still fully functional

The following description details the method for removing the individual assemblies:-

5.2.2 STORE AND TIMING LOGIC BOARDS

The two logic boards are withdrawn as a unit:-

1. Remove the caps from the STORE, RELEASE and the two LOCK STORE pushbuttons. Remove the knobs from the MODE, STORED TRIGGER POINT and DISPLAY MODE lever switches.
2. Remove the 8 screws marked 'A' in Figs.14 and 15.
3. Swing the rear fixing brackets upwards to allow them to clear the rear mounting plate as the boards are withdrawn from the front panel. When the unit has been moved far enough to enable the lever switches and pushbuttons to clear the frame, withdraw the assembly from the top of the instrument with the various cableforms still attached.
4. Remove the screens from each board, and also unscrew the screen mounting pillars. This will allow the two boards to be separated. The two 'L' shaped fixing brackets should be removed from the top corner of each board and remounted on the bottom corner using the rearmost hole and a single nut and screw. The boards can now be fixed to the top of the instrument as shown in Fig.16, using the original fixing holes at the rear, and a single screw through a convenient hole in the frame at the front. Check that all the connectors are firmly in position.

   Refitting is the reverse of the removal procedure. Ensure that the 16 way ribbon cable plugs are fully pushed home after fixing the assembly inside the instrument.

5.2.3 TUBE AND REAR COVER

Removal of the tube is straightforward and provides access to the track side of the Analogue to Digital Convertor and E.H.T. boards. Note that access to the rear of the tube may be gained by removing the moulded plastic cover which is retained by four fixing screws. The tube is removed together with its magnetic shield in the following manner:-

1. Disconnect the E.H.T. lead at the cavity cap connector at the front of the tube.
2. Disconnect the two trace rotation coil leads at the top of the power supply board. Mark one of these leads so that they may be reconnected in the correct order. Disconnect the lead from the tube base to the pin marked GRID on the power supply board.
3. Remove the tube clamp, secured by three screws.

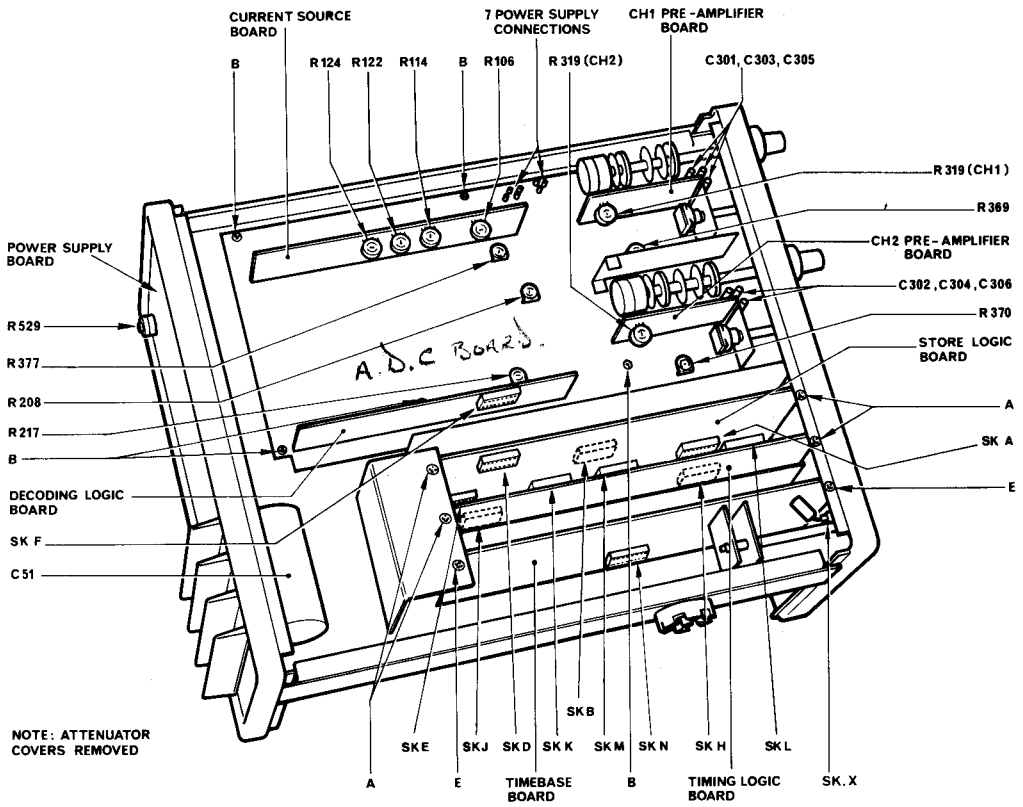


Fig.14 Bottom View

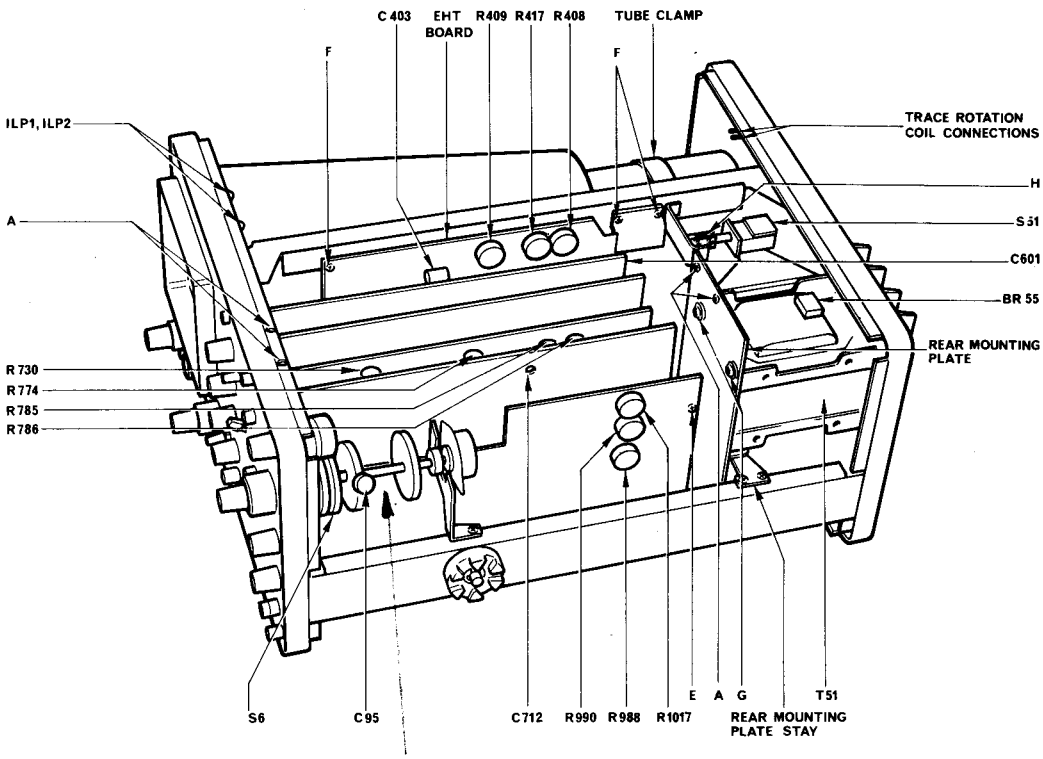


Fig.15 Right hand View

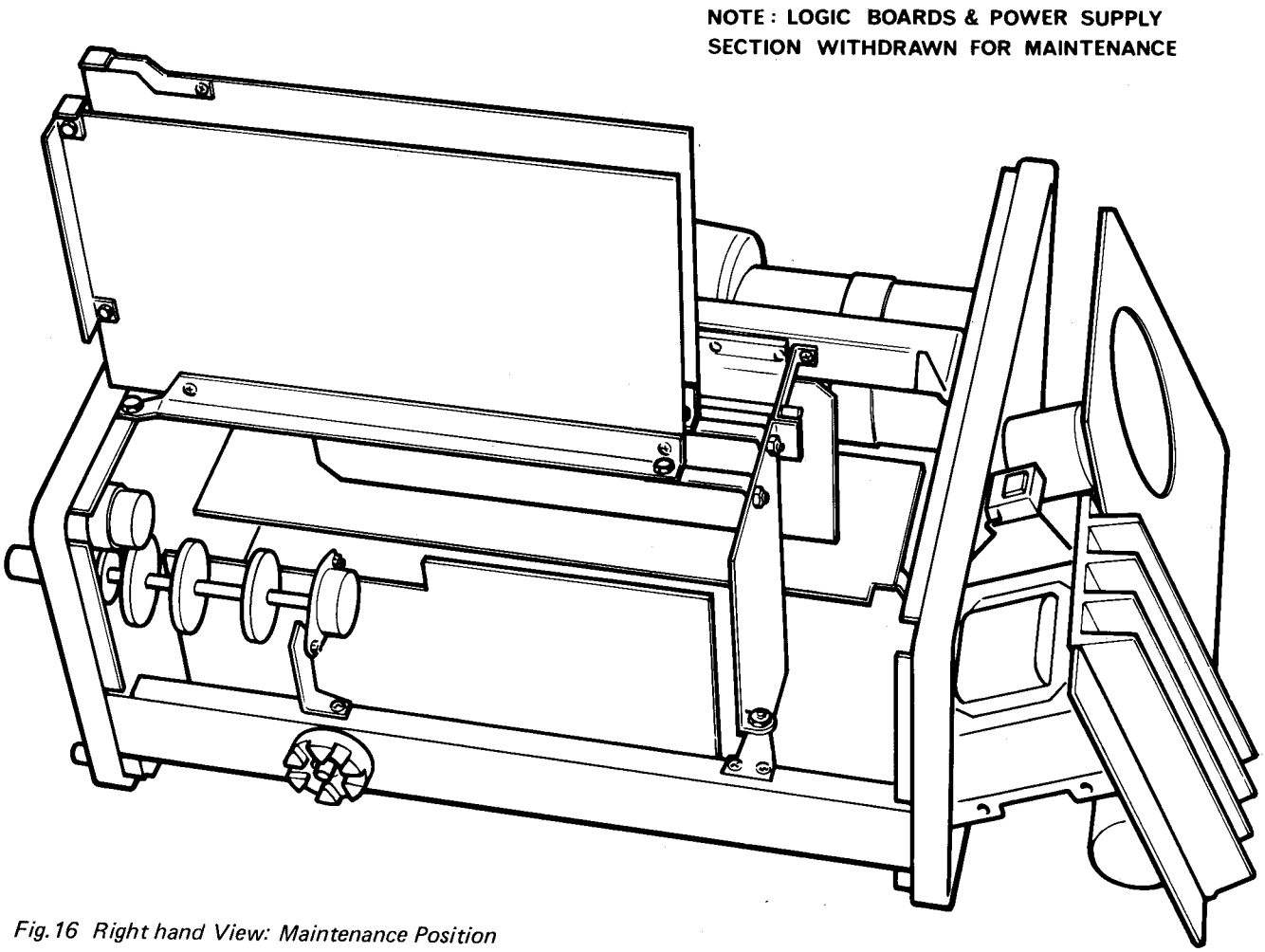


Fig. 16 Right hand View: Maintenance Position

4. The tube may now be pulled back so that the faceplate disengages from the plastic moulding inside the front panel. Lift the front of the tube and remove the connector on the base. Withdraw the tube complete with shield.
5. The tube is a push fit inside the magnetic shield and is removed together with the trace rotation coil, therefore as the tube is withdrawn from the shield the trace rotation coil leads must be fed through the hole in the shield.

5.2.4 ANALOGUE TO DIGITAL CONVERTOR ASSEMBLY

Access to the trackside of the A.D.C. board is best achieved by removing the tube as described in section 5.2.3. If the board must be removed it is taken out together with the Y attenuators, input coupling switches and shift controls as follows:-

1. Remove the Y attenuator cover by removing the five fixing screws and sliding the cover towards the rear of the instrument to clear the edge of the frame. The cover may then be lifted out.
2. Remove the knobs from the Y attenuators, shift controls and input coupling switches. Remove the nut securing the rotary attenuator switches.
3. Disconnect the 7 power supply leads on the left hand edge of the board. Disconnect the 4 miniature co-axial plugs across the centre of the board, SK.P, Q, R and S, and the 'BIAS' lead. Remove the 'P' clip securing these leads to the pillar on the right hand side of the board. Disconnect the 16 way flat ribbon cable from SK.F on the right hand 'daughter' board.
4. Remove the 5 securing screws marked B in Fig.14. Lift the rear of the board and withdraw it from the instrument.

   Refitting the board is the reverse of the removal procedure, but note that when fitting the securing nut to the attenuator switches, the switch assembly should be held with long-nosed pliers to avoid twisting the switch along its length. The colour code of the power supply leads may be ascertained by inspecting the bottom edge of the power supply board; the two 50 volt supplies marked 'Va' and 'Vb' on the A.D.C. board are interchangeable.

5.2.5 POWER SUPPLY ASSEMBLY

Normal access to the component side of the board is possible by removing the tube, and the trackside of the board is exposed by removing the moulded plastic rear

cover (4 fixing screws). The board may be removed by releasing the two screws securing it to the frame and also the two screws securing the heatsink bar at the edge of the board to the finned heatsink assembly. Alternatively the board may be removed as a complete assembly with the finned heatsink,power transformer, ON/OFF switch and C51 in the following manner:-

1. Remove rear cover.
2. Remove the two screws, marked 'G' in Fig.15, securing the power transformer to the logic assembly mounting plate.
3. Slacken the clamp, marked 'H' in Fig.15, and release the ON/OFF switch actuating rod from the ON/OFF switch.
4. Remove two screws securing the power supply board to the frame on the tube side of the instrument and a further four screws securing the finned heatsink to the frame. Two fixing screws holding the small panel bearing the supply line voltage switch and fuse must also be removed.
5. The rear panel assembly may now be withdrawn sufficiently to replace most of the components: complete separation entails disconnecting the two main cableforms from the power supply board and five leads associated with the c.r.t.
   Refitting is the reverse of removal. Care should be taken to ensure that the insulating shim between the power transformer and the logic assembly mounting plate is correctly positioned and the insulating bushes fitted to the screws 'G' securing these two parts are fitted. The clamp linking the supply switch,S51, to the front panel should be carefully aligned so that the switch operates freely without any tendency to stick.

5.2.6 TIMEBASE

Routine access to the timebase board may be gained by removing the logic boards as detailed in section 5.2.2. The timebase range switch may also be removed (see 3. below) and the board itself may be taken out along with the timebase controls (X shift, timebase range, trigger level, source and coupling and external input socket). Proceed as follows:-

1. Remove the knobs from the 5 rotary controls and the cap from the lever switch.
2. Remove the nut securing the EXT. TRIG.B.N.C. socket and unsolder R91 allowing the socket to be removed.
3. Remove the nut from the bush of the TIME/CM rotary switch. Disconnect the 16 way ribbon cable from the timebase range switch at SK.L on the bottom of the timing logic board, and also the five leads to the time-base board at the pins labelled 9, 10, 0V, 15 and 16. Remove the single fixing screw holding the rear support bracket of the switch to the frame. Withdraw the switch assembly.
4. At the rear of the timebase board, disconnect the 4 power supply leads, the twin ribbon cable to the X plates pins 5 and 6, and remove the fixing screw securing the board to the rear mounting plate (marked 'E' in Fig.15).
5. From underneath the instrument, disconnect and identify the three screened leads to the pins labelled SB, CH1 trig. and CH2 trig. and the single wire to the Line trig. pin. Remove the two bottom fixing screws (marked 'E' in Fig.14). Remove the rear mounting plate stay (see Fig.15). Pull the rear of the board back between the power transformer and the frame side-member until it is possible to disengage the rotary control spindles from their holes in the front panel. The board may now be withdrawn from the instrument.

5.2.7 E.H.T. BOARD

Access to the E.H.T. board is normally obtained by removing the c.r.t. and the two logic boards. If, for some reason, the board itself must be removed, proceed as follows:-

1. Remove the c.r.t. the logic board assembly and the A.D.C. board assembly.
2. Slacken the clamp 'H' (see Fig.15) and withdraw the ON/OFF switch actuating rod through the front panel.
3. Remove the knobs from the SCALE, INTENSITY and FOCUS controls. Remove the small plate in front of the ON/OFF switch. Disconnect all leads.
4. Release the 3 screws marked 'F' in Fig.15, and pull the board towards the rear of the instrument until the control spindles clear the front panel, and remove the board from the instrument.

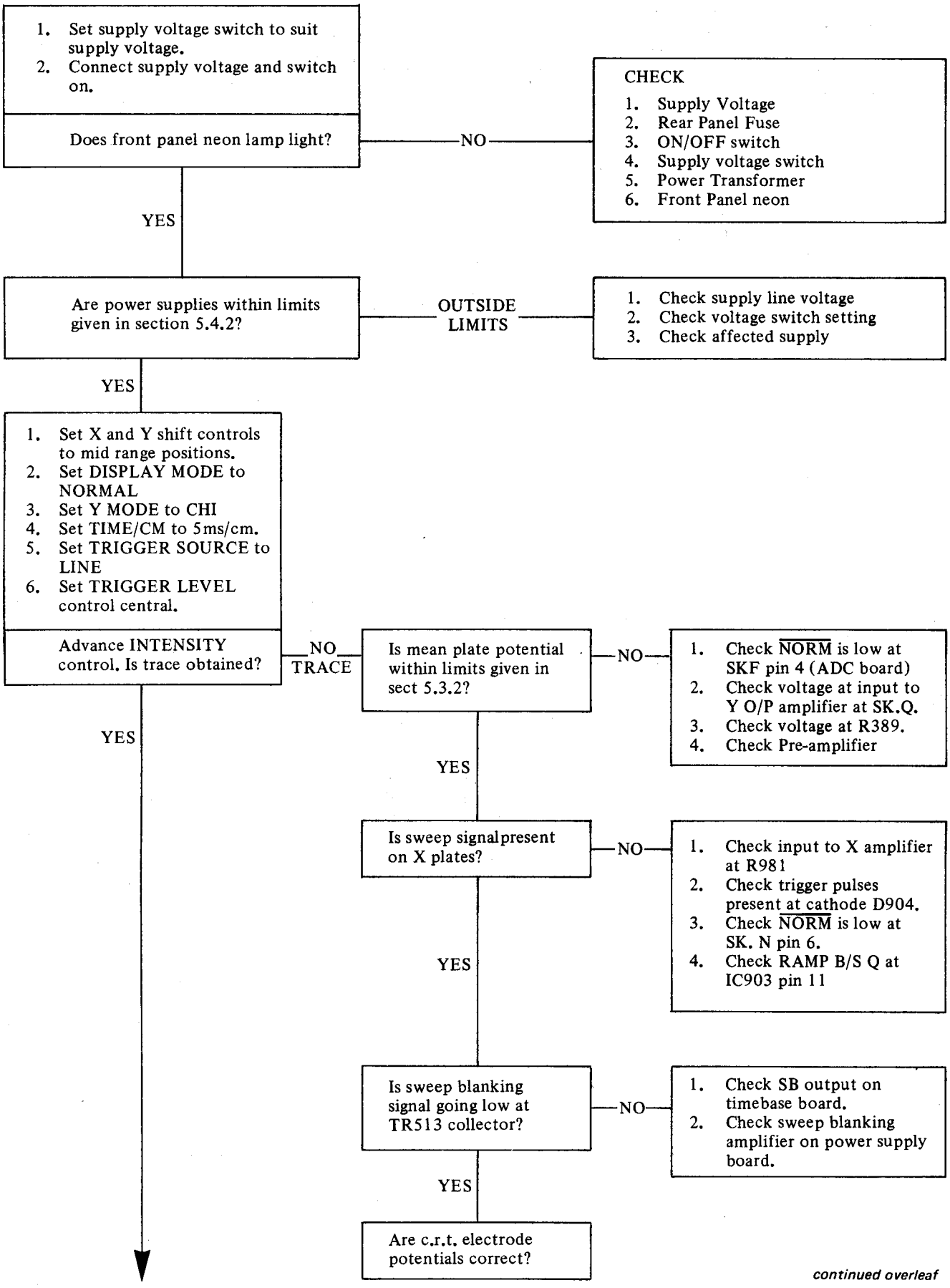
5.3 FAULT FINDING

Faults may be attributed to specific areas of the instrument by following the fault localisation procedure given in section 5.3.1. More detailed examination of the analogue circuitry may be undertaken with the aid of the circuit voltage tables given in section 5.3.2, and the Control Condition Table illustrated in Fig.17 will help to isolate faults in the digital (logic) circuitry.
Certain faults occurring in the digital section of the instrument (in connection with the manipulation of the digitised signal and the addressing of the stores) and also the Analogue to Digital Convertor (A.D.C.) are often characterised by particular distortions of the displayed signal in the REFRESHED and ROLL modes. A logical method of approaching these faults is outlined in section 5.3.3 together with the secondary fault localisation charts for the stored data path (section 5.3.4) and the A.D.C. (section 5.3.5).

	Display Ramp Start	Display Ramp Stop	Read Address Clock	Write Address Clock	L.S.Bit Write Address	L.S.Bit Read Address	Dot Joiner Sample & Hold (S & H) drive	Dot Joiner Time constant (TC) controls A B C D	50% Hold conditions	Special Functions	Y Channel Beam Switch
Normal Mode Single Trace	From Refresh B/S Q	Analogue via TR919	0,909 MHz	—	—	—	—	—	—	Refresh Mode Selected on R's 19/23	—
Normal Mode Dual Trace	"	"	"	—	—	—	—	—	—	—	Ramp B/S Q clocks IC 708 b, on R1/11 (ALT) 2nd stage R.A.C. drives IC 708 b, clear to give chop (R12/18)
Refreshed Mode Ranges 7/23 Single Trace (Released)	From R.A.C. M.S.B. via Delay Circuit	From R.A.C. M.S.B. via Delay Circuit	0,909 MHz from IC 728a, b, via gate IC 707	From Range Divider - See Table for frequency	From Write Address Counter (W.A.C.)	From Read Address Counter (R.A.C.)	P4 Pulse at 0,909 MHz rate via gate IC 732a	0 1 0 1	50% Hold drives L.S.B. Write Address high and sets up Dual Trace conditions for Read Address and Dot joiner (Condition 1)	—	—
					[EXCEPT 50% HOLD]						
Refreshed Mode Ranges 7/23 Dual Trace (Released)	"	"	"	"	"	From B/S IC 723a via gate IC 719	P4 Pulse at 0,455 MHz rate via IC 725a, b, & IC 732a	0 0 1 1	50% Hold drives L.S.B. write address high. (Condition 2)	—	From L.S.B. W.A.C.
Refreshed Mode Range 1/6 Single Trace (Released)	"	Analogue via TR 919	1,818 MHz from PI via IC 720b	1,818 MHz on all 6 ranges	"	From Read Address Counter (R.A.C.)	P4 Pulse at 1,818 MHz rate via IC 725a, b, & IC 732a	1 1 0 0	Condition 1	Write sequence stops read. Then two read sweeps before trigger is enabled	—
					[EXCEPT 50% HOLD]						
Refreshed Mode Ranges 1/6 Dual Trace (Released)	"	"	"	"	"	From B/S IC 723a via gate IC 719	P4 Pulse at 0,909 MHz rate via gate IC 732a	1 0 1 0	Condition 2	"	From L.S.B. W.A.C.
Roll Mode Ranges 7/23 Single Trace (Released)	From Coincidence gate via delay	From Coincidence gate via delay	0,909 MHz from IC 728a, b, via gate IC 707	From Range Divider - See Table for frequency	From Write Address Counter	From Read Address Counter	P4 Pulse at 0,909 MHz rate via gate IC 732a	0 1 0 1	Condition 1	—	—
					[EXCEPT 50% HOLD]						
Roll Mode Range 7/23 Dual Trace (Released)	"	"	"	"	"	From B/S IC 723a via gate IC 719	P4 Pulse at 0,455 MHz rate via IC 725a, b, & IC 732a	0 0 1 1	Condition 2	—	From L.S.B. W.A.C.
Roll Mode Range 1/6 Single Trace (Released)	From M.S.B. R.A.C.	From M.S.B. R.A.C.	1,818 MHz from PI via IC 720b	1,818 MHz on all 6 ranges	"	From RAC	1,818 MHz rate via gate IC 732a	1 1 0 0	Condition 1	Displayed information is set by W.A.C. until "STORE" Condition is reached when R.A.C. addresses store.	—
					[EXCEPT 50% HOLD]						
Roll Mode Range 1/6 Dual Trace (Released)	"	"	"	"	"	From B/S IC 723a via gate IC 719	0,909 MHz rate via gate IC 732a	1 0 1 0	Condition 2	"	From L.S.B. W.A.C.

Fig. 17 Control Condition Table

SECTION 5.3.1 FAULT LOCALISATION PROCEDURE



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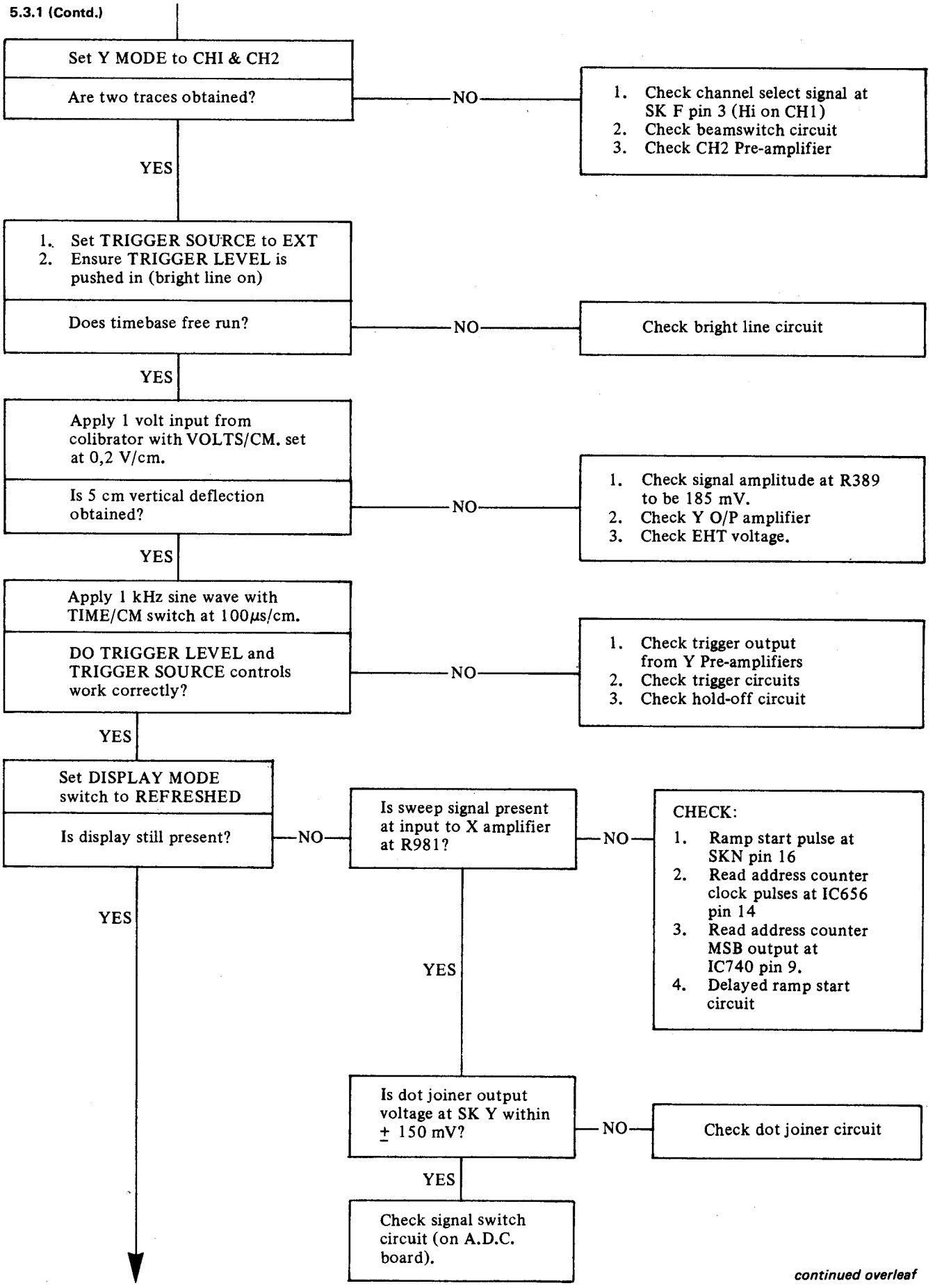
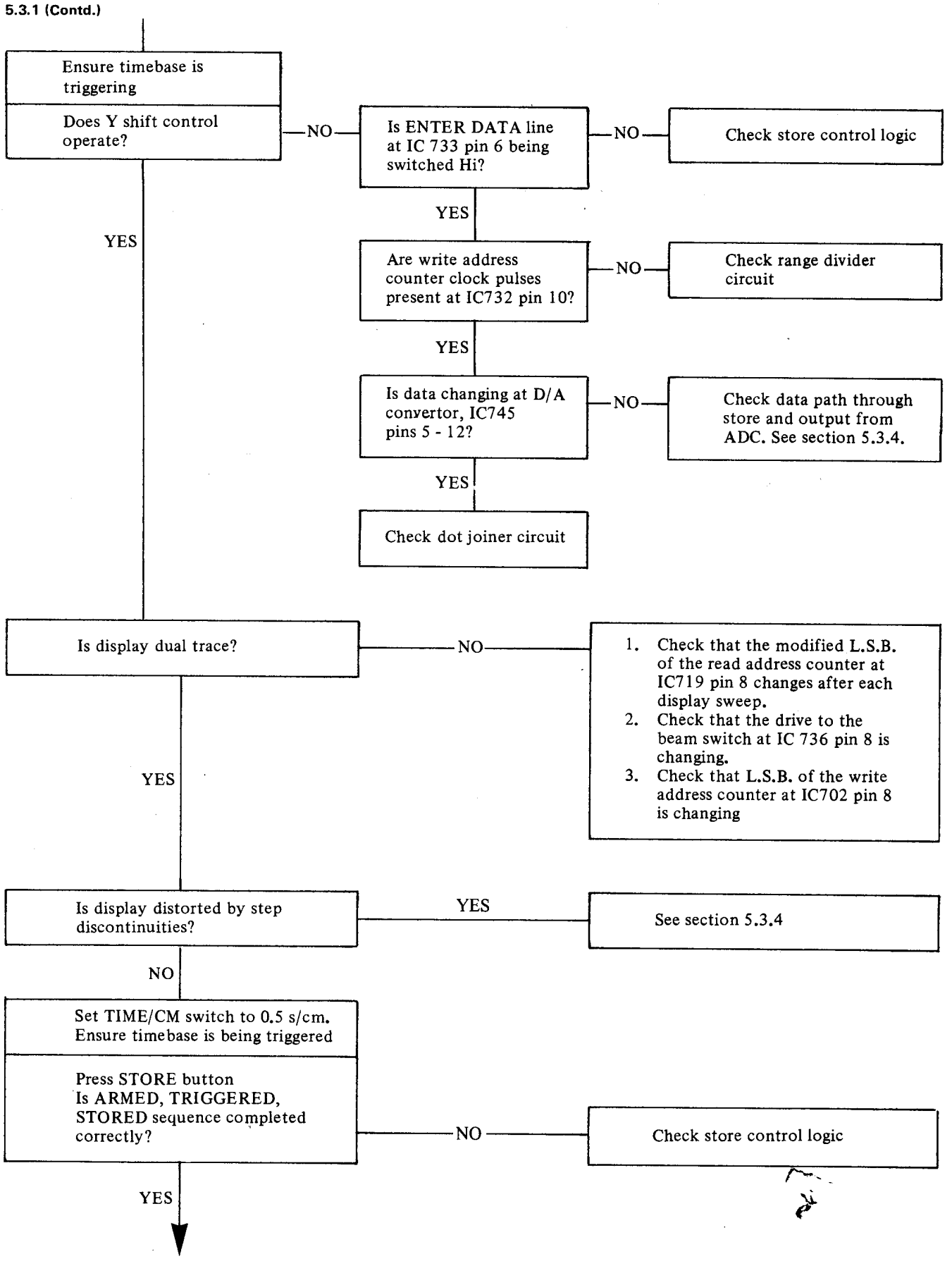
5.3.1 (Contd.)



continued overleaf

5.3.1 (Contd.)



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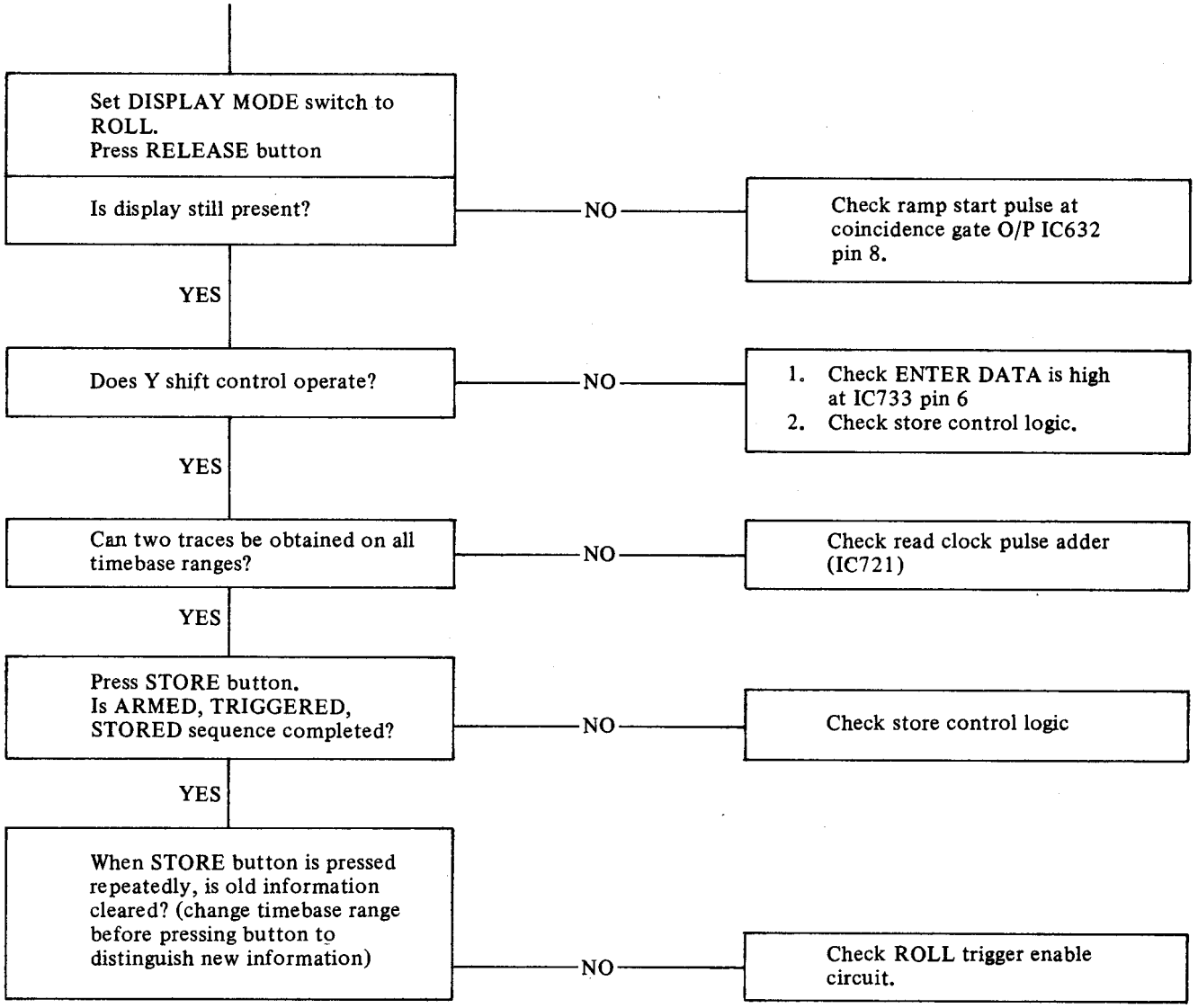
5.3.1 (Contd.)


Set DISPLAY MODE switch to ROLL.
Press RELEASE button
Is display still present?
NO
Check ramp start pulse at coincidence gate O/P IC632 pin 8.
YES
Does Y shift control operate?
NO
1. Check ENTER DATA is high at IC733 pin 6
2. Check store control logic.
YES
Can two traces be obtained on all timebase ranges?
NO
Check read clock pulse adder (IC721)
YES
Press STORE button.
Is ARMED, TRIGGERED, STORED sequence completed?
NO
Check store control logic
YES
When STORE button is pressed repeatedly, is old information cleared? (change timebase range before pressing button to distinguish new information)
NO
Check ROLL trigger enable circuit.

5.3.2 CIRCUIT VOLTAGES

The following voltages may be used as a general guide during faultfinding. All voltages are measured with respect to ground (chassis) with a high input impedence instrument with the supply line voltage at the nominal value set on the SUPPLY VOLTAGE switch. The readings are taken with the front panel controls set as follows unless otherwise indicated:-

INTENSITY, X SHIFT and both Y SHIFT CONTROLS at mid position.
CH1 and CH2 input coupling switches in GND position.
DISPLAY MODE in NORMAL position.
Y MODE in CH1 position.
TIME/CM. at 1ms/cm.
X EXPAND in X1 position (fully anti-clockwise).
TRIGGER LEVEL mid position.
BRIGHT LINE OFF.
TRIGGER SOURCE in EXT. position.

Y Pre-Amplifier

D301 Anode	– 7.2V
D302 Cathode	+ 7.2V
TR301 Drain	+ 10V
TR301 Source	+ 1.5V
TR303 Collector	0V
TR303 Base	– 9.2V
TR302 Drain	– 9.8V
TR302 Source	– 18.5V
TR305 emitter	– 0.7V
TR306 emitter	– 0.7V
TR307, TR308 collectors	+ 5.8V
TR309 collector	0V
TR310 collector	+ 4.2V

Y Output Amplifier

TR408, TR409 bases	+ 0.7V
TR408 collector	+ 5.1V
TR409 collector	+ 4.5V
TR406, TR407 bases	+ 16V
TR406, TR407 collectors	+ 17.5V
TR404, TR405 bases	+ 19.8V
TR404, TR405 collectors (Y plate mean potential)	+ 109V

Beamswitch and Signal Switch

TR319 collector	+ 1.9V CH1 selected + 0.1V CH2 selected
TR321 base	0V
D317, D318 Anodes	+ 1.4V (– 0.6V in REFRESHED mode)
D319, D320 Anode	–0.6V (+ 1.4V in REFRESHED mode)
D323 Anode	– 6.4V

ADC: Scaling Amplifier

TR201 base	0V
TR202 collector	+ 6.5V
TR203 collector	+ 2.8V
TR204 base	0V
D204 Anode	– 6.5V
TR206 base	+ 2V
TR206 collector	+ 5.1V

ADC: Sample and Hold

D208 Anode	– 12.2V
TR213 Gate	+ 1.4V
TR213 Source	+ 2.9V
TR214 Drain	+ 1.4V
TR214 Source	– 4.5V

ADC: Summing Amplifier

IC102 pin 2	+ 2V
IC102 pin 1	+ 10.6V
IC102 pin 12	– 1.7V

ADC: Current Sources

IC101 pin 3		+ 3.7V
IC101 pin 4		+ 7V
IC101 pin 1		+ 5.3V
TR134 base		+ 3.9V (D1 high)
	or	+ 0.1V (D1 low)
TR134 collector		+ 4.7V (D1 high)
	or	+ 6.1V (D1 low)
TR135 collector		+ 6.0V (D1 high)
	or	+ 5.4V (D1 low)
TR232 emitter		+ 10.7V

Timebase

TR914 base	0V
TR915, TR916 collectors	+ 5.5V
TR901, TR902 collectors	+ 14V
TR903 collector	+ 18V
TR904 base	+ 13.7V
TR904 collector	+ 15.6V
TR905 collector	– 19.4V (– 20.6 when triggered)
TR909 base	– 1.8V (+ 0.8 when triggered)
TR912 base	+ 0.8V (– 3.4V when triggered)
TR912 collector	+ 0.2V (+18V when triggered)
TR913 collector	+ 13.2V (+ 0.2V when triggered)
TR924 base	+ 0.6V (plus 11.4V positive going ramp during sweep)
TR924 collector	– 4.4V (plus 6V negative going ramp during sweep)
Junction R998/R983	– 12.2V
TR927 emitter	+ 6.4V
TR925, TR926 collectors (X plate mean potential)	+ 85V

Logic Levels

Inputs: Logic '0' (max.)	+ 0.8V
Logic '1' (min.)	+ 2V
Outputs: Logic '0' (max.)	+ 0.4V
Logic '1' (min.)	+ 2.4V
Typical Levels: Logic '0'	+ 0.2V
Logic '1'	+ 4V

5.3.3 DATA FAULTS

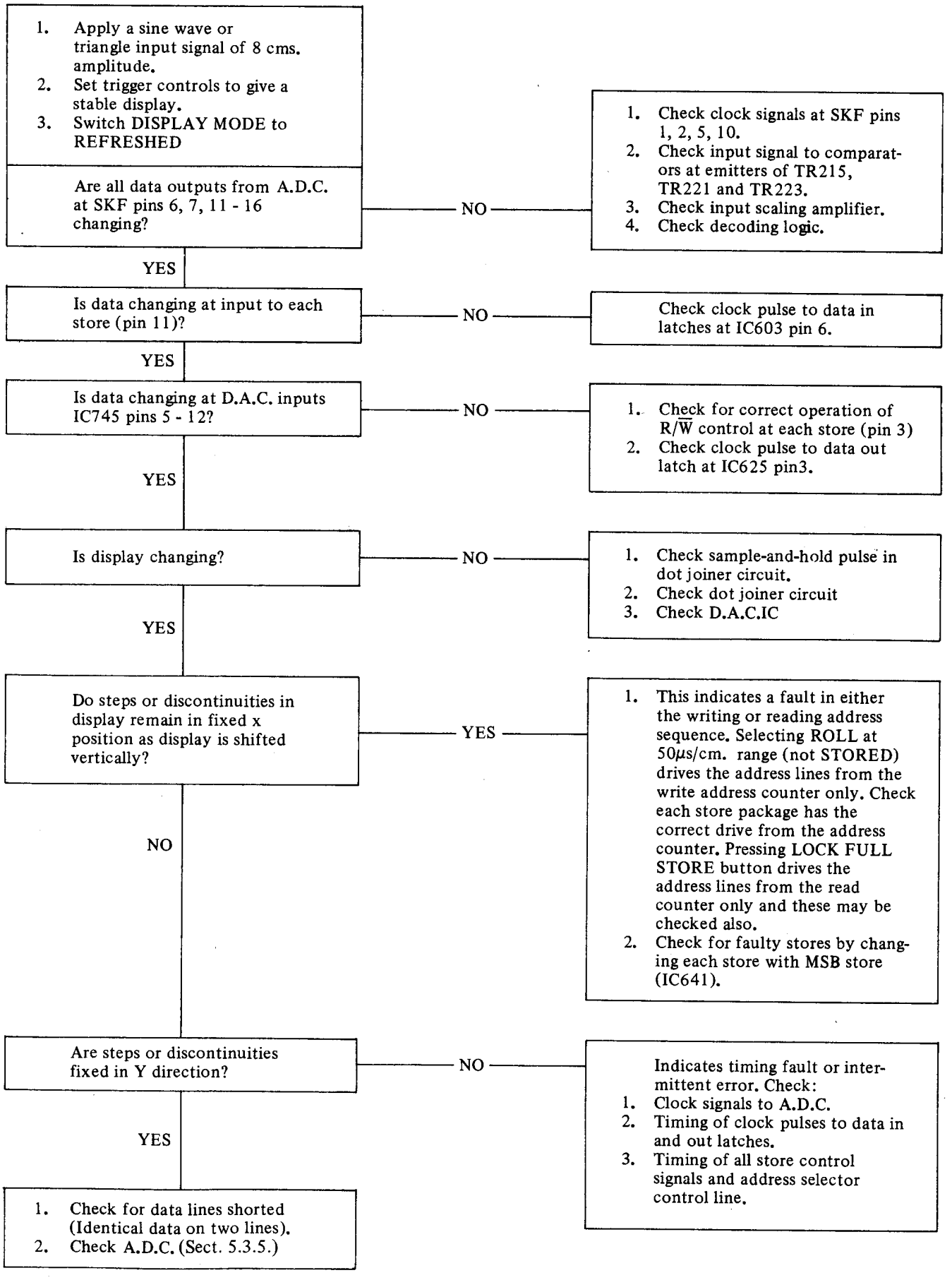
When tracing faults which cause gross distortions (steps, discontinuities, etc.) of the display in the REFRESHED and ROLL modes, it is helpful to distinguish between three cases:

1. Addressing errors. These will occur at particular positions across the screen in the X direction regardless of the setting of the vertical shift controls.
2. Data errors. These will occur at specific positions up the screen in the Y direction regardless of the Y shift control.
3. Timing errors. These will usually be spikes or notches occurring in a fairly random fashion, but often affected by the timebase range switch and the store controls, interaction between the traces may also occur.
   Address lines may be verified by checking for a true binary sequence, that is, by ensuring each bit is changing at twice the frequency of the next most significant bit. This may be done at the address inputs of the stores by switching to the ROLL mode with the timebase range switch at 50μs/cm. In this condition the stores are continuously addressed by the write address counter only. Pressing the LOCK FULL STORE push-button selects the read address counter only.

The eight data lines may be checked from the output of the analogue to digital convertor at SK.F, through the 'data in' latches, IC618 and IC619, the eight store packages, 'data out' latches IC650 and IC659, to the digital inputs of the digital to analogue convertor, IC745. Note that the sense of the data is inverted after the input latches. If a triangle or sawtooth (as obtained from an oscilloscope ramp output for example) waveform is used as an input signal, the data will approximate to a binary sequence as with the address counters, and may be easily verified. With the instrument in the ROLL and the time-base set fo 100μs/cm., the read and write address counters will be running at the same rate, so that the data output rate from the store will be the same as the data input rate, thus simplifying checking. Note that even in this condition, however, the output data cannot be compared directly with the input data since the relative timing between the two (due to the time that the data is held in the store before being read out) will be arbitrary.

Timing errors must be found by checking the various clockpulses and control signals around the store and A.D.C. against the timing diagrams given in this section and also the circuit description section. When inspecting fast pulses, a fast rise-time oscilloscope must be used (say better than 10ns) together with an appropriate low capacitance probe and earth lead. The logic devices used are from the well known 'T.T.L.' (Transistor-Transistor Logic) family and typical propagation delays for each type of device may be obtained from manufacturer data sheets.

5.3.4 CHECKING DATA PATH



5.3.5 ANALOGUE TO DIGITAL CONVERTOR FAULTS

With the DISPLAY MODE set to REFRESHED apply a sine wave or triangle input signal. Set the amplitude and trigger controls so that a single half cycle of the input signal is displayed from positive peak to negative peak as in fig 18 a/

Is signal correct at the emitter of TR215? This should be inverted in sense and at approx. 3.7 volts peak amplitude for full screen deflection.

INCORRECT AMPLITUDE OR DISTORTED WAVEFORM

1. Check scaling amplifier circuit and adjustment.
2. Check sample and Hold circuit.

YES

Are first two data bits (D1, D2) changing in correct manner? (see fig 19 b & c).

NO

1. Check comparators
2. Check reference voltages
3. Check decoding logic

YES

Is signal waveform at emitter of TR221 correct? (see fig 19d).

NO

1. Check first two switched current sources, TR136 and TR139.
2. Check first summing amplifier.

YES

Are data bits D3, D4, D5 correct? (see fig 19e, f & g)

NO

1. Check comparators
2. Check second row reference voltages.
3. Check decoding logic.

YES

Is signal waveform at emitter of TR223 correct? (see fig 19h)

NO

1. Check remaining three switched current sources, TR144, TR147 and TR 150.
2. Check second summing amplifier.

YES

Are data bits D6, D7, D8 changing?

NO

1. Check third row comparators.
2. Check third row reference voltage chain
3. Check decoding logic

YES

Are errors (notches) present in the display at fixed Y levels?

YES

Does pattern repeat in each quarter of screen?

NO

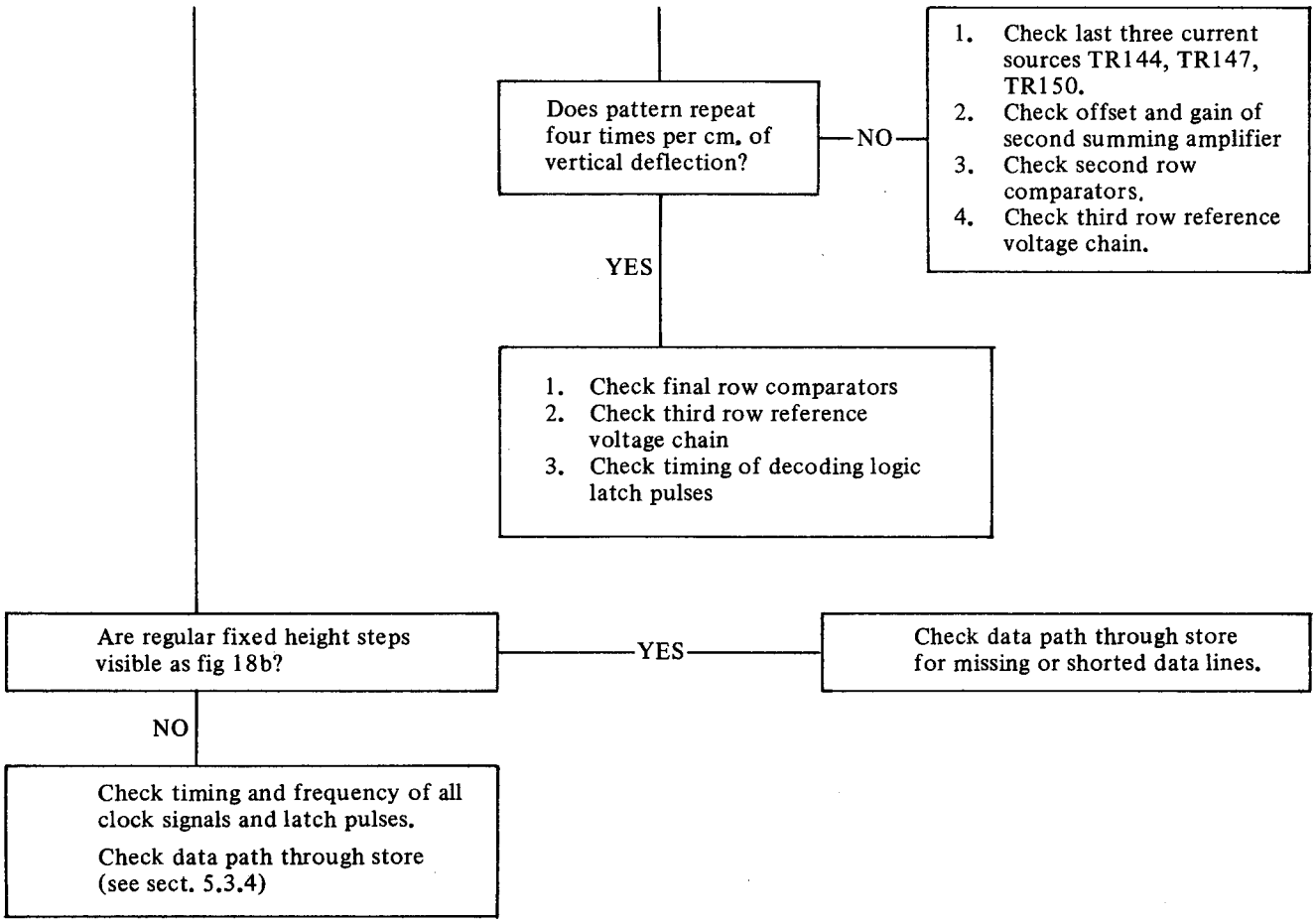
1. Check first two current sources
2. Check offset and gain of first summing amplifier.
3. Check first row comparators.
4. Check second row reference voltage chain.

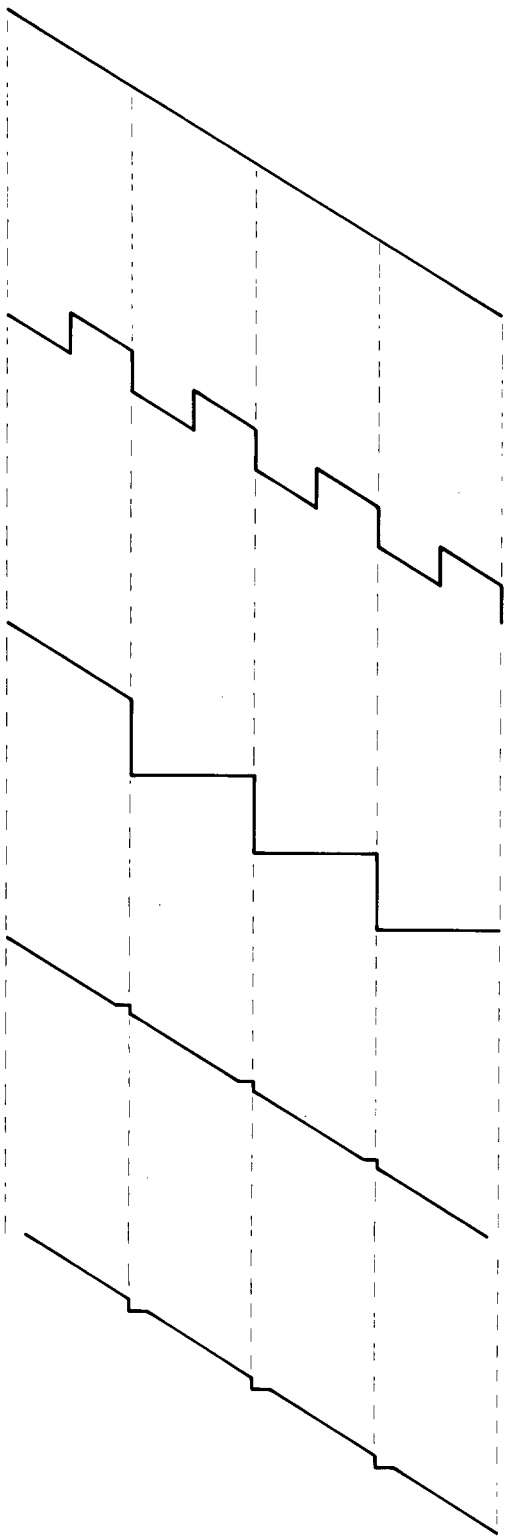
NO

YES

continued overleaf

5.3.5 (Contd.)


Does pattern repeat four times per cm. of vertical deflection?
NO
1. Check last three current sources TR144, TR147, TR150.
2. Check offset and gain of second summing amplifier
3. Check second row comparators.
4. Check third row reference voltage chain.
YES
1. Check final row comparators
2. Check third row reference voltage chain
3. Check timing of decoding logic latch pulses
Are regular fixed height steps visible as fig 18b?
YES
Check data path through store for missing or shorted data lines.
NO
Check timing and frequency of all clock signals and latch pulses.
Check data path through store (see sect. 5.3.4)



A/ INPUT SIGNAL

B/ DATA BIT MISSING

STEP HEIGHT	DATA LINE
4 cms	D1
2 cms	D2
1 cm	D3
5 mm	D4
2.5 mm	D5
1.2 mm	D6
.6 mm	D7
.3 mm	D8

C/ FIRST TWO SWITCHED CURRENT SOURCES IN ADC NOT WORKING (TR136 AND TR139)
OR
FIRST SUMMING AMPLIFIER FAULTY.

D/ Similar faults for remaining three current sources and second summing amplifier but step height 4 times smaller and pattern repeats over each quarter of the screen.

E/ CONVERSION ERRORS DUE TO

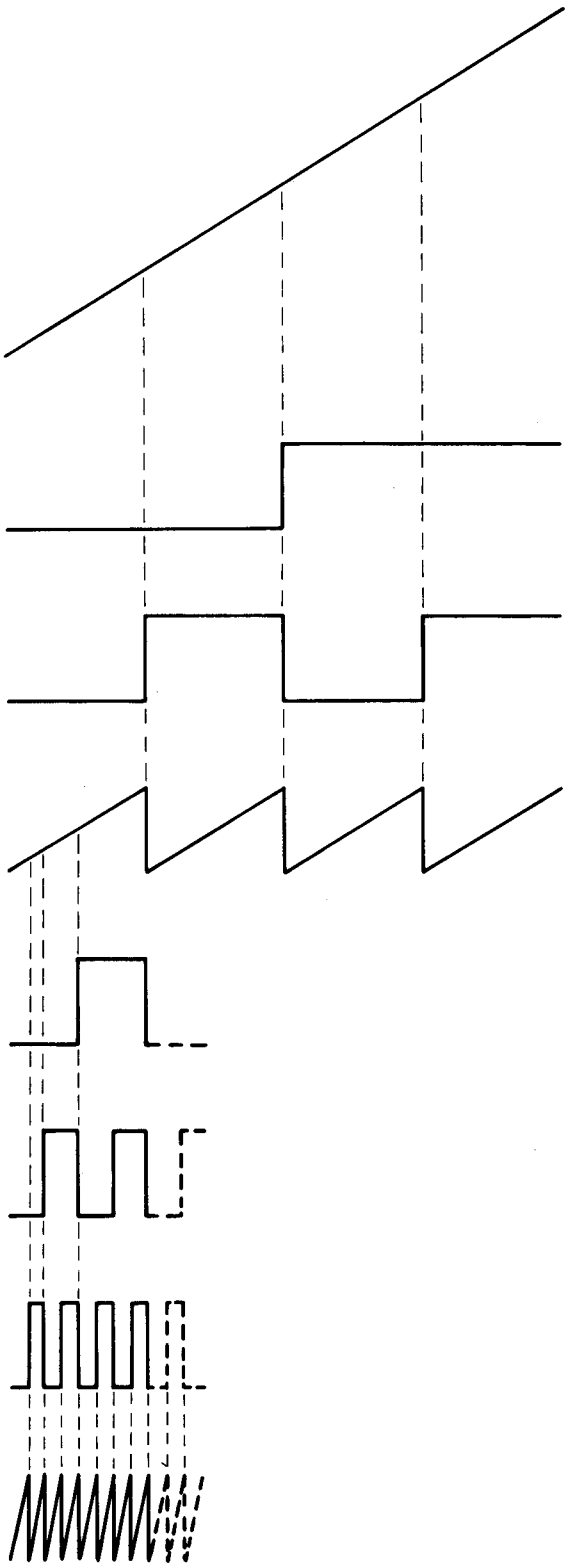
1/ Maladjustment of current sources (R122, R114)

2/ Offsets in first summing amplifiers.

3/ Offsets in first row of comparators.

4/ Timing errors (check clock signal timing)

Fig.18 Data Faults



A/ INPUT SIGNAL AT EMITTER OF TR215

B/ D1 OUTPUT (SK.F PIN. 16)

C/ D2 OUTPUT (SK.F PIN. 15)

D/ WAVEFORM AT EMITTER OF TR221 OUTPUT OF FIRST SUMMING AMPLIFIER

E/ D3 OUTPUT (SK.F PIN 14)

F/ D4 OUTPUT (SK.F PIN 13)

G/ D5 OUTPUT (SK.F PIN 12)

H/ WAVEFORM AT EMITTER OF TR223 OUTPUT OF SECOND SUMMING AMPLIFIER

Fig. 19 ADC Waveforms

5.4 CALIBRATION PROCEDURE

The calibration procedure is detailed below. Note that any calibration adjustments found necessary must not be made until a 15 minute warm-up period has elapsed. The locations of the various preset components are shown in Figs.14 and 15.

5.4.1 TEST EQUIPMENT REQUIRED

1. Multimeter to measure up to 1500 volts with better than 20kΩ per volt impedence. Accuracy to be within ± 2%.
2. Variable Autotransformer (Variac, etc.) Output voltage range 200 – 270 volts at 1A with a.c. r.m.s. voltmeter.
3. Function Generator with frequency range of 0.1Hz to 10kHz, preferably with sawtooth output.
4. Digital Voltmeter with 3½ digit display and 1mV basic resolution. Accuracy to be within ± 0.2%.
5. Source of Time and Voltage Calibration signals, to cover the range 0.1μs – 0.5s. and 25mV – 100V.
6. Square-wave generator to provide 500kHz flat top square wave with amplitude adjustable between 25mV and 1 volt. Risetime to be less than 5ns.
7. Constant amplitude r.f. sine-wave generator to cover the range 500kHz to 15MHz with a 50kHz reference frequency. Output amplitude 25mV to 5 volts pk-pk when terminated with 50Ω load. Amplitude accuracy over the frequency range to be within ± 3%.
8. Capacitance standardiser. 1MΩ/28pF with B.N.C. connections.
9. 50Ω B.N.C. through-termination.
10. E.H.T. meter to measure 3kV.
11. Frequency Counter to measure 1kHz at 1 volt.

5.4.2 POWER SUPPLY VOLTAGES

1. Set the INTENSITY control to minimum.
2. Set the SUPPLY VOLTAGE switch on the rear panel to suit the available supply. Using the autotransformer, set the supply to the instrument to within ± 1% of the selected nominal voltage.
3. Check that the POWER neon, N51, is lit and that the SCALE control varies the graticule illumination.
4. Check the voltages with respect to the chassis at the pins on the lower edge of the power supply board as follows:-

pin	limits min.	voltage max.
+5	5.0	5.5
–20	–19	–21
–6	–5.5	–6.5
+12	11.4	12.6
+20	19	21
+170	155	185

5. Measure the voltage across C402 (see Fig.15) on the E.H.T. board and adjust R409 (SET E.H.T.) to bring this to 185V with the supply voltage adjusted as in 2. above.
6. Measure the voltage at the – 1kV pin on the E.H.T. board (near C403). This voltage should be between – 950V and – 1050V with respect to the chassis, check that it does not vary by more than 10V when the supply voltage to the instrument is varied by ± 10% of the nominal voltage selected with the SUPPLY VOLTAGE switch.
7. Check that the voltage on the '+ 3kV' pin at the rear of the E.H.T. board (to which the cable from the c.r.t. cavity cap connector is fitted), is greater than 2.5kV relative to chassis.

5.4.3 GEOMETRY

1. Set the MODE switch to NORMAL, the TIME/CM. switch to 1ms/cm. and ensure the TRIGGER LEVEL control is pushed in ('Bright Line' position). With the INTENSITY control advanced approximately half way and the Y MODE switch in the CH1 and CH2 position, obtain two traces on the screen.
2. Adjust the FOCUS control in conjunction with R417 ('ASTIG') on the E.H.T. board to obtain clear traces.
3. Adjust the TRACE ROTATION control, R529, on the rear panel to align the traces with the horizontal graticule lines.
4. Apply a 1kHz sinewave to one channel and adjust the sensitivity and triggering controls to obtain a stable display with an amplitude of 8 cms. pk-pk. Adjust R408 (GEOM) on the E.H.T. board for minimum distortion of the display in both X and Y axes. Reset the FOCUS and ASTIG controls to optimise the trace quality.

5.4.4 Y CALIBRATION AND SHIFT RANGE

1. With the input coupling switch in the GND position select CH1 on the Y MODE switch and adjust the front panel BALance control, R373, so that there is no trace shift when changing from the 0.2V/cm range to the 0.5V/cm. range. Adjust R369 (VAR BAL) on the A.D.C. board so that there is no shift when the CH1 variable sensitivity control is operated.
2. Repeat the preceding step for CH2 using R374 (BAL) and R370 (VAR BAL).
3. With CH1 and CH2 selected set the two Y shift pots, R1 and R2, so that the wipers (measured at the pins marked 'SH' on the front of the A.D.C. board) are at + 4V with respect to chassis. Adjust R377 (SHIFT CENTRE) so that the two traces are equally spaced each side of the central horizontal graticule lines.
4. Apply a sinewave signal to each channel in turn and set the amplitude for 8cm. pk-pk display. Check that the traces can be shifted completely off the screen in each direction.
5. With CH1 only selected, set the attenuator switch to 20mV/cm. and apply a 100mV., 1kHz square wave signal from the calibrator. Monitor the signal voltage at the junction of R389 and D316 cathode on the A.D.C. board with an oscilloscope. Adjust ~~R320~~ R319 on the CH1 pre-amplifier board to set the signal level to 185mV. Repeat the procedure on CH2.
6. With a 100mV signal still applied on the 20mV/cm. range, set R438 (in the centre of the E.H.T. board) for 5cms display. Check calibration of other channel.

5.4.5 ATTENUATOR COMPENSATION

1. Check that attenuator cover is fitted.
2. Set CH1 attenuator switch to 0.2V/cm. and apply a 2V, 1kHz square wave via a 1MΩ/28 pF standardiser.. Adjust C301 for a square corner to the display. Repeat procedure with CH2 adjusting C302.
3. Set CH1 attenuator to 0.5V/cm. and apply a 2.5V, 1kHz square wave direct. Adjust C305 for a square corner to the display. Repeat step with CH2 adjusting C306.
4. With CH1 attenuator still set at 0.5V/cm. apply a 5V, 1kHz square wave via the standardiser and adjust C303 for a square corner. Repeat step with CH2 adjusting C304.
5. Remove standardiser and check all attenuator ranges applying the appropriate amplitude, to ensure all ranges give a square corner to the applied waveform and are accurate in amplitude to within ± 3%.

5.4.6 TIMEBASE CALIBRATION

1. Set TIME/CM. control to 1ms/cm. and X EXPAND control to X10 (fully clockwise position). Apply 1ms. markers to CH1, adjusting Y sensitivity to give approximately 3cm amplitude, triggering with bright line off (TRIGGER LEVEL control pulled out). Adjust R990 (SET x 10) on the timebase board for exactly 10cms. between markers.
2. Set X EXPAND to X1 (fully counter clockwise) and adjust R988 (SET X1) on timebase board for 1cm. between markers.
3. With 1ms. markers still applied, vary the supply voltage to the instrument by ± 10% from the nominal value and check that there is less than ± 1% change in timebase calibration.
4. Set TIME/CM to 10μs/cm. and apply 10μs markers. Adjust the trimmer, C95, on the timebase range switch for 1cm. between markers.
5. Set TIME/CM to 1μs/cm and apply 0.1μs markers with the X EXPAND control in the X10 position. Using the X shift control, ensure that the calibration of the first 10cms. of trace and the middle 10cms. of the trace are within ± 4%.
6. With the X EXPAND control at X1, check all the timebase ranges from 1μs/cm to 0.5s/cm, with the appropriate markers, to within ± 3%. Check that the REFRESHED mode is automatically selected on ranges below 0.5s/cm.
7. Check that the trace length is greater than 11 cms. on all timebase ranges.
8. Move DISPLAY MODE switch to REFRESHED. Select 1ms/cm. range and apply 1ms. markers. Check accuracy is within ± 3%. Check that the trace length increases when switching from REFRESHED to NORMAL. This increase should be approximately 0.5cm and can be varied by R973.

5.4.7 TRIGGER BALANCE

1. With the DISPLAY MODE switch in the NORMAL position and no trigger signals applied, check that the timebase free runs with the BRIGHT LINE on and does not free run with the BRIGHT LINE off.
2. Apply a 1kHz sine wave and adjust amplitude to give approximately 6cms. display. Adjust R1012 on the timebase board (below the timebase range switch, S6) so that there is no vertical shift in the trigger point when moving the TRIGGER SOURCE control between + and −. Check that the TRIGGER LEVEL is midway through its range when the timebase is triggering at the zero crossing point on the displayed waveform.
3. With the signal applied to CH1 input, adjust R1011 on the timebase board so that there is no change in trigger point when the TRIG. COUPLING switch is moved from AC to DC. Repeat this adjustment with R1009 for CH2.
4. Check that the LF and HF REJECT positions of the TRIG. COUPLING switch are functional.
5. Apply a 1kHz square wave input signal and reduce the amplitude to 2mm. Check that stable triggering can be obtained on both + and − slope positions for both input channels.
6. Set the TRIG SOURCE selector to EXT. and apply a 1 volt, 1kHz square wave to the EXT TRIG input. Check that stable triggering can be obtained on both + and − slope settings with the BRIGHT LINE either on or off.
7. Check the LINE trigger facility is functional and that the l.e.d. lamp associated with the TRIGGER LEVEL control is working.

5.4.8 INTERNAL CALIBRATOR

Set the pk-pk amplitude of the 1V calibrator output using R1017 on the timebase board (SET CAL). Check the 0.1V output is accurate within ± 2%.

5.4.9 Y PULSE RESPONSE

1. With the CH1 attenuator set at 20mV/cm. apply a fast risetime 500kHz flat topped square wave to CH1, using a 50Ω termination to prevent cable reflections. Adjust amplitude for a 5cm. display and set C419 and C424 on the E.H.T. board for a square corner with less than 1% undershoot or overshoot. Check CH2 at the same sensitivity.
2. Set the Y attenuators to 5mV/cm. and apply a signal from the constant amplitude r.f. generator. Set the signal amplitude at 50kHz to give 5cm. display and then increase the input frequency until the display height falls to 3.5cm. This frequency should be greater than 11MHz. Repeat this procedure with CH2.
3. Apply the 500kHz square wave and check the pulse response on all attenuator ranges with 5cms. display. Both channels must exhibit less than 2% undershoot or overshoot on any range.

5.4.10 H.F. TRIGGER

Apply a 10MHz sine wave to CH1 and adjust amplitude for 1cm. of display on the 20mV/cm. attenuator range. Check that steady triggering can be obtained with the BRIGHT LINE switched off. Switch the attenuator to 0.1V/cm. to give 2mm. display and reduce the input frequency to 2MHz. Check for stable triggering and repeat both tests on CH2.

Method used at Gould.
Apply 10KHz sine wave L.F Rej gain leading edge.
H.F Rej lose " "

Although it states ±1% don't forget the inst.. acc.. is only ±3%

Use Tek. PG. 506, this is what they use at Gould, high amp.. @ 500KHz for ranges 5mV to 1V

5.4.11 CLOCK OSCILLATOR FREQUENCY

Set the TIME/CM control to 1ms/cm., and connect the output of the internal CALibrator to a frequency counter and adjust C601 at the rear of the store logic board to obtain a reading of 890Hz within ± 1%. If a counter is not available, monitor the calibrator on CH1 with the NORMAL mode selected and adjust C601 for 8 complete cycles in 9cms.

5.4.12 ANALOGUE TO DIGITAL CONVERTOR

1. Measure the voltage across the pins of the A.O.T. resistor, R163, on the A.D.C. board with a d.v.m. Adjust R106 on the current source board to bring this voltage to 2.80V.
2. Measure the voltage across the pins of A.O.T. resistor R289. Adjust R124 on the current source board to bring this voltage to 0.817V.
3. With the DISPLAY MODE switch in the REFRESHED position apply a triangle or sine wave input signal and set the amplitude for a display of 8cms. Adjust the timebase and trigger controls so that one half cycle is displayed from the positive peak to the negative peak. Ensure that the l.e.d. associated with the TRIGGER LEVEL control is lit.
4. Adjust R122 to minimise conversion errors (notches) at the ¾ scale point (i.e. at approx. 2cms. above the graticule centre line) on the display.
5. Adjust R114 to minimise conversion errors occuring at the ¼ and ½ scale points. Errors at these points will also be affected by R122. If the conversion errors cannot be entirely removed by these two adjustments, it may be necessary to fit a resistor of between 10kΩ and 27kΩ in value, in the position marked R163. Similarly, if there are regular groups of errors occurring in each quarter of the screen, a resistor of value 3k9 to 12kΩ may be fitted in the position marked R289. It is emphasised that these adjustments should only be used for correcting SMALL conversion errors: large errors in the displayed signal should be investigated as described in the Faultfinding Procedure (section 5.3).

5.4.13 DIGITAL TO ANALOGUE CONVERTOR

The range of the D.A.C. must be set up such that the trace can just be deflected off the screen (approx. 9cms). Proceed as follows:-

1. Set the DISPLAY MODE switch to ROLL and remove the input signal. Rotate the Y shift control fully counter clockwise to deflect the trace to its lower limit and adjust R774 on the Timing Logic board to position the trace on the lower graticule line.
2. Apply a 100mV square wave to CH1 input and set the CH1 attenuator switch to 20mV/cm. Adjust the Y shift control to obtain a 0.5cm. display and then re-adjust R774 to position the top of the displayed waveform on the lower graticule line.
3. Rotate the shift control fully clockwise and use R730 to position the trace on the top graticule line. Reset the shift control to display a 0.5cm. amplitude trace as before and re-adjust R730 to set the lower edge of the display on the top graticule line.

5.4.14 SCALING AMPLIFIER

With a 5cm. square wave displayed in the NORMAL mode, set R208 on the A.D.C. board to give no change in amplitude when switching from NORMAL to REFRESHED modes. Set R217 for no change in vertical position between the two display modes. Ensure that full coverage of the screen can be obtained in the REFRESHED mode.

5.4.15 DOT JOINER

1. Set the DISPLAY MODE switch to REFRESHED and apply a 10kHz square wave. Adjust the amplitude to give a 4cm. display and set the TIME/CM. switch to 5μs/cm. Adjust C712 on the Timing Logic board (accessible through a hole in the screen) to give 'cleanest' trace free from ripples.
2. Set the timebase rate to 20μs/cm. and the Y MODE switch to CH1. Adjust R785 on the Timing Logic board for minimum undershoot or overshoot on the displayed waveform.
3. Set the timebase range to 0.1ms/cm. and the X EXPAND control for approximately X5 expansion. Set C713 for a square corner.
4. Switch the Y MODE control to CH1 and CH2 and adjust R786 for a square corner.

5.4.16 FUNCTIONAL CHECKS

Check all timebase ranges in the REFRESHED mode and ensure that the single shot STORE facility is functioning correctly. Check the operation of the two LOCK STORE pushbuttons in both single and dual trace modes.

5.5 WIRING DETAILS FOR 100V OPERATION

The primary connections come from the transformer as flying leads. The unused blue and white 100V tap leads are normally terminated on pins on the on/off switch mount ing bracket. These must be interchanged with the brown and yellow 115V tap leads, normally wired to the tap switch.

Disconnect the blue and white leads from the pins. Disconnect the thin brown lead from the bottom centre tag of the tap switch and the thin yellow lead from the tag above it. Withdraw these leads upwards from the cable loom and replace them by the blue and white.

Connect the blue lead to the bottom centre tag of the tap switch in place of the brown. Connect the white lead to the tag above, in place of the yellow. Connect the yellow and brown leads to the pins on the on/off switch bracket.

Note that access to the tap switch is improved if the rear panel section is unscrewed from the frame and withdrawn slightly.

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	½W	10%	unless otherwise stated
CF	Carbon Film	⅛W	5%	unless otherwise stated
MO	Metal Oxide	½W	2%	unless otherwise stated
MF	Metal Film	¼W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potentiometer Type MPD, PC		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+ 80% − 25%	
CE(2)	Ceramic	500V	± 10%	unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		± 10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		± 10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (aluminium)		+ 50% − 10%	
T	Tantalum		+ 50% − 10%	

POWER SUPPLIES Y O/P AMPLIFIER AND BLANKING AMPLIFIERS

Ref	Value	Description	Tol %±		Part No.
RESISTORS					
R401	3M3	CF		½W	36002
R402	500	CP			A4/35335
R403	100	CF			21794
R404	100	CF			21794
R405	3M3	CC			1181
R406	4k7	CC			3427
R407	1M5	CC			7016
R408	200k	PCP			39264
R409	10k	PCP			39265
R410	47k	CF			21815
R411	3M3	CF			36002
R412	15k	CF			28727
R413	47k	CF			21815
R414	220k	CF			21823
R415	1M	CC			1171
R416	1M	CP			A4/35337
R417	200k	PCP			39264
R418	270k	CF			32356
R419	220k	CP			A4/35336
R420	560k	CF			32359
R421	10k	CF			21809
R422	2M2	CC			1180
R423	3k	WW			33212
R424	91	CF			28782
R425	47	CF			28714
R426	68	CF			28716
R427	33k	CF			21814
R428	390	CF		1W	19038
R429	91	CF			28782
R430	47	CF			28714
R431	10	CF			21793
R432	3k	MO	5	6W	33212
R433	100	CF			21794
R434	100	CF			21794
R435	68	CF			28716
R436	100	CF			21794
R437	100	CF			21794
R438	220	CP			35877
R439	2k7	CF			28726
R440	2k7	CF			28726
R441	470	CF			21797
R442	470	CF			21797
R443	22	CF			28710
R444	10	CF			21793
R445					
R446					
R447	150	CF			28719
R448	680	CF			28723
R449					
R450	100	CF			21794
R451	10	CF			21793
R501	100k	CF		½W	18574
R502	3k3	CF			21803
R503	3k3	CF			21803

Ref	Value	Description	Tol %±	Part No.
RESISTORS (Contd.)				
R504	5k6	CF		21806
R505	5k6	CF		21806
R506	5k6	CF		21806
R507	6k8	CF		21807
R508	5k6	CF		21806
R509	3k3	CF		21803
R510	1k	CF		21799
R511	3k9	MO		26724
R512	3k3	CF		21803
R513	2k2	CF		21802
R514				
R515	100	CF		21794
R516	3k3	CF		21803
R517	10k	CF		21809
R518	470	CF		21797
R519	820	CF		28724
R520	56	CF		28715
R521	47	CF		28714
R522	OR22	WW	2½W	36159
R523	220	CF		21796
R524	12k	WW		21141
R525	12k	WW		21141
R526	15k	CF	½W	18564
R527	27k	CF	2W	33211
R528	22k	CF	½W	18566
R529	1k	PCP		36080
R530	560	CF	1W	19040
R531				
R532	8k2	CF	½W	18561
R533	1M	CF		31840
R534	2k7	CF		28726
R535	4k7	CF		21805
R536				
R537				
R538	100	CF		21794
R539	100	CF		21794
R540	47	CF	1W	4038
CAPACITORS				
C401	.01μF	CE(2)	250V	22395
C402	1μF	E	350V	29494
C403	4.7μF	E	63V	32195
C404	4μF	E	450V	23599
C405	4μF	E	450V	23599
C406	4μF	E	450V	23599
C407	4μF	E	450V	23599
C408	4μF	E	450V	23599
C409	4μF	E	450V	23599
C410	.01μF	CE(2)	2kV	23603
C411	.01μF	CE(2)	2kV	23603
C412	.01μF	CE(2)	2kV	23603
C413	.01μF	CE(2)	2kV	23603
C414	.047μF	CE(2)	1k5V	36633
C415	0.01μF	PE	5kV	37854
C416	0.01μF	PE	5kV	37854

POWER SUPPLIES, Y O/P AMPLIFIER AND BLANKING AMPLIFIERS (Contd.)

Ref	Value	Description	Tol %±		Part No.
CAPACITORS (Contd.)					
C417	100pF	CE(2)		500V	22376
C418	100pF	CE(2)		500V	22376
C419	12/75pF	TRIMMER			36091
C420	150pF	CE(2)			4514
C421	.15μF	CE(2)		250V	35601
C422	.1μF	CE(2)		30V	19647
C423					
C424	10/40pF	TRIMMER			35506
C425					
C426	39pF	CE(2)		500V	22371
C427	.047μF	CE(2)		12V	19657
C428	.01μF	CE(2)		250V	22395
C429	5.6pF	CE(2)		500V	22361
C430	7.5pF	PS			42102
C431	4700pF	CE(2)		4kV	26863
C432	4700pF	CE(2)		4kV	26863
C433	1μF	PE		160V	31383
C434	.01μF	CE(2)		250V	22395
C435	4700pF	CE(2)		4kV	26863
C502	4700pF	E		16V	36020
C503	.1μF	CE(2)		30V	19647
C504	.1μF	CE(2)		30V	19647
C505	15pF	CE(2)		500V	22366
C506	.02μF	CE(2)		1k5V	25223
C507	.1μF	CE(2)		30V	19647
C508	.1μF	CE(2)		30V	19647
C509a	100μF	E		300V	36023
C509b	100μF				
C510	2200μF	E		40V	36022
C511	2200μF	E		40V	36022
C512	3300μF	E		25V	36021
C513	560pF	CE(2)		500V	22384
C514					
C515	10μF	E		25V	32180
C516	10μF	E		25V	32180
C517	10μF	E		25V	32180
C518	10μF	E		25V	32180
C519	.01μF	CE(2)		250V	22395
C520	10μf	E		25V	32180
C521	.01μF	CE(2)		250V	22395
C522	.01μF	CE(2)		250V	22395
TRANSISTORS					
TR401		2N3053			4039
TR402		BD159			34652
TR403		BC182B			33205
TR404		BF380			32902
TR405		BF380			32902
TR406 } TR407		AE13 Transistor Pair			31254
TR408		2N2369			23307
TR409		2N2369			23307

Ref	Value	Description	Tol %±	Part No.
TRANSISTORS (Contd.)				
TR505		BC212		29327
TR506		BC212		29327
TR507		BC182		33205
TR508		BC182		33205
TR509		2N3053		4039
TR510		2SC1173		36188
TR511				
TR512				
TR513		2N5831		33209
TR514		2N2369		23307
TR515		2N2369		23307
TR516		BC182		33205
DIODES				
D401		IN4007		52337
D402		ZENER	180V	40632
D403		ZENER	180V	40632
D404		IN4007		52337
D405		IN4007		52337
D406		IN4007		52337
D407		SCM30		33249
D408		SCM30		33249
D409		SCM30		33249
D410		IN4007		52337
D411		ZENER	11V	33936
D412		ZENER	10V	33935
D503		ZENER	5V1	33928
D504		ZENER	5V1	33928
D505		ZENER	5V1	33928
D506		ZENER	6V2	28764
D507		IN4148		23802
D508		ZENER	24V	33944
D509		IN4148		23802
INTEGRATED CIRCUITS				
IC501			12V	36178
IC502			6V	36177
IC503			15V	36179
IC504			15V	36185
MISCELLANEOUS				
L401	33μH			33204
L402	33μH			33204
L403				4442
L404				4442
FS501			250mA	32338
BR401		WO4		29367
SKU				36105

CH1 & CH2 PRE-AMPS

Ref	Value	Description	Tol %±	Part No.
RESISTORS				
R301	470	CF		21797
R302	3.3k	CF		18556
R303	470	CF		21797
R304	22k	CF		21812
R305	22k	CF		21812
R306	27k	CF		21813
R307	470	CF		21797
R308	470	CF		21797
R309	6k8	CF		21807
R310	6k8	CF		21807
R311	1k8	CF		28725
R312	1k5	CF		21801
R313	1k5	CF		21801
R314	1k8	CF		28725
R315	47	CF		28714
R316	47	CF		28714
R317	2k2	CF		21802
R318	2k2	CF		21802
R319	100	CP		35878
R320	120	CF		28718
R349	47	CF		28714
R350	47	CF		28714
R351	10k1	MF	½	31928
R352	10k1	MF	½	31928
R353	15k	CF		28727
R354	15k	CF		28727
R355	100	CF		21794
R356				
R357	10	CF		21793
R358	10	CF		21793
R359	56	CF		28715
R360	2k7	CF		28726
R361	10k	CF		21809
R362	2k7	CF		28726
R363	6k8	CF		21807
R364				
R365	5k6	CF		21806
R366	5k6	CF		21806
R367	3k9	CF		21804
R368	3k9	CF		21804
R369	1k	CP		35880
R370	1k	CP		35880
R371	22	CF		28710
R372	22	CF		28710
R373	22k	PCP		A3/35339
R374	22k	PCP		A3/35339
R375	1k	CF		21799
R376	1k	CF		21799
R377	1k	PCP		35880
R378	1k5	CF		21801
R379	47	CF		28714
R380	3k9	CF		21804
R381	47	CF		28714
R382	47	CF		28714
R383	1k5	CF		21801
R384	1k5	CF		21801

Ref	Value	Description	Tol %±	Part No.
RESISTORS (Contd.)				
R385	5k6	CF		21806
R386	5k6	CF		21806
R387	6k8	CF		21807
R388	6k8	CF		21807
R389	330	CF		28721
R390	1k8	CF		28725
R391	1k3	CF		28792
R392	10k	CF		21809
R393	10k	CF		21809
R394	1k1	MO		28791
R395	1k1	MO		28791
R396	390	CF		28722
R397	390	CF		28722
R398	3k9	CF		21804
R399	100	CF		21794
CAPACITORS				
C301	16pF	TRIMMER		32059
C302	16pF	TRIMMER		32059
C303	16pF	TRIMMER		32059
C304	16pF	TRIMMER		32059
C305	6pF	TRIMMER		29421
C306	6pF	TRIMMER		29421
C307	.01µF	CE(2)	250V	22395
C308	.01µF	CE(2)	250V	22395
C309	47pF	CE(2)	500V	22372
C310	.01µF	CE(2)	250V	22395
C311	12pF	CE(2)	500V	22365
C312	22µF	E	25V	32181
C313	15µF	E	63V	32197
C314	15µF	E	63V	32197
C315	120pF	CE(2)	500V	22377
C316	120pF	CE(2)	500V	22377
C317	470pF	CE(2)		11492
C318	470pF	CE(2)		11492
C319	18pF	CE(2)	500V	22367
C320	18pF	CE(2)	500V	22367
C321	1000pF	CE(2)	500V	22387
C322				
C323	1000pF	CE(2)	500V	22387
C324	1000pF	CE(2)	500V	22387
C325	.1µF	CE(2)	30V	19647
C326	.1µF	CE(2)	30V	19647
C327	0.01µF	CE(2)	250V	22395
C328				
C330	27pF	CE(2)	500V	22369
TRANSISTORS				
TR301) TR302)		AE31	Dual Fet	A36243
TR303		BC209C		33331
TR304		BC212		29327
TR305) TR306)		AE13	Matched Pair	A31254
TR307) TR308)		AE13	Matched Pair	A31254

CH1 & CH2 PRE-AMPS (Contd.)

Ref	*Value*	*Description*	*Tol %±*	*Part No.*
TRANSISTORS (Contd.)				
TR309		2N3640		31781
TR310		2N3640		31781
TR315		2N3904		24146
TR316		2N3904		24146
TR317		2N3906		21533
TR318		2N3906		21533
TR319		2N3640		31781
TR320		2N3640		31781
TR321		2N3906		21533
TR322		2N3906		21533
TR323		2N3906		21533
TR324		2N3904		24146
TR325		2N3904		24146
DIODES				
D301		IN3595		29330
D302		IN3595		29330
D303		ZENER	10V	33935
D304		IN4148		23802
D305		IN4148		23802
D309		ZENER	7V5	33932
D310		ZENER	7V5	33932
D311		IN4148		23802
D312		IN4148		23802
D313		IN4148		23802
D314		IN4148		23802
D315		IN4148		23802
D316		IN4148		23802
D317		IN4148		23802
D318		IN4148		23802
D319		IN4148		23802
D320		IN4148		23802
D321		IN4148		23802
D322		ZENER	2V7	33921
D323		ZENER	6V2	33930
D324		ZENER	12V	33937
D325		ZENER	12V	33937
D326		IN4148		23802
D327		IN4148		23802
SOCKETS				
SKP				36105
SKQ				36105
SKR				36105
SKS				36105
MISCELLANEOUS				
L301		Ferrite Bead		26986
IC301		78L15AWC		36092

ANALOGUE TO DIGITAL CONVERTOR

Ref	Value	Description	Tol %±	Part No.
RESISTORS				
R101	10	CF		21793
R102	390	CF		28722
R103	10	CF		21793
R104	1k2	CF		21800
R105	820	CF		28724
R106	1k	CP		35875
R107	47	MO		26748
R110	696R5	MF	.25	35874
R111	330	CF		28721
R112				
R113	12k	CF		21810
R114	1k	CP		35875
R115	6k8	MF		35873
R116	1k2	CF		21800
R120	12k	CF		21810
R121	1k2	CF		21800
R122	1k	CP		35875
R123	13k5	MF		35872
R124	220	CP		35877
R125	1k	MF		36032
R126	330	CF		28721
R127	12k	CF		21810
R128	6k96	MF		35867
R129	47	CF		28714
R130	1k2	CF		21800
R131	12k	CF		21810
R132				
R133	13k9	MF		35868
R134	1k2	CF		21800
R135	12k	CF		21810
R136				
R137	27k8	MF		35871
R138	1k2	CF		21800
R139	8k9	MF		35869
R140	5k6	CF		21806
R141	5k6	CF		21806
R142	5k6	CF		21806
R143	47	CF		28714
R144	47	CF		28714
R145	47	CF		28714
R146	10	MF		27314
R147	10	MF		27314
R148	10	MF		27314
R149	10	MF		27314
R150	10	MF		27314
R151	10	MF		27314
R152	10	MF		27314
R156	47	CF		28714
R157	47	CF		28714
R158	47	CF		28714
R159	47	CF		28714
R160	5k6	CF		21806
R161	5k6	CF		21806
R162	5k6	CF		21806
R163		A.O.T.		
R170	470	CF		21797
R171	1k	CF		21799
R172	1k	CF		21799
R173	1k	CF		21799
R181	2k2	CF		21802
R182				
R183	2k2	CF		21802
R184	1k	CF		21799
R185	1k5	CF		21801
R186	220	CF		21796
R201	47	CF		28714
R202	3k9	CF		21804
R203	1k2	CF		21800
R204	3k9	CF		21804
R205	2k7	CF		28726
R206	4k7	CF		21805
R207	100	CF		21794
R208	220	CF		35881
R209	2k7	CF		28726
R210	560	CF		18547
R211	2k2	CF		21802
R212	1k	CF		21799
R213	47	CF		28714
R214	22	CF		28710
R214	22	CF		28710
R215	22	CF		28710
R216	22	CF		28710
R217	4k7	CF		35879
R218	6k8	CF		21807
R219	5k6	CF		21806
R220	3k9	CF		21804
R221	470	CF		18546
R222	1k2	CF		21802
R223	3k9	CF		21804
R224	10k	CF		21809
R225	3k9	CF		21804
R226	1k	CF		21799
R227	47	CF		28714
R228	22	CF		28710
R229	470	CF		21797
R230	22	CF		28710
R231	470	CF		21797
R232	680	CF		28723
R233	100	CF		21794
R234	1k	CF		21799
R235	2k2	CF		21802
R236	100	CF		21794
R237	68	CF		28716
R239	47	CF		28714
R240	1k	CF		21799
R241	1k8	CF		28725

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ANALOGUE TO DIGITAL CONVERTOR (Contd.)

Ref	Value	Description	Tol %±	Part No.
RESISTORS (Contd.)				
R242	4k7	CF		21805
R243	22	CF		28710
R244	680	CF		28723
R245	22	CF		28710
R246	330	CF		28721
R247	22	CF		28710
R248	47	CF		28714
R249	1k	MF		36032
R250	1k	CF		21799
R251	22	CF		28710
R252	270	CF		28720
R253	330	CF		28721
R254	22	CF		28710
R255	47	CF		28714
R256	250	MF		35870
R257	1k	CF		21799
R258	680	CF		28723
R259	22	CF		28710
R260	1k8	CF		28725
R261	4k7	CF		21805
R262	22	CF		28710
R263	27	CF		28711
R264	680	CF		18548
R265	1k	CF		21799
R266	50	MF	.25	35866
R267	50	MF	.25	35866
R268	50	MF	.25	35866
R269	47	CF		28714
R270	47	CF		28714
R271	47	CF		28714
R272	68	CF		28716
R273	2k2	CF		21802
R274	27	CF		28711
R275	5k6	CF		21806
R276	5k6	CF		21806
R277	5k6	CF		21806
R278	10	MF		27314
R279	10	MF		27314
R280	10	MF		27314
R281	10	MF		27314
R282	10	MF		27314
R283	10	MF		27314
R284	10	MF		27314
R285	47	CF		28714
R286	47	CF		28714
R287	47	CF		28714
R288	47	CF		28714
R289			A.O.T.	
R290	100	CF		21794
R291	100	CF		21794
R292	2k7	CF		28726
R293	47	CF		28714
R294	47	CF		28714
R295	47	CF		28714
R298	100	CF		21794

Ref	Value	Description	Tol %±	Part No.
CAPACITORS				
C201	.01μF	CE(2)	250V	22395
C202	22μF	E	25V	32181
C203	.01μF	CE(2)	250V	22395
C204	.1μF	CE(1)	30V	19647
C205	.1μF	CE(1)	30V	19647
C206	12pF	CE(2)	A.O.T. 500V	22365
C207	5.6pF	CE(2)	500V	22361
C208	.1μF	CE(1)	30V	19647
C209	22μF	E	25V	32181
C210	150pF	CE(2)	500V	22378
C211	5.6pF	CE(2)	500V	22361
C212	27pF	CE(2)	500V	22369
C213	10pF	CE(2)	500V	22364
C214	18pF	CE(2)	500V	22369
C215	.1μF	CE(1)	30V	19647
C216	12pF	CE(2)	500V	22365
C217				
C218	.1μF	CE(1)	30V	19647
C219	.1μF	CE(1)	30V	19647
C220	.1μF	CE(1)	30V	19647
C221	5.6pF	CE(2)	500V	22361
C222	10pF	CE(2)	500V	22364
C223	39pF	CE(2)	500V	22371
C224	33pF	CE(2)	500V	22370
C225	.1μF	CE(1)	30V	19647
C226	.1μF	CE(1)	30V	19647
C227	5.6pF	CE(2)	500V	22361
C228	39pF	CE(2)	500V	22371
C229	390pF	CE(2)	500V	22382
C230	150pF	CE(2)	500V	22378
C231	150pF	CE(2)	500V	22378
C232				
C233	22pF	CE(2)	500V	22368
C234	.01μF	CE(2)	250V	22395
C235	.1μF	CE(1)	30V	19647
C236				
C237				
C238	.01μF	CE(2)	250V	22395
C239				
C240	22μF	E	25V	32181
C241	4.7μF	E	63V	32195
C242	.01μF	CE(2)	250V	22395
C243	.01μF	CE(2)	250V	22395
C244	.01μF	CE(2)	250V	22395
C245	.1μF	CE(1)	30V	19647
C246	.1μF	CE(1)	30V	19647
C247	1000pF	CE(2)	500V	22387
C248	330pF	CE(2)	500V	22381
C249	.01μF	CE(2)	250V	22395
C250	22pF	CE(2)	500V	22368
C260	.1μF	CE(1)	30V	19647
C261	22μF	E	25V	32181
C262	.1μF	CE(1)	30V	19647
C263	.01μF	CE(2)	250V	22395
C264	.01μF	CE(2)	250V	22395
C265	.1μF	CE(1)	30V	19647

ANALOGUE TO DIGITAL CONVERTOR (Contd.)

Ref	Value	Description	Tol %±	Part No.
CAPACITORS (Contd.)				
C266	.1μF	CE(1)	30V	19647
C267	.1μF	CE(1)	30V	19647
C268	.1μF	CE(1)	30V	19647
C269				
C270	.047μF	CE(2)	12V	19657
C271	.047μF	CE(2)	12V	19657
C272	.047μF	CE(2)	12V	19657
C273	.047μF	CE(2)	12V	19657
C274	.047μF	CE(2)	12V	19657
C275	22μF	E	25V	32181
C276	120pF	CE(2)	500V	22377
INTEGRATED CIRCUITS				
IC101		723		31228
IC102		CA3046		36632
IC111		TY38111		36928
IC112		TY38111		36928
IC113		TY38111		36928
IC114		TY38111		36928
IC115		TY38111		36928
IC116		TY38111		36928
IC117		TY38111		36928
IC118		TY38111		36928
IC119		TY38111		36928
IC120		7475		31834
IC121		7400		52038
IC122		7400		52038
IC123		74S74		36005
IC124		74S74		36005
IC125		7420		52039
IC126		7408		53688
IC127		7403		31879
IC128		7404		31836
IC129		7400		52038
IC130		74S74		36005
IC131		74S74		36005
IC132		7400		52038
TRANSISTORS				
TR132		2N3906		21533
TR133		BC107		26790
TR134		2N2369		23307
TR135		2N2369		23307
TR136		2N3906		21533
TR137		2N2369		23307
TR138		2N2369		23307
TR139		2N3906		21533
TR140		BC107		26790
TR141		2N3906		21533
TR142		2N2369		23307
TR143		2N2369		23307
TR144		2N3906		21533
TR145		2N2369		23307
TR146		2N2369		23307
TR147		2N3906		21533
TR148		2N2369		23307
TR149		2N2369		23307

Ref	Value	Description	Tol %±	Part No.
TRANSISTORS (Contd.)				
TR150		2N3906		21533
TR151		2N3906		21533
TR201		2N2369		23307
TR202		2N2369		23307
TR203		2N2369		23307
TR204		2N2369		23307
TR205		2N2369		23307
TR206		2N2369		23307
TR207		2N2369		23307
TR208		E111		36028
TR209		2N2369		23307
TR210		2N2369		23307
TR211		E111		36028
TR212		2N2369		23307
TR213 }		AE23	Matched Pair	A32957
TR214 }				
TR215		2N3906		21533
TR219		2N3640		31781
TR220				
TR221		BFY 90		26987
TR222				
TR223		BFY 90		26987
TR224		2N3640		31781
TR225		2N2369		23307
TR226		2N2369		23307
TR227		2N2369		23307
TR231		BC182B		33205
TR232		BFY 51		29329
DIODES				
D101		IN4148		23802
D102		IN4148		23802
D103		IN4148		23802
D104		IN4148		23802
D105		IN4148		23802
D201		IN4148		23802
D202		ZENER	5V1	33928
D203		ZENER	5V1	33928
D204		ZENER	6V2	33930
D205		IN4148		23802
D206		IN4148		23802
D207		IN4148		23802
D208		ZENER	12V	33937
D209				
D210		IN4148		23802
D211		ZENER	6V2	33930
D212		IN4148		23802
D213		IN4148		23802
D214				
D215		IN4148		23802
D216		IN4148		23802
MISCELLANEOUS				
L201	10μH			35355

STORE AND TIMING LOGIC

Ref	Value	Description	Tol %±	Part No.
RESISTORS				
R601	470	CF		21797
R602	470	CF		21797
R603	1k	CF		21799
R604	3k3	CF		21803
R605	3k9	CF		21804
R606	2k2	CF		21802
R607	4k7	CF		21805
R608	6k8	CF		21807
R609	330	CF		28721
R610	1k	CF		21799
R611	1k	CF		21799
R612	1k	CF		21799
R613	2k2	CF		21802
R614	2k2	CF		21802
R615	3k9	CF		21804
R616	3k9	CF		21804
R617	4k7	CF		21805
R618	4k7	CF		21805
R619	4k7	CF		21805
R620	1k	CF		21799
R621	1k	CF		21799
R622				
R623	47	CF		28714
R624	1k	CF		21799
R625	1k	CF		21799
R626	1k	CF		21799
R627	1k	CF		21799
R628	1k	CF		21799
R700	5k6	CF		21806
R701	4k7	CF		21805
R702	4k7	CF		21805
R703	1k	CF		21799
R704	2k2	CF		21802
R705	2k2	CF		21802
R706	1k	CF		21799
R707	1k	CF		21799
R708	2k2	CF		21802
R709	2k2	CF		21802
R710	330	CF		28721
R711	330	CF		28721
R712	330	CF		28721
R713				
R714	2k2	CF		21802
R715	2k2	CF		21802
R716	2k2	CF		21802
R717	2k2	CF		21802
R718	2k2	CF		21802
R719	2k2	CF		21802
R720	1k	CF		21799
R721	1k	CF		21799
R722	1k	CF		21799
R723	1k	CF		21799
R724	4k7	CF		21805
R725	2k2	CF		21802
R726	2k2	CF		21802

Ref	Value	Description	Tol %±	Part No.
RESISTORS (Contd.)				
R727	1	WW	2½W	31890
R728	3k3	CF		21803
R729	2k2	CF		21802
R730	1k	CP		35875
R731	1k	CF		21799
R732	220	CF		21796
R733	82	MF		36033
R734	1k	MF		36032
R735	470	CF		21797
R736	1k	MF		36032
R737	100	CF		21794
R738	47	CF		28714
R739	10	CF		21793
R740	220	CF		21796
R741	5k6	CF		21806
R742	5k6	CF		21806
R743	2k2	CF		21802
R744	4k7	CF		21805
R745	8k2	CF		21808
R746	220	CF		21796
R747	47k	CF		21815
R748	4k7	CF		21805
R749	4k7	CF		21805
R750	2k7	CF		28726
R751	1k	MF		36032
R752	2k7	CF		28726
R753	2k2	CF		21802
R754	1k	CF		21799
R755	1k8	CF		28725
R756	4k7	CF		21805
R757	1k	CF		21799
R758	1k8	CF		28725
R759	47k	CF		21815
R760	470	CF		21797
R761	2k2	CF		21802
R762	2k2	CF		21802
R763	10k	CF		21809
R764	4k7	CF		21805
R765	4k7	CF		21805
R766	4k7	CF		21805
R767	4k7	CF		21805
R768	4k7	CF		21805
R769	4k7	CF		21805
R770	1k	CF		21799
R771	4k7	CF		21805
R772	1k	CF		21799
R773	6k8	CF		21807
R774	10k	CP		36031
R775	100	CF		21794
R776	1k	CF		21799
R777	820	CF		28724
R778	10	CF		21793
R779	10	CF		21793
R780	10	CF		21793
R781	2k2	CF		21802
R782	470	CF		21797

STORE AND TIMING LOGIC (Contd.)

Ref	Value	Description	Tol %±	Part No.
RESISTORS (Contd.)				
R783	4k7	CF		21805
R784	330	CF		28721
R785	2k2	CP		36030
R786	2k2	CP		36030
R787	100	CF		21794
R788	180	CF		21795
R789	2M2	CC		1180
R790	2k2	CF		21802
R791	4k7	CF		21805
R792	1k	CF		21799
R793	2k2	CF		21802
R794	1k	CF		21799
R795	560	CF		21798
R796	1k	CF		21799
R797	1k8	CF		28725
R798	1k8	CF		28725
R799	56	MF		36034
CAPACITORS				
C601	15pF	TRIMMER		36227
C602	22pF	CE(2)		34348
C603				
C604	.047μF	CE(1)	12V	19657
C605	.047μF	CE(1)	12V	19657
C606	.047μF	CE(1)	12V	19657
C607	.047μF	CE(1)	12V	19657
C608	100pF	CE(2)	500V	22376
C609	.047μF	CE(1)	12V	19657
C610				
C611	.047μF	CE(1)	12V	19657
C612	.047μF	CE(1)	12V	19657
C613				
C614				
C615	.047μF	CE(1)	12V	19657
C616	.047μF	CE(1)	12V	19657
C617				
C618				
C619	.047μF	CE(1)	12V	19657
C620	.047μF	CE(1)	12V	19657
C621				
C622				
C623	.047μF	CE(1)	12V	19657
C624				
C625	.047μF	CE(1)	12V	19657
C626	10μF	E	25V	32180
C627	220pF	CE(2)	500V	22379
C628				
C629	.1μF	CE(1)	30V	19647
C701	.01μF	CE(2)	250V	22395
C702	47pF	CE(2)	250V	22372
C703	680pF	CE(2)	500V	22385
C704	1000pF	CE(2)	500V	22387
C705	330pF	CE(2)	500V	22381
C706	56pF	CE(2)	500V	22373
C707	220pF	CE(2)	500V	22379

Ref	Value	Description	Tol %±	Part No.
CAPACITORS (Contd.)				
C708	.1μF	CE(2)	30V	19647
C709	560pF	CE(2)	500V	22394
C710	10pF	CE(2)	500V	22364
C711	.1μF	CE(1)	30V	19647
C712	3/10pF	TRIMMER		32669
C713	12/75pF	TRIMMER		36091
C714	560pF	CE(2)		36093
C715	560pF	CE(2)		36093
C716	100pF	CE(2)	500V	22376
C717	220pF	CE(2)	500V	22379
C718	.01μF	CE(2)	250V	22395
C719	.01μF	CE(2)	250V	22395
C720	22μF	E	25V	32181
C721	.1μF	CE(1)	30V	19647
C722	.1μF	CE(1)	30V	19647
C723	.01μF	CE(2)	250V	22395
C724	22μF	E	25V	32181
C725	.047μF	CE(1)	12V	19657
C726	.047μF	CE(1)	12V	19657
C727	.047μF	CE(1)	12V	19657
C728	.047μF	CE(1)	12V	19657
C729	1μF	PE	63V	31364
C730	.047μF	CE(1)	12V	19657
C731	.047μF	CE(1)	12V	19657
C732	.047μF	CE(1)	12V	19657
C733	.047μF	CE(1)	12V	19657
C734	.1μF	CE(1)	30V	19647
C735	.047μF	CE(1)	12V	19657
C736	.047μF	CE(1)	12V	19657
C737	100pF	CE(2)	500V	22376
C738				
C739				
C740	1500pF	CE(2)	500V	22388
C741				
C742	.01μF	CE(2)	250V	22395
C743	.01μF	CE(2)	250V	22395
INTEGRATED CIRCUITS				
IC602		74S74		36005
IC603		7420		52039
IC604				
IC605		7400		52038
IC606		7403		31879
IC607		7400		52038
IC608				
IC609				
IC610		74S74		36005
IC611		7404		31836
IC612				
IC613		7475		31834
IC614		8242 OR 9386		35679
IC615				
IC616				
IC617		7400		52038
IC618		7475		31834
IC619		7475		31834

STORE AND TIMING LOGIC (Contd.)

Ref	Value	Description	Tol %±	Part No.
INTEGRATED CIRCUITS (Contd.)				
IC620		7476		33448
IC621		7475		31834
IC622		8242 OR 9386		35679
IC623		8242 OR 9386		35679
IC624				
IC625		7400		52038
IC626		4102-1 OR 2102-1		35680
IC627		4102-1 OR 2102-1		35680
IC628				
IC629		7474		52098
IC630		7400		52038
IC631		7482		35678
IC632		7410		52043
IC633		4102-1 OR 2102-1		35680
IC634		4102-1 OR 2102-1		35680
IC635		4102-1 OR 2102-1		35680
IC636		7474		52098
IC637		74157		36007
IC638		8242 OR 9386		35679
IC639		7476		33448
IC640		7476		33448
IC641		4102-1 OR 2102-1		35680
IC642		4102-1 OR 2102-1		35680
IC643		4102-1 OR 2102-1		35680
IC644		7475		31834
IC645		74157		36007
IC646		8242 OR 9386		35679
IC647		7493		52341
IC648		7493		52341
IC650		7495A		36006
IC651				
IC652		7475		31834
IC653		74157		36007
IC654		8242 OR 9386		35679
IC655		7493		52341
IC656		7493		52341
IC657				
IC658				
IC659		7495A		36006
IC701		7400		52038
IC702		7400		52038
IC703				
IC704				
IC705		7404		31836
IC706		7400		52038
IC707		7400		52038
IC708		7476		33448
IC709		7400		52038
IC710		7403		31879
IC711		MOSTEK 5009		34952
IC712				
IC713		7403		31879
IC714				

Ref	Value	Description	Tol %±	Part No.
INTEGRATED CIRCUITS (Contd.)				
IC715				
IC716		7403		31879
IC717		7410		52043
IC718		7476		33448
IC719		7400		52038
IC720		7410		52043
IC721		7476		33448
IC722		7476		33448
IC723		7476		33448
IC724				
IC725		7400		52038
IC726		7476		33448
IC727		7405		53637
IC728		7400		52038
IC729		7400		52038
IC730				
IC731		7400		52038
IC732		7410		52043
IC733		7400		52038
IC734		7474		52098
IC735		7403		31879
IC736		7400		52038
IC739		7476		33448
IC740		7400		52038
IC741		7476		33448
IC742		7476		33448
IC743		SL702C		30214
IC744		702C		24789
IC745		1408-8		35683
TRANSISTORS				
TR601		2N2369		23307
TR602		2N3640		31781
TR603		2N3640		31781
TR701		BC212		29327
TR702				
TR703				
TR704		BC108		26110
TR705		BN2369		23307
TR706		2N2369		23307
TR707		E111		36028
TR708		2N2369		23307
TR709		2N2369		23307
TR710		BC214C		36019
TR711		BC212		29327
TR712		E111		36028
TR713		BC212		29327
TR714		E111		36028
TR715		2N2369		23307
TR716				
TR717		2N2369		23307
TR718		2N2369		23307

STORE AND TIMING LOGIC (Contd.)

Ref	*Value*	*Description*	*Tol %±*	*Part No.*
DIODES				
D601				35202
D602				35202
D603				35202
D701	6V2	ZENER		33930
D702		IN4148		23802
D703	11V	ZENER		33936
D704		IN4148		23802
D705		IN4148		23802
D706		IN4148		23802
D707		IN4148		23802
D708		IN4148		23802
D709	5V6	ZENER		33929
D710		IN4148		23802
D711	12V	ZENER		33937
D712		IN4148		23802
D713		IN4148		23802
D714				
D715				
D719		IN4148		23802
D720		IN4148		23802
D721	6V2	ZENER		33930
L701	33μH			33204

Ref	*Value*	*Description*	*Tol%±*	*Part No*
SWITCHES				
S601				35344
S602				35343
S603				35344
S701				35341
S702				35341
S703				35342
S704				35342
SOCKETS				
SKA				36096
SKB				36096
SKD				36096
SKE				36096
SKH				36096
SKJ				36096
SKK				36096
SKL				36096
SKM				36096
SKY				36105

TIMEBASE

Ref	Value	Description	Tol %±	Part No.
RESISTORS				
R900	47	CF		28714
R901	10	CF		21793
R902	390	CF		28722
R903	1k2	CF		21800
R904	1k2	CF		21800
R905	47	CF		28714
R906	15	CF		28708
R907	15	CF		28708
R908	3k3	CF		18556
R909	82	CF		28717
R910	10	CF		21793
R911				
R912	560	CF		21798
R913	220	CF		21796
R914	220	CF		21796
R915	560	CF		21798
R916	2k2	CF		21802
R917	22k	CF		21812
R918	820k	CF		32360
R919	330	CF		28721
R920	120	CF		28718
R921	270	CF		28720
R922	22k	CF		21812
R923	22k	CF		21812
R924	820k	CF		32360
R925	330	CF		28721
R926	1k8	CF		28725
R927				
R928	270k	CF		32356
R929	3k9	CF		21804
R930	2k7	CF		28726
R931	10	CF		21793
R932	220	CF		21796
R933	1k5	CF		21801
R934	3k3	CF		21803
R935	4k7	CF		21805
R936	1k	CF		21799
R937	10k	CF		21809
R938	1k	CF		21799
R939	1M	CF		31840
R940	1k	CF		21799
R941	22k	CF		21812
R942	270	CF		28720
R943	3k3	CF		21803
R944	2k2	CF		21802
R945	2k2	CF		21802
R946	2k2	CF		21802
R947	4k7	CF		21805
R948	56k	CF		28729
R949	82k	CF		21818
R950	22k	CF		21812
R951	12k	CF		21810
R952	18k	CF		21811
R953	3k9	CF		21804
R954	3k9	CF		21804
R955	47k	CF		21815
RESISTORS (Cont.)				
R956	56k	CF		28729
R957	100k	CF		21819
R958	100k	CF		21819
R959	12k	CF		21810
R960				
R961	22k	CF		21812
R962	6k8	CF		21807
R963	27k	CF		21813
R964				
R965	1k2	CF		28100
R966	2k2	CF		21802
R967	2k2	CF		21802
R968	2k2	CF		21802
R969	2k2	CF		21802
R970	27k	CF		21813
R971	3k9	CF		21804
R972	4k7	CF		21805
R973	10k	CF	A.O.T.	21809
R974	22k	CF	A.O.T.	21812
R975	2M2	CC		1180
R976	100	CF		21794
R977	56k	CF	1W	19058
R978	68k	CF		21816
R979	100	CF		21794
R980	3k9	CF		21804
R981	100	CF		21794
R982	56k	CF	1W	19058
R983	1k8	CF		28725
R984	10k	WW	4W	29481
R985	100	CF		21794
R986	1k6	MO		28793
R987	3k9	CF		21804
R988	10k	PCP		39265
R989	180	CF		21795
R990	250	PCP		40355
R991	120	CF		28718
R992	100	CF		21794
R993	10k	WW	4W	29481
R994	56k	CF	1W	19058
R995	1k8	CF		28725
R996	1k3	MO		28792
R997	1k6	MO		28793
R998	1k8	CF		28725
R999	100	CF		21794
R1000	15k	CF		28727
R1001	15k	CF		28727
R1002	27k	CF		21813
R1003	22k	CF		21812
R1004	4k7	CF		21805
R1005	22k	CF		21812
R1006	27k	CF		21813
R1007	100k	MF		29476
R1008	43k	MO		26723
R1009	2.5k	PCP		40354
R1010	4k3	MO		26723
R1011	2.5k	PCP		40354

TIMEBASE (Cont.)

Ref	Value	Description	Tol %±	Part No.
RESISTORS (Cont.)				
R1012	2.5k	PCP		40354
R1013				
R1014				
R1015	3k3	CF		21803
R1016	4k7	CF		21805
R1017	2.5k	PCP		40354
R1018	2k7	CF		28726
R1019	900	MF		35582
R1020	100	MF		35581
R1021	10k	CF		21809
R1022	1k	CF		21799
R1023	2k2	CF		21802
R1024	10	CF		21793
CAPACITORS				
C901	.01µF	CE(2)	250V	22395
C902	33pF	CE(2)	500V	22370
C903	33pF	CE(2)	500V	22370
C904	.01µF	CE(2)	250V	22395
C905	27pF	CE(2)	500V	22369
C906	.47µF	CE(2)	3V	35352
C907	.47µF	CE(2)	160V	31381
C908	470pF	CE(2)	500V	22383
C909	4700pF	CE(2)	500V	22393
C910	.01µF	CE(2)	250V	22395
C911	270pF	CE(2)	500V	22380
C912	.01µF	CE(2)	250V	22395
C913	.01µF	CE(2)	250V	22395
C914	27pF	CE(2)	500V	22369
C915	27pF	CE(2)	500V	22369
C916	27pF	CE(2)	500V	22369
C917	.01µF	CE(2)	250V	22395
C918	0.047µF	CE(2)	12V	19657
C919	.1µF	CE(2)	30V	19647
C920	220pF	CE(2)		11587
C921	.1µF	CE(2)	30V	19647
C922	.1µF	CE(2)	30V	19647
C923	.01µF	CE(2)	1%	24886
C924	.047µF	CE(2)	30V	2793
C925	.01µF	CE(2)	250V	22395
C926	27pF	CE(2)	500V	22369
C927	1000pF	CE(2)	500V	22387
C928	220pF	CE(2)	500V	22379
DIODES				
D900		IN4148		23802
D901		IN3595		29330
D902		IN4148		23802
D903		IN4148		23802
D904		IN4148		23802
D905	8V2	ZENER		33933
D906		IN4148		23802
D907		IN4148		23802
D908		IN4148		23802
D909		IN4148		23802
D910		IN4148		23802

Ref	Value	Description	Tol %±	Part No.
DIODES (Contd.)				
D911		IN4148		23802
D912		IN4148		23802
D913		IN4148		23802
D914		IN4148		23802
D915		ZENER	5V6	33929
D916				35202
D917		OA47		4468
D919		IN4148		23802
INTEGRATED CIRCUITS				
IC901		7403		31879
IC902		7400		52038
IC903		7476		33448
IC904		7403		31879
IC905		7400		52038
IC906		7410		52043
TRANSISTORS				
TR901		2N2369		23307
TR902		2N2369		23307
TR903		2N2369		23307
TR904		2N2369		23307
TR905		BC212		29327
TR906		BC182B		33205
TR907		BC212		29327
TR908		2N2369		23307
TR909		2N2369		23307
TR910		BC212		29327
TR911		2N2369		23307
TR912		2N2369		23307
TR913		2N2369		23307
TR914		BC108		26110
TR915		2N2369		23307
TR916		2N2369		23307
TR917		BC108		26110
TR918		2N2369		23307
TR919		2N2369		23307
TR920		2N2369		23307
TR921		BC212B		36900
TR922		BC212		29327
TR923		BC182B		33205
TR924		BC212		29327
TR925		BF258		31490
TR926		BF258		31490
TR927		BC212		29327
TR928		MPF102		25870
TR929		MPF102		25870
TR930		2N2369		23307
TR931		2N2369		23307
TR932		BC212		29327
TR933		BC212		29327
TR934		BC212		29327
SWITCHES				
S900				35999
S901				35343

INTERCONNECTIONS

Ref	Value	Description	Tol %±		Part No.
RESISTORS					
R1	22k	CP			A4/35986
R2	22k	CP			A4/35986
R3	470	CP	With S13		A4/36070
R4	470	CP	With S14		A4/36070
R5					
R6	5k	CP	Part of S6		
R7	22k	CP	With S7		A4/35338
R8	1k + 1k	CP	R8a + R8b		A4/36069
R22	22	CF			28710
R23	22	CF			28710
R24	990k	MF	½		31927
R25	22	CF			28710
R26	470k	CC		¼W	4906
R27	1M	MF			26346
R28	18	CF			28709
R29	16k	MF			29361
R30	15k8	MF			33291
R31	5k23	MF			33290
R32	1k72	MF			33289
R33	787	MF			33288
R34	360	MF			33287
R35					
R42	22	CF			28710
R43	22	CF			28710
R44	990k	MF	½		31927
R45	27	CF			28711
R46	470k	CC	10	¼W	4906
R47	1M	MF			26346
R48	18	CF			28709
R49	16k	MF			29361
R50	15k8	MF			33291
R51	5k23	MF			33290
R52	1k72	MF			33289
R53	787	MF			33288
R54	360	MF			33287
R55					
R57	270	CF			28720
R58	68k	CF			21816
R59	150k	CF			21821
R90	100k	CF		1W	19061
R91	470	CF			21797
R92	4k7	CF			21805
R93/98		RESISTOR NETWORK			A3/36455
CAPACITORS					
C20	.1μF	PE		400V	29495
C25	.01μF	CE(2)		500V	24902
C40	.1μF	PE		400V	29495

Ref	Value	Description	Tol %±		Part No.
CAPACITORS (Contd.)					
C45	.01μF	CE(2)		500V	24902
C51	47000μF	E		10V	36024
C90	5600pF	CE(2)		500V	22394
C91	4.7μF	E		63V	32195
C92	.047μF	CE(2)		30V	2793
C93	1μF	CE(2)	1	63V	24888
C94	.01μF	PE	1	160V	24886
C95	6/25pF	TRIMMER			23593
C96	47pF	CE(2)			685
RECTIFIERS					
BR51		WO4			29367
BR52		WO4			29367
BR53		WO4			29367
BR54		WO4			29367
BR55		VH148			36281
SWITCHES					
S1					A3/31292
S2					A3/31292
S3					35998
S4					35998
S5					
S6			With R6		35345
S7			Part of R7		
S13			Part of R3		
S14			Part of R4		
S51					A4/36232
S52					29057
DIODES					
D53		IN4003			32771
D54		IN4003			32771
D90		OA47			4468
D91		OA47			4468
SOCKETS					
SKV					1222
SKW					1222
SKX					1222
SKZ					24913
MISCELLANEOUS					
L20		FX1242			26986
L21		FX1242			26986
L22		FX1242			26986
L23		FX1242			26986
L24		FX1242			26986
L25		FX1242			26986