MODEL 10282A/1640A OPTION 002 SDLC

(Synchronous Data Link Control)

MANUAL SUPPLEMENT

(Preliminary)

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## 1.   INTRODUCTION.

2.   This manual supplement complements the 1640A preliminary Service and Operating manuals.  It is for 1640A Serial Data Analyzers equipped with Option 002 SDLC (Synchronous Data Link Control).  It contains installation, operation, test, and service information.

## 3.   DESCRIPTION.

4.   The Hewlett-Packard Model 1640A Option 002 consists of a 1640A with SDLC Board A10 installed in place of Dummy Board A8.  This increases the 1640A interface capability to include Synchronous systems that use High Level Data Link Control (HDLC), such as IBM's SDLC or CCITT X.25 protocol.

5.   In SDLC protocol, communication is performed via frames. Frames define a bit stream into meaningful blocks.  Each frame is bounded (delimited) by a beginning and an ending flag (figure 1). The flag bit pattern is $01111110_2$ ($7E_{16}$).
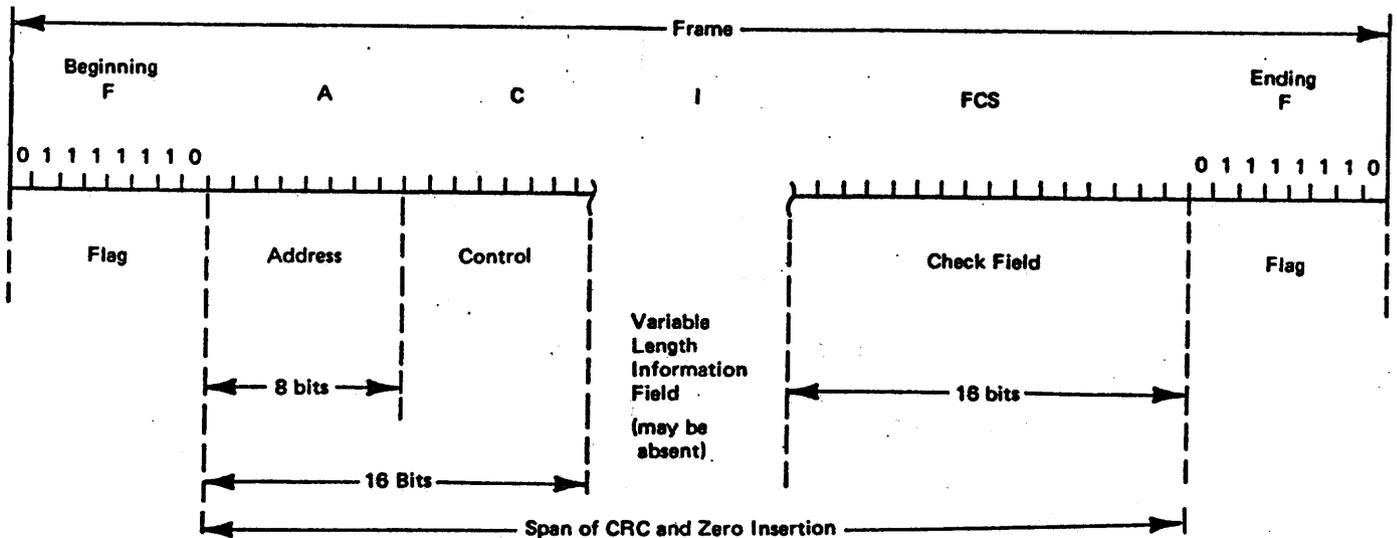


Figure 1. Frame Format ( courtesy of International Business
Machines Corporation).

6. Between the flags, the bit stream is formatted into fields. These fields are defined as: Address (A); Control (C); Information (I); and Frame Check Sequence (FCS).

7. The Address field (8 bits following the beginning flag) contains a secondary station address (primary station is never addressed). The Control field (next 8 bits after the Address field) contains commands or responses for data link control. Next is the Information field for data transfer. It has no restrictions on format, content, or length (completely left out in some cases). The last 16 bits prior to the ending flag are defined as the Frame Check Sequence field. The FCS is used to detect transmission errors via a Cyclic Redundancy Check.

8. Since a frame is delimited by flags, the fields within a frame must not contain any flag bit patterns (01111110). This is prevented by zero insertion and deletion. The transmitter automatically inserts a zero following any bit pattern of five ones in a row that occurs between flags. Any inserted zeros are automatically deleted by the receiver. Inserted and deleted zeros are not included in the FCS computation.

9. 1640A Option 002 SDLC Compatibility:

   a. Zero insertion in Simulate (on TX data out). Zero deletion both in Monitor (on incoming TX and RX data) and in Simulate (on incoming RX data).

b.   Frame Check Sequence (FCS) generation in Simulate.  FCS checking (via ERROR Trigger) both in Monitor (on incoming TX and RX data) and in Simulate (on incoming RX data).

c.   Automatic flag and abort (defined as more than 7 ones in a row) recognition for framing and FCS computation on all incoming data (both Monitor and Simulate).

d.   Functional in point-to-point and multipoint networks, but not in loop configurations.

e.   Not capable of automatically encoding Control field commands and responses in Simulate.  For example:  will not generate or respond to the following: frame sequencing ($N_s$ and $N_r$ counts); retransmission requests; or traffic regulation.

10.  A field-installable kit (HP Part No. 10282A) is available that allows modification of a standard 1640A for Option 002 SDLC capability.

11.  INSTALLATION.

12.  To install a 10282A in an HP Model 1640A, proceed as follows:

a.   Set LINE switch to off position and disconnect power cord.

b.   Remove 1640A top cover (4 black pozidrive screws in corners).  Do not remove the cables between top cover and mainframe.

c.   Remove front PC board retaining bracket.  A common screwdriver with a long blade is necessary.

d.   Remove Dummy Board A8 (or CRC Board A9, if installed) from Mother Board A1.   See figure 2.
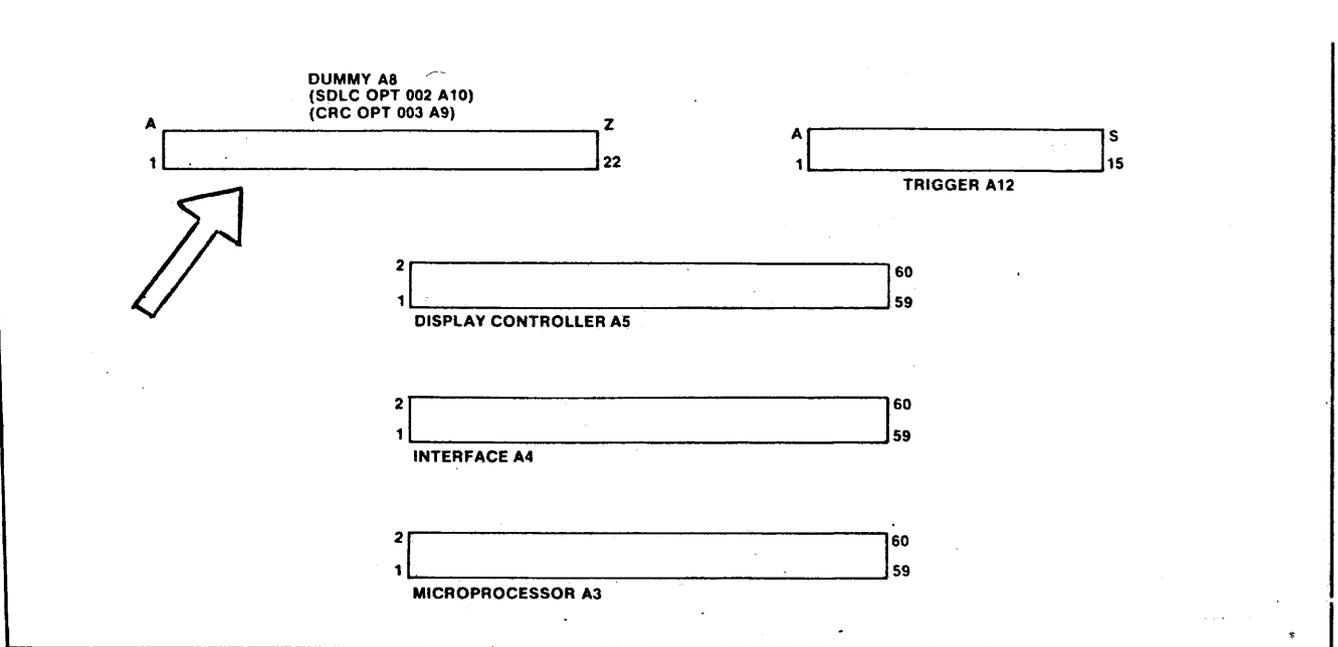


Figure 2. Dummy/SDLC/CRC Board Location on Mother Board.

e.   Install SDLC Board A10 in Dummy/SDLC/CRC connector on Mother Board A1 (figure 2).   Make sure that the component side of the board is facing away from the CRT (pin 1 of board must match pin 1 of connector).

<u>CAUTION</u>

If SDLC Board A10 is installed with component side facing the CRT, instrument damage may result.

f.   Reinstall front PC board retaining bracket.

g.   Replace 1640A top cover and reinstall 4 black screws.

h.   Reconnect power cord.

13.   OPERATION.

14.   A 1640A Option 002 may be used four ways:   (1) as if the option were not installed; (2) to transmit simple (non-sequenced format) SDLC frames in Simulate; (3) to monitor SDLC communications; or (4) to detect SDLC Frame Check Sequence errors (via ERROR Triggering) in either Monitor or Simulate.

15.   To configure the 1640A Option 002 for SDLC Frame Check Sequence error detection, either Monitor or Simulate, proceed as follows:

    a.   Press FORMAT key.

    b.   Use FIELD SELECT key to set DATA CODE to [ASCII-8] .

    c.   Move blinking cursor down to MODE with ⬇ CURSOR key and use FIELD SELECT key to choose [SYNC] .

    d.   Move cursor down to ERROR CHECK.

    e.   Use FIELD SELECT key to choose [SDLC] .

    f.   Press MODE key.

    g.   With either [MONITOR] or [SIMULATE] selected, move cursor down to TRIG SOURCE and select [ERROR] with FIELD SELECT key.

<div align="center">NOTE</div>

If Simulate mode is selected (for example, performing loop-back testing with the 1640A as the source in order to identify modem pattern incompatibility), make sure

that a beginning and an ending flag are entered for each frame to be transmitted. The flag pattern of $01111110_2$ is entered via the Hex ENTRY keys 7 and E (∿ character in ASCII-8 ). Example: ∿A,C,I,FCS∿A,C,I,FCS∿.

16. The 1640A matrix must be configured to agree with the system under test. Also, 1640A menu choices should be set for the system and test desired (such as TRIG MODE, HALF or FULL DUP-LEX, SUPPRESS, etc.). See 1640A Operator's Guide.

17. The 1640A Option 002 will now trigger on any incoming Frame Check Sequence (TX or RX in Monitor; RX in Simulate) that does not match the FCS computed by the 1640A.

18. OPERATION VERIFICATION.

19. The 1640A Matrix Board is configured by means of jumper pins into a loop-around mode whereby the 1640A "talks to itself." An abbreviated SDLC data stream is entered in the transmit (TX) buffer from the keyboard. As this SDLC message is transmitted, the 1640A computes the Frame Check Sequence (FCS) characters and inserts them in the FCS field of the transmitted data frame. The received (RX) data is then checked to verify that proper FCS characters were generated by the 1640A. ERROR triggering is used to verify that no FCS errors occur (if TX FCS = RX FCS, then no trigger). Also, this test verifies flag recognition and zero insertion/deletion functions.

20. Procedure:

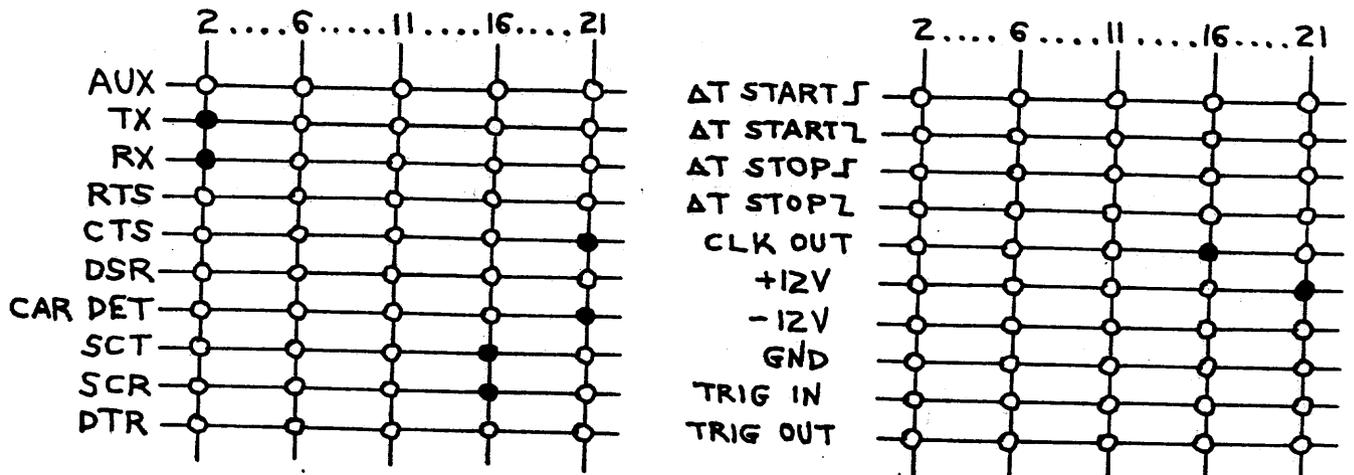a. Insert pins in matrix as shown in figure 3. Remove RS-232 cable from rear of matrix.



Figure 3. Matrix Board Pin Configuration.

b. Press FORMAT key.

c. Press DEFAULT key.

d. Use FIELD SELECT key to set DATA CODE to [ASCII-8].

e. Use ⬇ CURSOR key and FIELD SELECT key to set BITS/SEC to [300]. This sets CLK OUT to 4800 BPS (16 x 300).

f. Use CURSOR and FIELD SELECT keys to set MODE to [SYNC].

g. Move cursor down to ERROR CHECK and use FIELD SELECT key to choose [SDLC].

h. Press MODE key.

i. Press FIELD SELECT key, then NOT key to enter SIMULATE mode.

j. Choose [FULL DUPLEX], [TX FIRST], REPLY ON all Don't Care, AFTER ∅∅∅∅ MSEC.

k.  Move cursor down to TRIG SOURCE and select [ERROR] with FIELD SELECT key.

l.  Select RUN MODE [REPEAT & END ON TRIG].

m.  Select SUPPRESS [SYNCS].

n.  Press TX ENTRY key.

o.  Enter $F_F$ ~AB?~⊢.(Note:  Keystroke sequence is (F,F) = $F_F$ ; (7,E) = ~; (4,1) = A; (4,2) = B; (3,F) = ?; (7,E) = ~; (END) = ⊢ .)

p.  Press RUN key.

q.  Verify that data is continuously written on display without stopping.  This shows that the TX FCS matches the RX FCS (no FCS errors or else display stops).

r.  Press STOP key.

s.  Press FIELD SELECT key to view [TX] data.

t.  Verify that TX data pattern is $F_F$ ~AB?$F_F$$F_F$ ~ .  The two trailing $F_F$ (Hex) characters show that the 1640A added Frame Check Sequence (FCS) characters to its output data frame, but the 1640A transmitter doesn't know what these characters are, so it displays $F_F$$F_F$ .

u.  Press FIELD SELECT key to view [RX] data.

v.  Verify that RX data pattern is $F_F$AB? $C_4$& ~ . The $C_4$ and & characters are the correct FCS characters.

## 21. REPLACEABLE PARTS.

22. Table 1 lists replaceable parts for Model 10282A. Component locations for the SDLC printed circuit board A10 are shown in figure 4. To order a part from Hewlett-Packard, address the order to the nearest HP Sales/Service Office. Include the model number, reference designation for the part, and the HP part number. If a part is not listed, provide a complete description of the part, including function and location.

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## Table 1.
## Replaceable Parts

**MATERIAL LIST**

| MODEL OR ASSEMBLY | OPTION | DESCRIPTION | |
|---|---|---|---|
| 01640-66510 | | BD-SDLC | |
| MFG. SPECS. | PRELIM. REL. | REVISION | CYCLE DATE | DELIVER |
| 08 | 1365 | 05-16-78 | 0 | C212D |

| SPECIAL CODES | | | | | REF DESIG A10 / DESCRIPTION | OPTION | PART NUMBER | LOC | QUANTITY | U/M | PNCH ISSUE POL | ALT-DEL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RT | FD IP | ITEM | MU IP | FORM | | | | | | | | |
| | NN | 1* | | | PROD CHG RECORD E-26388 3-27-78 | | CHANGE | | 0 | | | |
| | | | | | C1-7 CF CE .01UF 100V 0103 | | 0160-2055 | A | 7 | | | |
| | | | | | C8 CF TA 10U 20V 0102 | | 0180-0374 | A | 1 | | | |
| | | | | | R1,2 RF.12MF 68.1 1 0101 | | 0757-0397 | A | 2 | | | |
| | | | | | X U26 SOCKET-IC 40 PIN 0104 | | 1200-0660 | A | 1 | | | |
| | | | | | U6,8 IC-HMI256BITPROM 0106 | | 1816-1333 ~~1816-0913~~ | H | 2 | | | |
| | | | | | U23 IC-MEMORY 74S287 0105 | | 1816-1302 | H | 1 | | | |
| | | | | | U9,16 IC TTL 74S112 0107 | | 1820-0629 | H | 2 | | | |
| | | | | | U22,25 IC 74LS74 0108 | | 1820-1112 | H | 2 | | | |
| | | | | | U10 IC 74LS02 0109 | | 1820-1144 | H | 1 | | | |
| | | 1* | | | U5,12 IC 74LS175 U18 0110 | | 1820-1195 | H | 3 | | | |
| | | 1* | | | U2,4 IC 74LS174 U21,24,27 0111 | | 1820-1196 | H | 5 | | | |
| | | | | | U14 IC 74LS04 0112 | | 1820-1199 | H | 1 | | | |
| | | | | | U15,19 IC 74LS51 0113 | | 1820-1210 | H | 2 | | | |
| | | | | | U11 IC QUAD 2-INPUT 0114 | | 1820-1211 | H | 1 | | | |
| | | | | | U7,13 IC-74LS164 0115 | | 1820-1433 | H | 2 | | | |
| | | | | | U1,3 IC 74LS169 0116 | | 1820-1435 | H | 2 | | | |

ASRLY CONT

-10-

| MODEL OR ASSEMBLY | OPTION | DESCRIPTION | PAGE |
|---|---|---|---|
| 01640-66510 | | BD-SDLC | 2 |

| MFG. SPECS. | PRELIM. REL. | REVISION | CYCLE DATE | DELIVER TO |
|---|---|---|---|---|
| 08 | 1365 | 05-16-78 | 0 | C2120 |

| SPECIAL CODES | | | | | | | | REF DESIG | DESCRIPTION | OPTION | PART NUMBER | LOC | QUANTITY | U/M | PCH | ISSUE POL | ALT-DEL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RT | FD | | ITEM | ML | | FORM | | | | | | | | | | | |
| | I | P | | I | P | M | | | | | | | | | | | |
| | | | | | | | | U26 | IC 8255 | 0202 | 1820-1919 | H | 1 | | | | |
| | | | | | | | | U17,20 | IC-8X01N | 0201 | 1820-2003 | H | 2 | | | | |
| | | | | | | | | | PC BD ETCHED | | *01640-26510 | A | 1 | | | | |
| | | | | | | | | | | | | | | | | END OF SL | |
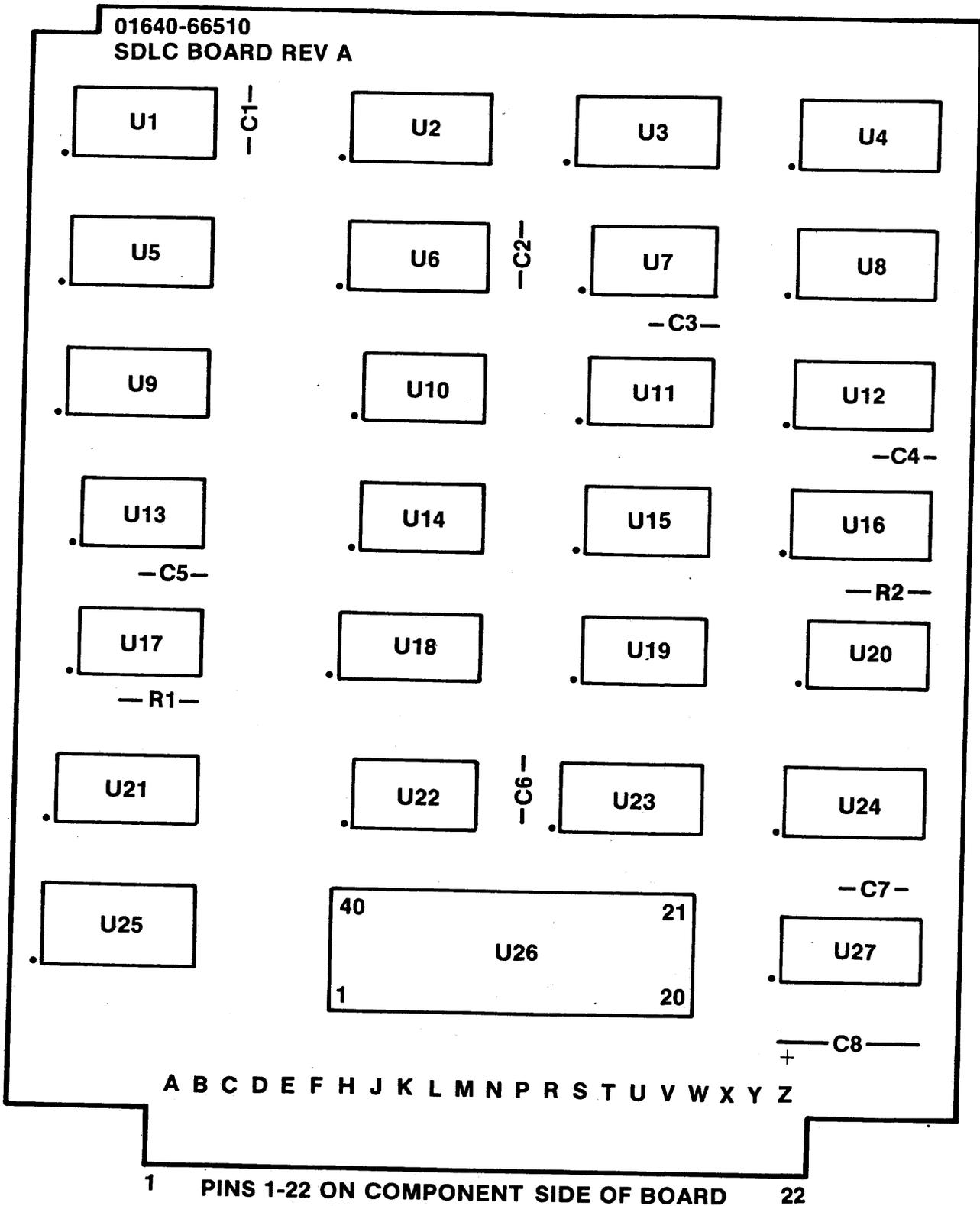
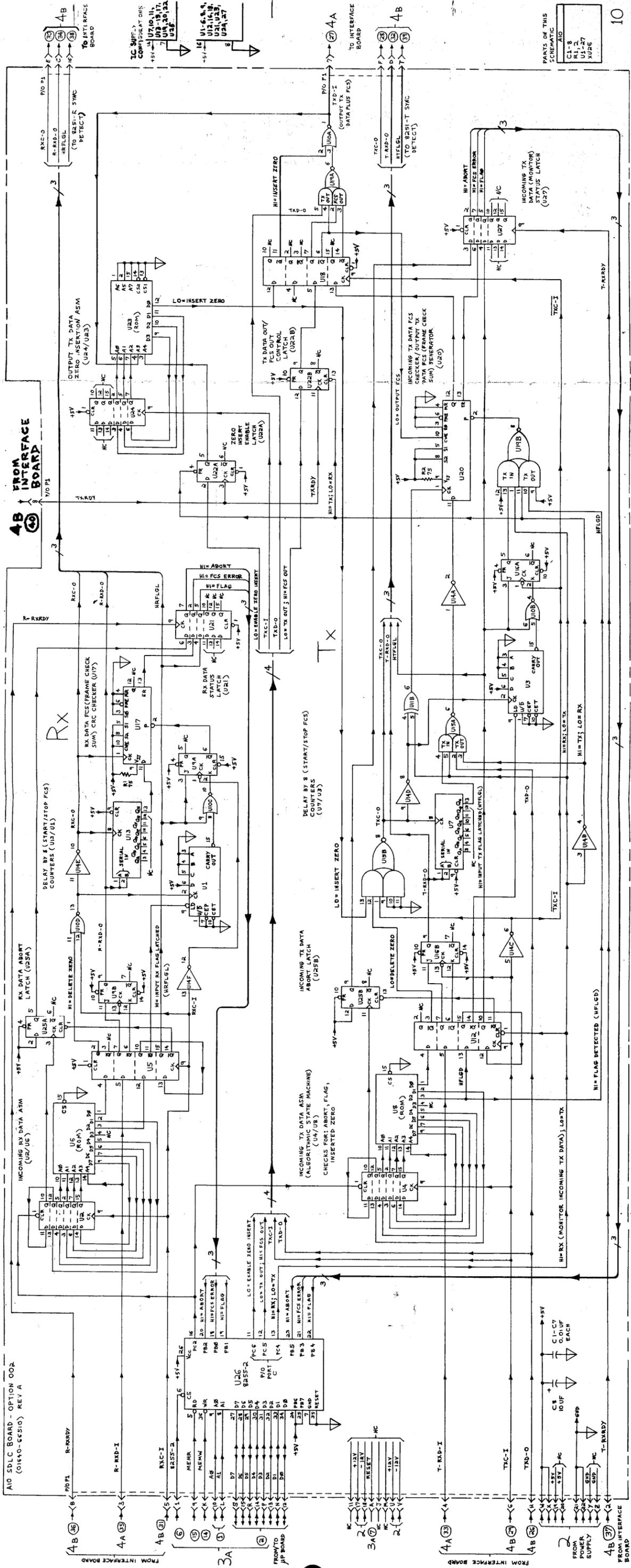Figure 4. SDLC Board A10 Component Locations.

# Model 10282A/1640A Option 002 SDLC

Figure 5. SDLC Board A10 Schematic.