Errata

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP 8657B referred to in this document is now the Agilent 8657B.

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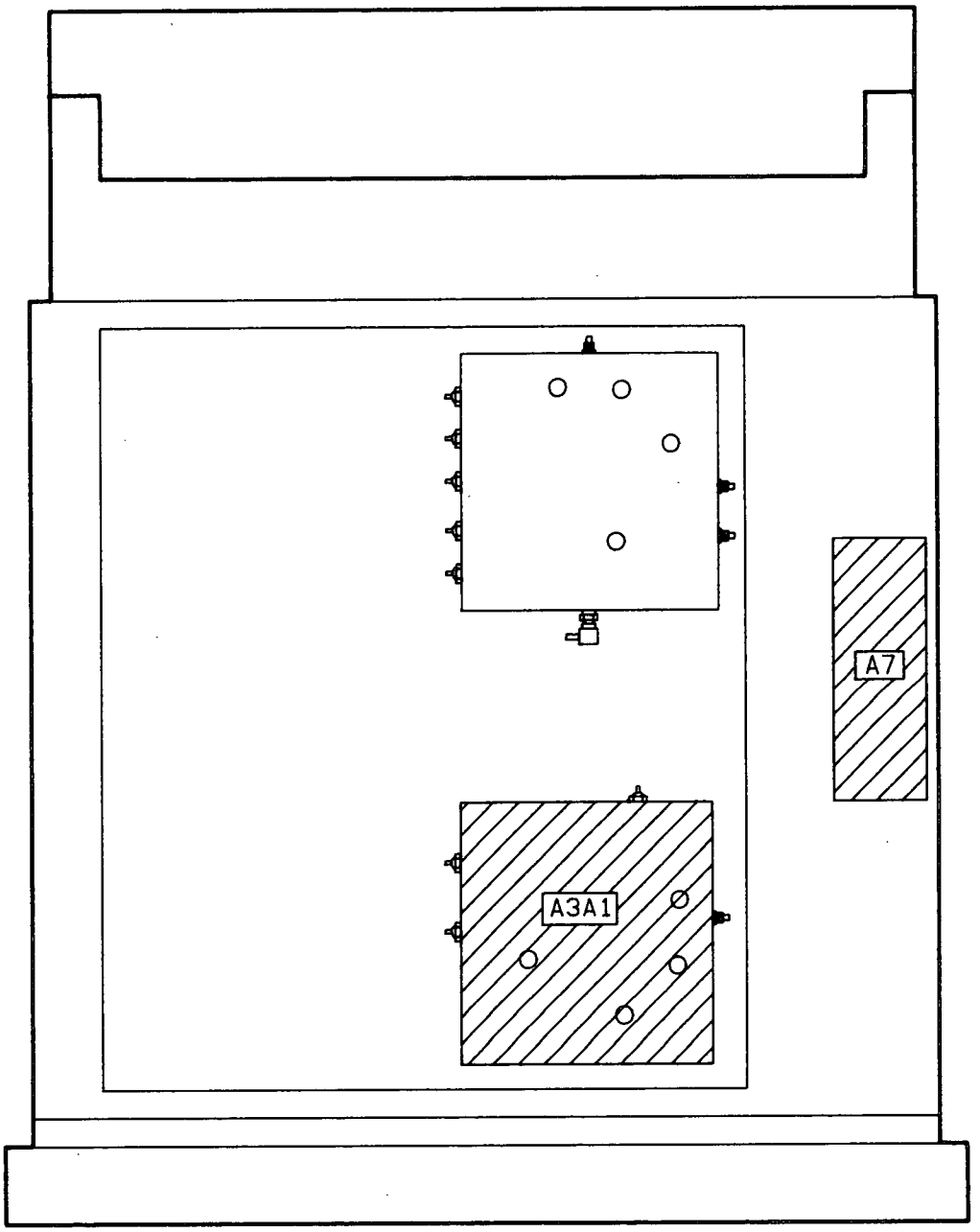
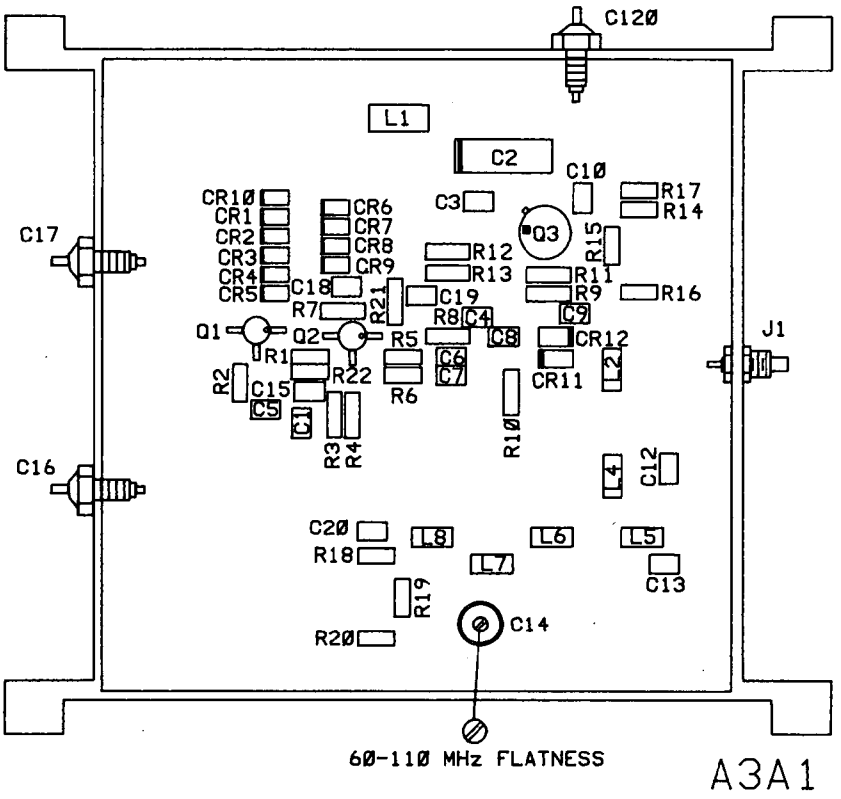
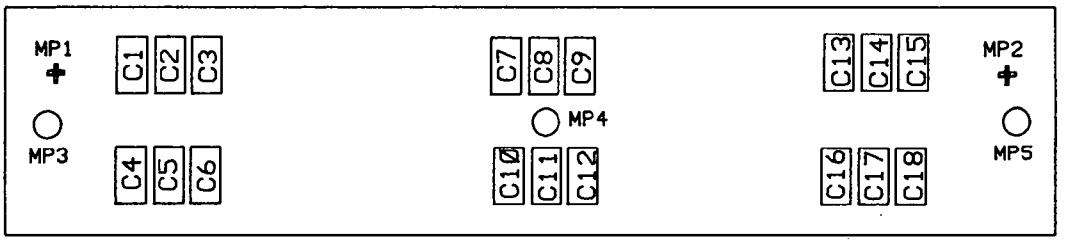
TOP INTERNAL VIEW - LEVEL 1



NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Chassis ground is achieved by mechanical contact through nuts holding PC board to frame.
3. Printed circuit trace inductor.
4. T1 is realized with semi-rigid coax cable. Inner conductor acts as transformer primary, outer ground shield acts as transformer secondary.
5. +11V is located on AC ground plane.





Component Locators

Figure Ø. Service Sheet 9 Information

Service Sheet 9

LOW FREQUENCY LOOP VOLTAGE CONTROLLED OSCILLATOR

PRINCIPLES OF OPERATION

General

The Low Frequency Voltage Controlled Oscillator (VCO) and Limiter Amplifier generate the 60 to 110 MHz signal that is mixed with 800 MHz on the Multiplier Assembly to lock the High Frequency Loop. The VCO is phase locked to the instrument's 50 MHz frequency reference by the Fractional-N phase lock loop. The Fractional-N phase lock loop and the VCO's frequency are controlled by data from the Microprocessor.

60 to 110 MHz VCO

The VCO is a tuned collector oscillator with transformer feedback. The transformer T1 is a piece of semi-rigid coax cable. The outer jacket is the primary and the center conductor is the secondary. The outer jacket primary is a 25 nH inductor and together with varactors CR1 through CR10 forms the tuned resonant circuit for the oscillator. Ten varactors are needed to achieve the tuning capacitance of 75 to 300 pF. Transistors Q1, Q2, and their associated components form an inverting amplifier with approximately 20 dB of gain. Positive feedback for oscillation is provided by feeding the amplifier output to the resonator by way of R11, while the input is connected to the secondary.

The VCO's frequency from 60-110 MHz is controlled by the tune voltage from the Fractional-N phase lock loop. The tune voltage is applied to the resonant circuit varactors through inductor L1. The frequency is approximately 60 MHz with the tune voltage at +9V and approximately 110 MHz with the tune voltage at −6V.

The +11V supply is the internal virtual ground for RF signals and is a stable dc voltage for the oscillator. Biasing for Q2 is provided through the primary (outer jacket) of T1 and resistors R3 and R7. Biasing for the base of Q1 is provided by resistors R12 and R13 through the center conductor (secondary) of T1.

Resistors R2 and R21 with their respective capacitors C5 and C15 are for oscillator stability. C18, C6, and C7 are dc-blocking capacitors.

Limiter Amplifier

The VCO's output is ac coupled to limiter amplifier Q3. The bias voltages of Q3 are set by resistors R9, R10 and R11. Collector to base diodes CR11 and CR12 limit the collector swing to ± one diode drop.

The output of the Limiter Amplifier is ac coupled by capacitor C10 to the Fractional-N phase lock loop Buffer Amplifier Q47 shown on Service Sheet 10 and to the 110 MHz Low-pass filter.

110 MHz Low-Pass Filter and Attenuator Pads

The input Attenuator of R14, R15 and R16 sets the input signal level to the Low-Pass Filter and provides impedance matching. The filter passes the 60 to 110 MHz VCO signal and rejects its harmonics. Capacitor C14 and inductor L7 form a series resonant circuit for adjusting the filters frequency response. The adjustment optimizes the filters rejection at 120 MHz. The output of the filter is fed to J1 through the level-setting attenuator formed by R18, R19, and R20.

TROUBLESHOOTING

Procedures for checking the A3A1 Low Frequency Loop Oscillator circuits are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, for example, ⟨✓1⟩ Fixed voltages are shown on the schematic inside a hexagon, for example, ⟨2V ±0.2V⟩ Transistor bias voltages are shown without tolerances.

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Digital Multimeter	HP 3466A
Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
Adapter Probe	HP 1250-1598
Adapter N(f) to BNC(m)	HP 1250-0077
Adapter BNC(f) to BNC(f)	HP 1250-0080
Cable BNC(m) to SMC(f)	HP 08662-60075

⟨✓1⟩ Voltage Controlled Oscillator, Limiter Amplifier and 110 MHz Low-Pass Filter

1. Set the Signal Generator as follows:

Frequency	80 MHz
Amplitude	−10 dBm
Modulation	Off

2. Set the measuring receiver with the sensor module precalibrated as follows:

Measurement	RF POWER
Display	LOG

3. Zero the measuring receiver and wait for the zero LED to go out.
4. Change the Signal Generator's frequency to 90 MHz. This ensures the frequency of the Low Frequency Loop VCO to be 60 MHz.

5. Measure frequency, tune voltage and power levels at each point indicated in Table 1.

NOTE

When probing the VCO with the covers removed, a frequency shift may be introduced.

6. Measure Residual FM using the measuring receivers 300 Hz and 3 kHz high-pass and low-pass filters, and RMS Detector. The Residual FM should be less than 3 Hz for all frequencies.
7. Measure Residual FM using the measuring receivers 50 Hz and 15 kHz high-pass and low-pass filters and RMS Detector. The Residual FM should be less than 5 Hz for all frequencies.

Table 1. VCO Frequency, Power Output and Tune Voltage.

Frequency (MHz)		VCO Tune Voltage at C16 (Vdc)	Power Level at J1 (dBm)
Front-Panel Setting	VCO Output (at J1)		
90	60	+9 to +7	−4.5 to −6.5
85	65	+8 to +6	−4.5 to −6.5
80	70	+6 to +4	−4.5 to −6.5
75	75	+5 to +3	−4.5 to −6.5
70	80	+3.5 to 1.5	−5.0 to −7.0
65	85	+2.0 to 0.0	−5.0 to −7.0
60	90	+1.0 to −1.0	−5.5 to −7.5
55	95	−0.5 to −2.5	−5.5 to −7.5
50	100	−1.5 to −3.5	−5.5 to −7.5
45	105	−3.0 to −5.0	−5.5 to −7.5
40	110	−5.0 to −7.0	

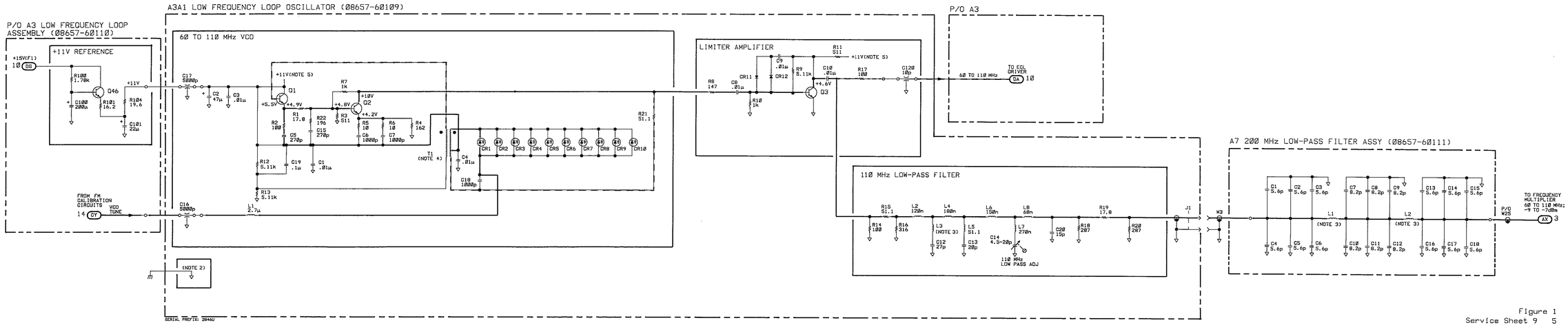


Figure 1
Service Sheet 9 5

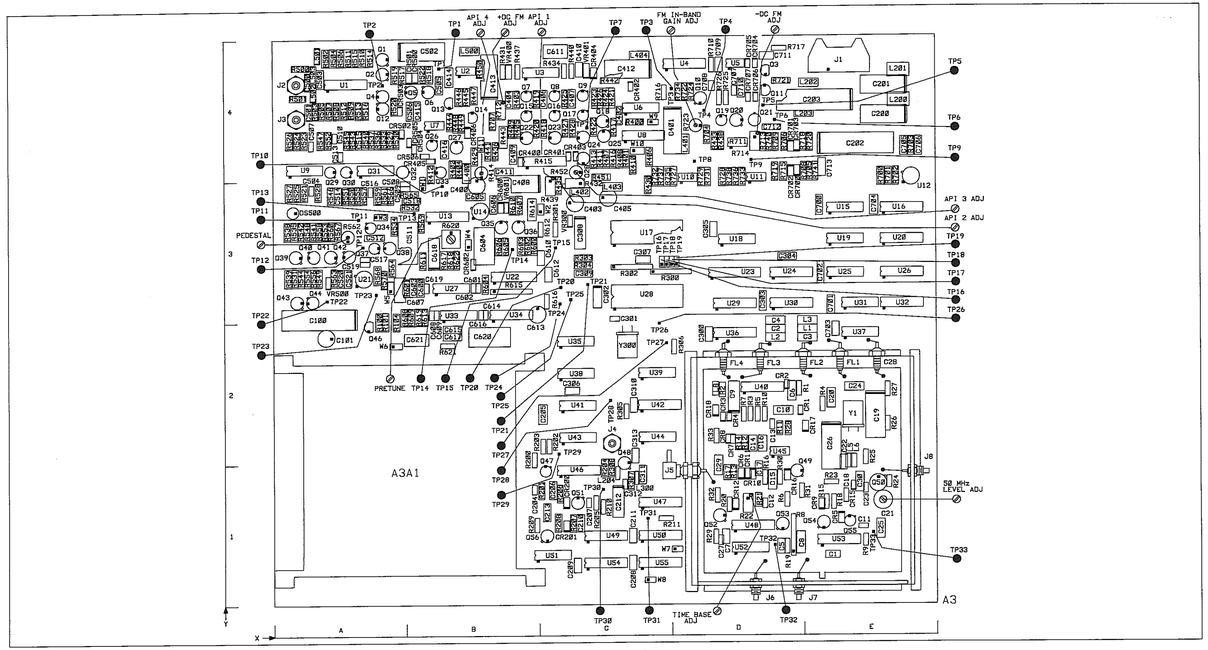


Figure Ø. Service Sheet 1Ø Information

Component Locator

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Nominal value of RF choke is 2.5-6uH.
3. Chassis ground is achieved by mechanical contact through nuts holding PC board to cover and W4.
4. Reference designations on this service sheet C, CR, L and R have numbers ranging from 200 to 299 only.
5. Wide-band RF choke approximately 6uH.

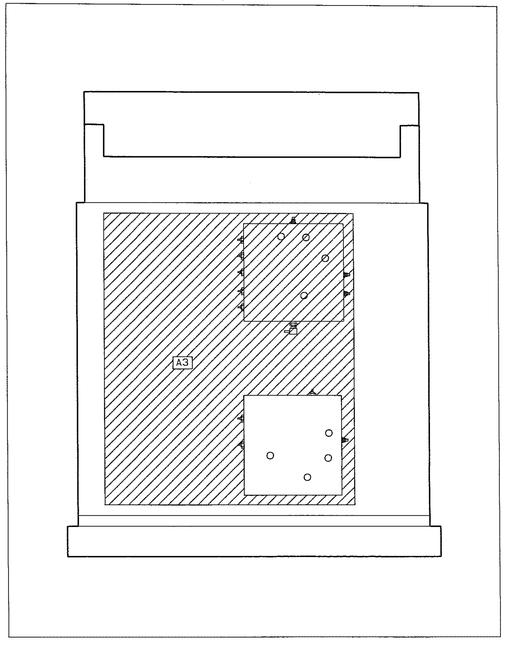
LOGIC LEVELS

	TTL	ECL
HIGH	2V	+4.2V
LOW	Ø.8V	+3.3V
IS MORE NEG. THAN IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

P/O A3, A3A1, A7 LOW FREQUENCY LOOP VOLTAGE CONTROLLED OSCILLATOR

SEE REVERSE SIDE

SS9



Service Sheet 10

LOW FREQUENCY LOOP DIVIDE-BY-2, AND PRESCALER

PRINCIPLES OF OPERATION

General

The VCO's output, 60 to 110 MHz, passes through Buffer Amplifier Q47, and is divided-by-2 at U46A. The output frequency of the Divide-By-2 circuit is 30 to 55 MHz, and is the clock for the Prescaler. The Prescaler divides the 30 to 55 MHz frequencies by 9, 10 or 11. The Prescaler is a variable 4-to-6-bit ring-counter followed by a divide-by-2 circuit. In the divide-by-10 mode, the ring-counter is set to modulus 5, and the Divide-By-2 circuit makes the total divisor equal to 10. In the divide-by-11 mode, the ring-counter is set to modulus 6 for one cycle, and to modulus 5 for another cycle of the Prescaler. After 2 cycles, the result is a divide-by-11. In the divide-by-9 mode, the ring-counter is set to modulus 4 for one cycle, and to modulus 5 for another cycle of the Prescaler. After 2 cycles, the result is a divide-by-9.

The modulus of the ring-counter is controlled by the Remove Cycle, and the Add Cycle control inputs. A high on the Remove Cycle control input changes the modulus of the Prescaler to 6, by controlling the K input of U54A. As long as the Remove Cycle control input is high, the modulus of the Prescaler is 6 for one cycle, and 5 for another cycle; the Prescaler divides-by-11. A high on the Add Cycle control input changes the modulus to 4, by controlling the K input of U54B. As long the Add Cycle control input is high, the modulus of the Prescaler is 4 for one cycle, and 5 for another cycle; the Prescaler divides-by-9. If both inputs are high, the Prescaler modulus is 4 (an unwanted state).

The Remove and Add Cycle inputs are used for the following purposes:

- The Remove Cycle, Divide-By-11, is set high by the Fractional-N IC to generate fractional frequencies, and by the FM Digital circuits to control frequency modulation.
- The Add Cycle, Divide-By-9, is set high by the FM Calibration circuits and by the FM Digital circuits to control frequency modulation.

Buffer Amplifier and Divide-By-2

The VCO's output, 60 to 110 MHz, is ac coupled by C204 to the base of Buffer Amplifier Q47. Q47 is dc biased at the collector for approximately +3.5 Vdc. The VCO's input voltage causes the collector voltage to cross valid ECL logic levels < +3.3V and > +4.2V. The ECL high and low output clocks the divide-by-2 master-slave D flip-flop U46A on each low to high transition. Thus, the output of U46A toggles dividing the input frequency by 2, and making the output frequency 30 to 55 MHz. Transistor Q51 translates the ECL logic levels to TTL logic levels. The output of U46A toggles Q51 on and off changing its collector voltage from approximately 0 Vdc (TTL low), to approximately +3.5 Vdc (TTL high). Buffer Driver Q56 buffers the output of Q51, and with U51D provides the drive required for the Prescaler.

Prescaler

The 30 to 55 MHz output clocks the Prescaler. U49, U50, and U54 have their set and reset inputs disabled; thus, their output state is dependent upon the J, K, and clock inputs.

Divide-By-10

The Prescaler divides-by-10 when the Add Cycle control input, and the Remove Cycle control input are both low. The ring-counter modulus is 5 for all cycles of the Prescaler. The timing diagram for this mode is shown in Figure 1.

The J inputs to U55A and U55B are low, and the K, set, and reset inputs are hard-wired high. U55A and U55B are clocked on the high to low transition of U50A's Q output, the output of the ring-counter. The high K and low J inputs of U55A and U55B sets their Q outputs low and not Q outputs high, but only after the ring-counter has completed a cycle and is reset. After the first Prescaler cycle the output state of U55A and U55B does not change when clocked. The inputs to U51B are both high, its output and the K input of U54A is low. With the J input of U54A connected to +5 Vdc, its Q output is clocked high on the next VCO divide-by-2 clock at time T1. The inputs to U51C are high at pin 9 and low at pin 8, its output and the K input of U54B is low. Since the J input to U54B was just clocked high, the next clock pulse at time T2 sets its output high. The output of U54A remains high until the Remove Cycle control input is set high. The high Q output of U54B is clocked through the ring-counter to the Q output of U50A at time T3. The low output of U50A sets the input of U51C at pin 9 low, its output and the K input of U54B is set high. The K inputs of U49A, U49B and U50A are set high by the Q output of U50A, on the next VCO divide-by-2 clock their Q outputs are all toggled low at time T4. The output of the ring-counter sets the J and K inputs of the divide-by-2 flip-flop U50B high. U50B is toggled at the end of each ring-counter cycle when both J and K inputs are high at time T4. The Q output of U54A remains high, and on the next clock the Q output of U54B is clocked high at time T5 and the high is clocked through to U50A. The cycle is repeated until a high is received at the Remove or at the Add Cycle control input instructing the Prescaler to remove or add a cycle.

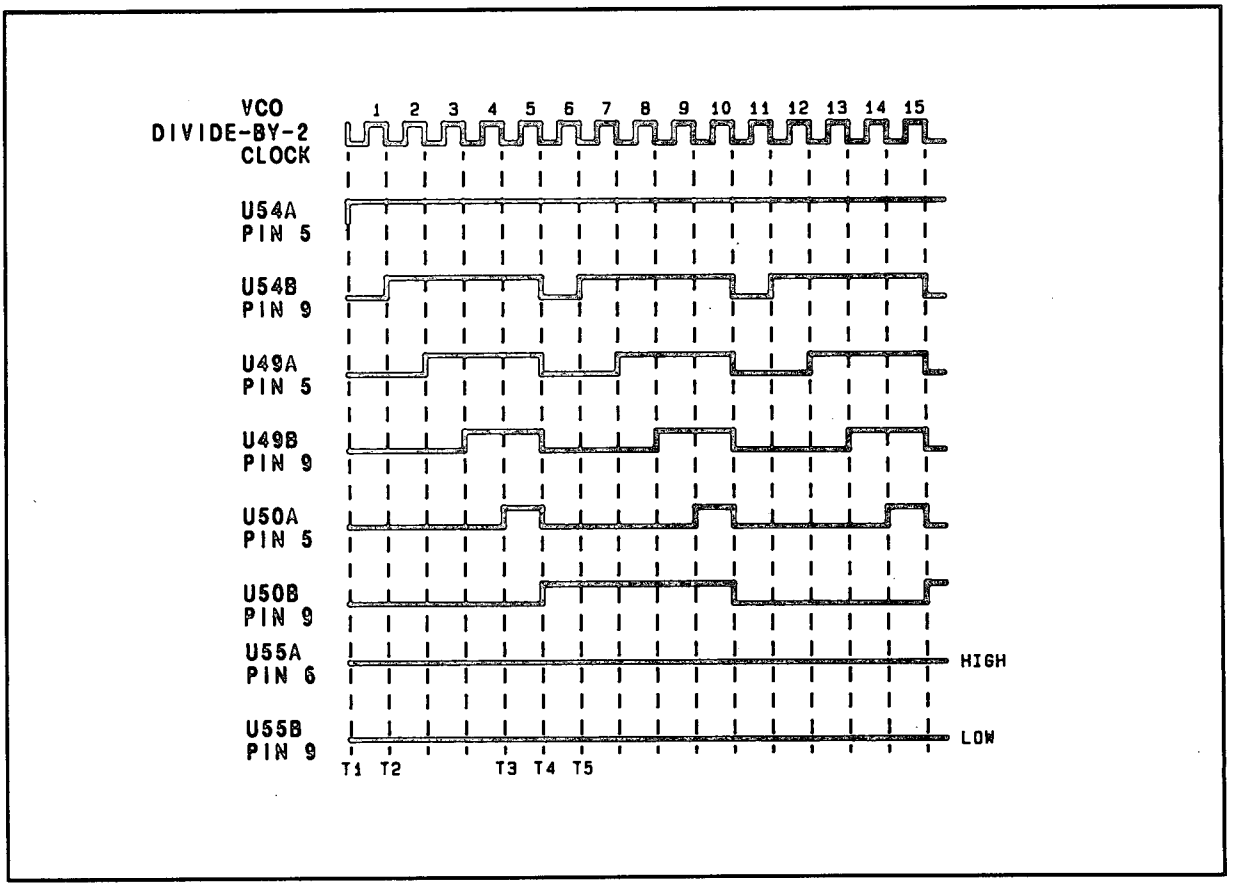


Figure 1. Divide-by-10 Timing Diagram.

Divide-By-11

The Prescaler divides-by-11 when the Remove Cycle control input is high, and the Add Cycle control input is low. The ring-counter's modulus is changed to 6 for one cycle, and to 5 for the next cycle of the Prescaler. The timing diagram for the divide-by-11 mode is shown in Figure 2.

With the J and K inputs to U55A high, when clocked the outputs toggle for each Prescaler cycle. The ring-counter's modulus also toggles from 6 to 5 each Prescaler cycle, and the Prescaler divides-by-11. This cycle is repeated until the Remove Cycle control input is set low. U55A is clocked on the high to low transition of U50A's Q output; at T2, the end of the Prescaler cycle. At time T1 the input at pin 5 of U51B is high, and the input at pin 6 is low. The K input to U54A is low and remains low until the not Q output of U55A is clocked low at time T2. The ring-counter remains in modulus 5 for the next cycle of the Prescaler. The K input to U54A is still low and at time T2 its Q output remains high. The Q output of U54B is toggled low, the not Q output of U55A is toggled low, and the Q output of U50B is toggled high. The VCO frequency is divided-by-5. At time T3, the Q output of U50A is high, and the not Q output is low. Both inputs to U51B are low, its output and the K input of U54A is high. The J and K inputs to U54A are both high and, its Q output is toggled low by the next clock at time T4. The K inputs of U49A, U49B, and U50A are set high by the high Q output of U50A. The next VCO divide-by-2 clock at time T4 toggles their Q outputs low. The Q output of U50A also sets the J and K inputs of the divide-by-2 J/K flip-flop U50B high at time T3. Its output is toggled low at time T4. The Q output of U54A remains low for one clock cycle, and is clocked high at time T5. The J and K inputs of U54B, U49A, U49B and U50A remain low. Their output does not change states when they are clocked. On the next clock, U54A's Q output is toggled high and is clocked through the ring-counter to the output of U50A. The modulus was changed to 6 for this Prescaler cycle with the added clock to toggle U54A. Figure 2 shows the 6 clock cycles between time T4 and T6. The high Remove Cycle control input is set low and the J input of U55A is low. The Q output of U50A clocks the not Q output of U55A high at time T4. The K input of U54A is low, and its output remains high. The ring-counter's modulus is changed to 5 at time T6, and remains in modulus 5 until an active Remove or Add Cycle control input is received.

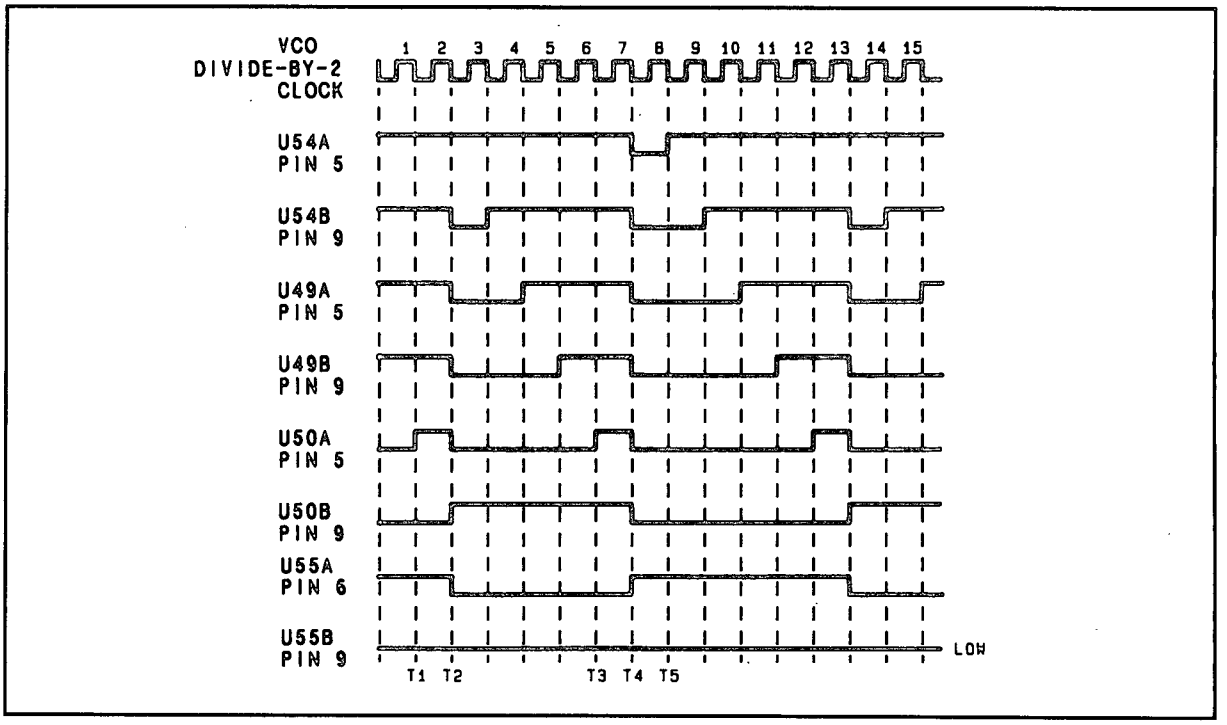


Figure 2. Divide-by-11 Timing Diagram.

Divide-by-9

The Prescaler divides-by-9 when the Add Cycle control input is high, and the Remove Cycle control input is low. The ring-counter's modulus is changed to 4 for one cycle, and to 5 for the next cycle of the Prescaler. The timing diagram for the divide-by-9 mode is shown in Figure 3.

With the J and K inputs to U55B high, when clocked, the outputs toggle for each Prescaler cycle. The ring-counter's modulus also toggles from 4 to 5, and the Prescaler divides-by-9. This cycle is repeated until the Add Cycle control input is set low. At time T1, both inputs to U51C are low and its output is high. The K input to U54B is still high at time T2. At time T2 the Q output of U55B is toggled high, and the Q output of U50A is toggled low. The ring-counter's modulus is still 5. The K input to U54A remains low, and its output remains high. The Q output of U54B is toggled low. The Q output of U55B is toggled high, and the Q output of U50B is toggled high. At time T3, the Q output of U50A is high, and the not Q output is low. The input of U51C at pin 9 is low. The input at pin 8 is high, set high by the Add Cycle input latched into U55B at time T2. The output of U51C (the K input of U54B) goes low. The Q output of U54B will not change when clocked at time T4. The K inputs of U49A, U49B and U50A are set high by the high Q output U50A at time T3. The VCO divide-by-2 clock at time T4 toggles their Q outputs low, and toggles the Q output of U50B low. The ring-counter's modulus is 4. The Q output of U54B is not reset low at time T4. The Q output of U49A is toggled low for one cycle at time T4, and high at time T5. The high Q output of U49A is clocked through to the Q output of U50A at time T6. The high Add Cycle input is removed, and the Q output of U55B is clocked low at time T4. Both inputs to U51C are low at time T6. U51C's output, the K input to U54B is high. Therefore, on the same clock that toggled the Q outputs of U49A, U49B, and U50A low, the output of U54B is toggled low at time T7. On the next clock the Q output of U54B is clocked high, and the high is clocked through to U50A. The ring-counter's modulus is changed to 5 at time T7, and remains in modulus 5 until an active Remove or Add Cycle control input is received.

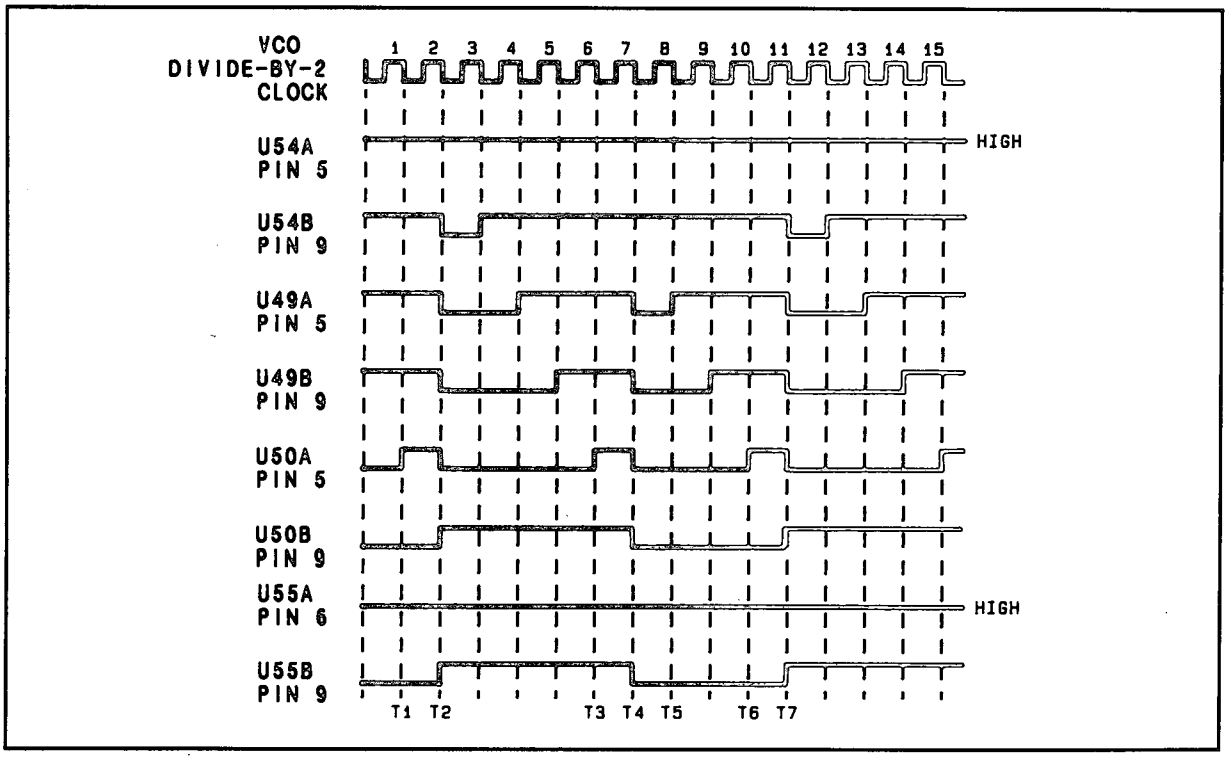


Figure 3. Divide-by-9 Timing Diagram.

TROUBLESHOOTING

Procedures for checking part of the A3 Low Frequency Loop Assembly circuits are given below. Areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, for example, ⟨✓1⟩ The frequencies shown on the schematic for Test Points 29, 30, and 31 are present when the Low Frequency Loop is locked.

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Frequency Counter	HP 5328A
Oscilloscope	HP 54100A
Oscilloscope Active Probe	HP 54001A

⟨✓1⟩ Buffer Amplifier

1. Remove jumper A3W6 (refer to Service Sheet 14). The VCO TUNE voltage goes to approximately 0.0V.
2. Connect the frequency counter to A3TP29 and measure the VCO frequency. The VCO frequency should be 96 MHz ±7 MHz.

NOTE

The ground connection to the counter probe must be as short as possible. If the counter does not count the 100 MHz, check the signal with the oscilloscope. Signal level is approximately 0.6 Vpp at A3TP29, and at ECL levels (low < +3.3V, high > +4.2V).

⟨✓2⟩ Divide-BY-2 and ECL to TTL

1. Connect the frequency counter to A3TP30 and measure the VCO frequency divided-by-2.
2. If the frequency is not correct, the outputs of Q51, and U51D should be checked.
   a. Q51's base VCO frequency is divided-by-2 and is at approximately 2.2 to 3.4 Vpp.
   b. Q51's collector voltage is at approximately 0.0 to 2.4 Vpp.
   c. U51D at pin 13 is approximately 1.0 to 3.4 Vpp.

⟨✓3⟩ Prescaler

1. Connect the frequency counter to A3TP31, and measure the VCO frequency divided-by-20.
2. If the frequency is not correct, check the frequencies shown in Tables 1, 2, and 3. (The frequencies shown in the tables are approximate, and are dependent upon the frequency of the Low Frequency Loop VCO when the VCO TUNE voltage input is approximately 0.0V.)

NOTE

Jumper A3W6 must be removed. The VCO TUNE voltage is approximately 0.0V. The VCO frequency should be 96 MHz ±7 MHz (refer to check 1). In the active state, the outputs of the J/K flip-flops are changing and not fixed at a TTL high or a TTL low.

Table 1. Prescaler J/K Flip-Flop Output Add and Remove Cycle Controls Inactive Low.

J/K Flip-Flops	J/K Flip-Flops Output	
	State	Frequency
U55A Pin 6	Inactive	—
U55B Pin 9	Inactive	—
U54A Pin 5	Inactive	—
U54B Pin 9	Active	10 MHz
U49A Pin 5	Active	10 MHz
U49B Pin 9	Active	10 MHz
U50A Pin 5	Active	10 MHz
U50B Pin 9	Active	5 MHz

3. Remove A3W8, and connect U55A pin 3 to +5 Vdc. (The frequencies in Table 2 are approximate, and are dependent upon the Low Frequency Loop VCO frequency when the VCO TUNE voltage input is approximately 0.0V.)

Table 2. Prescaler J/K Flip-Flop Output Add Cycle Control (Inactive Low) and Remove Cycle Control (Active High).

J/K Flip-Flops	J/K Flip-Flops Output	
	State	Frequency
U55A Pin 6	Active	4.5 MHz
U55B Pin 9	Inactive	—
U54A Pin 5	Active	4.5 MHz
U54B Pin 9	Active	9 MHz
U49A Pin 5	Active	9 MHz
U49B Pin 9	Active	9 MHz
U50A Pin 5	Active	9 MHz
U50B Pin 9	Active	4.5 MHz

4. Remove A3W7, and connect U55B pin 11 to +5 Vdc. (The frequencies in Table 3 are approximate, and are dependent upon the Low Frequency Loop VCO frequency when the VCO TUNE voltage input is approximately 0.0V.)

Table 3. Prescaler J/K Flip-Flop Output Add Cycle Control (Active High) and Remove Cycle Control (Inactive Low).

J/K Flip-Flops	J/K Flip-Flops Output	
	State	Frequency
U55A Pin 6	Inactive	—
U55B Pin 9	Active	5.5 MHz
U54A Pin 5	Inactive	—
U54B Pin 9	Active	5.5 MHz
U49A Pin 5	Active	11 MHz
U49B Pin 9	Active	11 MHz
U50A Pin 5	Active	11 MHz
U50B Pin 9	Active	5.5 MHz

A3 Component Coordinates (1 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	E,1	C213	C,1	C513	A,4	CR1	D,2	FL1	E,2	Q10	D,4
C2	D,2	C300	D,2	C514	A,3	CR2	D,2	FL2	E,2	Q11	D,4
C3	E,2	C301	C,3	C515	A,4	CR3	D,2	FL3	D,2	Q12	A,4
C4	D,2	C302	C,3	C516	A,3	CR4	D,2	FL4	D,2	Q13	B,4
C5	D,1	C303	D,3	C517	A,3	CR5	E,1			Q14	B,4
C6	D,2	C304	D,3	C518	B,3	CR6	D,1	J1	E,4	Q15	B,4
C7	D,1	C305	D,3	C519	A,3	CR7	D,2	J2	A,4	Q16	C,4
C8	D,1	C306	C,2	C520	A,3	CR8	D,2	J3	A,4	Q17	C,4
C9	D,2	C307	C,3	C521	A,3	CR9	E,1	J4	C,2	Q18	C,4
C10	D,2	C308	C,3	C600	B,3	CR10	D,1	J5	C,1	Q19	D,4
C11	E,1	C309	C,3	C601	B,3	CR11	D,1	J6	D,1	Q20	D,4
C12	D,1	C310	C,2	C602	B,3	CR12	D,1	J7	E,1	Q21	D,4
C13	D,2	C311	C,1	C603	B,3	CR15	E,1	J8	E,2	Q22	B,4
C14	D,2	C312	C,1	C604	B,3	CR16	D,1			Q23	C,4
C15	D,1	C313	C,2	C605	B,3	CR17	E,2	L1	E,2	Q24	C,4
C16	D,2	C400	B,3	C606	B,3	CR18	D,2	L2	D,2	Q25	C,4
C17	D,1	C401	D,4	C607	B,3	CR200	C,1	L3	E,2	Q26	B,4
C18	E,1	C402	C,4	C608	B,3	CR201	C,1	L5	E,2	Q27	B,4
C19	E,2	C403	C,3	C609	B,3	CR400	B,4	L6	E,2	Q28	C,4
C20	E,2	C404	B,4	C610	C,3	CR401	C,4	L8	D,2	Q29	A,4
C21	E,1	C405	C,3	C611	C,4	CR402	C,4	L200	E,4	Q30	A,4
C22	E,2	C406	C,4	C612	C,3	CR403	C,4	L201	E,4	Q31	A,4
C23	E,1	C407	C,4	C613	B,3	CR404	C,4	L202	E,4	Q32	A,4
C24	E,2	C408	B,3	C614	B,3	CR405	B,4	L203	E,4	Q33	B,4
C25	E,1	C409	B,4	C615	B,2	CR406	B,4	L204	C,1	Q34	A,3
C26	E,2	C410	C,4	C616	B,3	CR500	B,4	L300	C,1	Q35	B,3
C27	D,1	C411	B,4	C617	B,2	CR501	B,4	L400	B,4	Q36	B,3
C28	E,2	C412	C,4	C618	B,3	CR502	A,4	L401	D,4	Q37	A,3
C29	D,1	C413	B,4	C619	B,3	CR503	A,4	L402	C,3	Q38	A,3
C30	E,1	C414	B,4	C620	B,2	CR504	B,4	L403	C,3	Q39	A,3
C100	A,3	C415	B,4	C621	B,2	CR505	B,4	L404	C,4	Q40	A,3
C101	A,2	C416	B,4	C700	E,3	CR506	B,4	L500	B,4	Q41	A,3
C200	E,4	C500	A,4	C701	E,3	CR600	B,3	L501	A,4	Q42	A,3
C201	E,4	C501	A,4	C702	E,3	CR602	B,3	L502	A,4	Q43	A,3
C202	E,4	C502	B,4	C703	E,2	CR700	D,4	L503	A,4	Q44	A,3
C203	E,4	C503	A,4	C704	E,3	CR701	D,4			Q46	A,2
C204	B,1	C504	A,3	C705	E,4	CR702	D,4	Q1	A,4	Q47	C,1
C205	C,2	C505	B,4	C706	E,4	CR703	D,4	Q2	A,4	Q48	C,2
C206	C,1	C506	B,4	C707	D,4	CR704	D,4	Q3	D,4	Q49	D,1
C207	C,1	C507	A,4	C708	D,4	CR705	D,4	Q4	A,4	Q50	E,1
C208	C,1	C508	B,3	C709	D,4	CR706	D,4	Q5	B,4	Q51	C,1
C209	C,1	C509	B,3	C710	D,4	CR707	D,4	Q6	B,4	Q52	D,1
C210	C,1	C510	A,4	C711	D,4			Q7	B,4	Q53	D,1
C211	C,1	C511	B,3	C712	D,4			Q8	C,4	Q54	E,1
C212	C,1	C512	A,3	C713	E,4	DS500	A,3	Q9	C,4	Q55	E,1

A3 Component Coordinates (2 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
Q56	C,1	R207	C,1	R431	B,4	R523	A,4	R568	A,3	R719	D,4
		R208	C,1	R432	C,3	R524	A,4	R569	B,3	R720	E,4
R1	D,2	R209	B,1	R433	D,4	R525	A,3	R570	A,3	R721	D,4
R2	D,2	R210	C,1	R434	C,4	R526	A,4	R600	B,3	R722	D,4
R3	D,2	R211	C,1	R435	C,3	R527	A,3	R601	B,3	R723	D,4
R4	E,2	R300	C,3	R436	B,4	R528	A,3	R602	B,3	R724	D,4
R5	D,2	R301	C,3	R437	B,4	R529	A,4	R603	B,3	R725	D,4
R6	D,1	R302	C,3	R438	D,4	R530	A,4	R604	B,3	R726	D,4
R7	D,2	R303	C,3	R439	C,3	R531	A,3	R605	B,3	R727	D,4
R8	D,1	R304	C,3	R440	C,4	R532	B,3	R606	B,3	R728	D,4
R9	E,1	R305	C,2	R441	B,4	R533	A,4	R607	B,3	R729	D,4
R10	D,2	R306	D,2	R442	C,4	R534	A,3	R608	A,3	R731	D,4
R11	D,2	R307	C,1	R443	B,4	R535	A,3	R609	B,3	R732	C,4
R12	D,2	R308	C,1	R444	B,4	R536	A,4	R610	B,3	R733	D,4
R13	D,1	R400	C,4	R445	B,4	R537	A,4	R611	B,3	R734	D,4
R14	D,2	R401	C,4	R446	B,4	R538	A,3	R612	C,3	R735	C,4
R15	E,1	R402	B,4	R447	B,4	R539	A,3	R613	B,3	R736	D,4
R16	D,1	R403	B,4	R448	B,4	R540	A,4	R614	B,3	R737	C,4
R17	D,1	R404	B,4	R449	B,4	R541	A,3	R615	B,3	R738	D,4
R18	E,1	R405	B,4	R450	B,4	R542	A,3	R616	C,3	R740	D,4
R19	D,1	R406	C,4	R451	C,4	R543	A,4	R617	B,3	R741	E,4
R20	D,1	R407	C,4	R452	C,4	R544	A,3	R618	B,3		
R21	D,1	R408	C,4	R500	A,4	R545	A,4	R619	B,3	TP1	B,4
R22	D,1	R409	B,4	R501	A,4	R546	A,3	R620	B,3	TP2	A,4
R23	E,1	R410	C,4	R502	A,4	R547	A,4	R621	B,2	TP3	D,4
R24	E,1	R411	C,4	R503	A,4	R548	A,3	R622	B,3	TP4	D,4
R25	E,2	R412	B,4	R504	A,4	R549	A,3	R700	E,4	TP5	D,4
R26	E,2	R413	C,4	R505	A,4	R550	A,3	R701	E,4	TP6	D,4
R27	E,2	R414	B,4	R506	A,4	R551	A,3	R702	E,4	TP7	C,4
R28	D,2	R415	C,4	R507	A,4	R552	A,4	R703	E,4	TP8	D,4
R29	D,1	R416	C,4	R508	A,4	R553	A,3	R704	D,4	TP9	D,4
R30	D,1	R417	C,4	R509	A,4	R554	A,3	R705	E,4	TP10	B,3
R31	D,1	R418	C,4	R510	A,4	R555	A,3	R706	D,4	TP11	A,3
R32	D,1	R419	B,4	R511	A,4	R556	A,3	R707	B,4	TP12	A,3
R33	D,2	R420	B,4	R512	A,4	R557	A,3	R708	E,4	TP13	B,3
R100	A,2	R421	C,4	R513	A,4	R558	A,3	R709	D,4	TP14	B,3
R101	A,2	R422	C,4	R514	A,4	R559	A,3	R710	D,4	TP15	C,3
R104	A,2	R423	C,4	R515	A,4	R560	A,3	R711	D,4	TP16	C,3
R200	B,2	R424	C,4	R516	A,4	R561	A,3	R712	B,4	TP17	C,3
R201	C,1	R425	C,4	R517	A,4	R562	A,3	R713	D,4	TP18	D,3
R202	C,2	R426	C,4	R518	B,4	R563	A,3	R714	D,4	TP19	D,3
R203	C,2	R427	C,4	R519	A,4	R564	A,3	R715	D,4	TP20	C,3
R204	C,1	R428	C,4	R520	A,4	R565	B,3	R716	C,4	TP21	C,3
R205	C,1	R429	B,4	R521	A,3	R566	A,3	R717	D,4	TP22	A,3
R206	C,1	R430	C,3	R522	B,4	R567	A,3	R718	E,4	TP23	A,3

A3 Component Coordinates (3 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
TP24	C,3	U35	C,2						
TP25	C,3	U36	D,2						
TP26	C,2	U37	E,2						
TP27	C,2	U38	C,2						
TP28	C,2	U39	C,2						
TP29	C,2	U40	D,2						
TP30	C,1	U41	C,2						
TP31	C,1	U42	C,2						
TP32	D,1	U43	C,2						
TP33	E,1	U44	C,2						
		U45	D,2						
U1	A,4	U46	C,1						
U2	B,4	U47	C,1						
U3	C,4	U48	D,1						
U4	D,4	U49	C,1						
U5	D,4	U50	C,1						
U6	C,4	U51	C,1						
U7	B,4	U52	D,1						
U8	C,4	U53	E,1						
U9	A,4	U54	C,1						
U10	D,4	U55	C,1						
U11	D,4								
U12	E,3	VR300	C,3						
U13	B,3	VR400	B,4						
U14	B,3	VR401	C,4						
U15	E,3	VR500	A,3						
U16	E,3	VR601	B,3						
U17	C,3								
U18	D,3	W1	B,3						
U19	E,3	W2	C,3						
U20	E,3	W3	A,3						
U21	A,3	W4	B,3						
U22	B,3	W5	A,3						
U23	D,3	W6	A,2						
U24	D,3	W7	D,1						
U25	E,3	W8	C,1						
U26	E,3	W9	C,4						
U27	B,3	W10	C,4						
U28	C,3	W11	B,4						
U29	D,3								
U30	D,3	Y1	E,2						
U31	E,3	Y300	C,2						
U32	E,3								
U33	B,3								
U34	B,3								

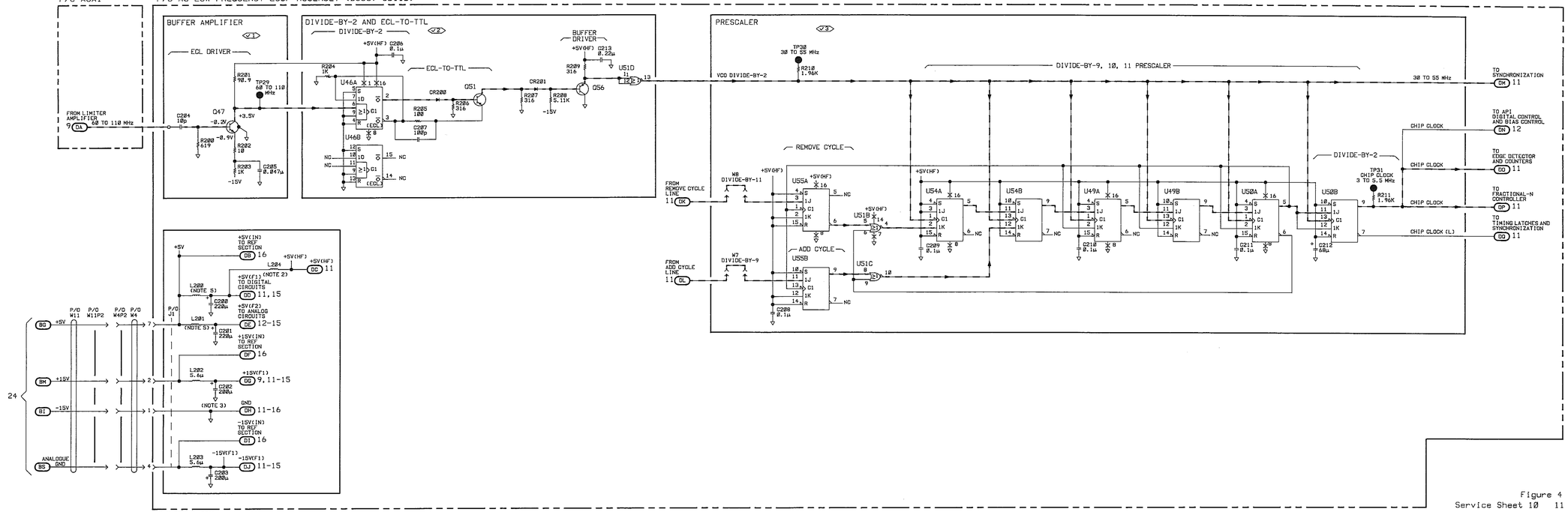


Figure 4
Service Sheet 10 11

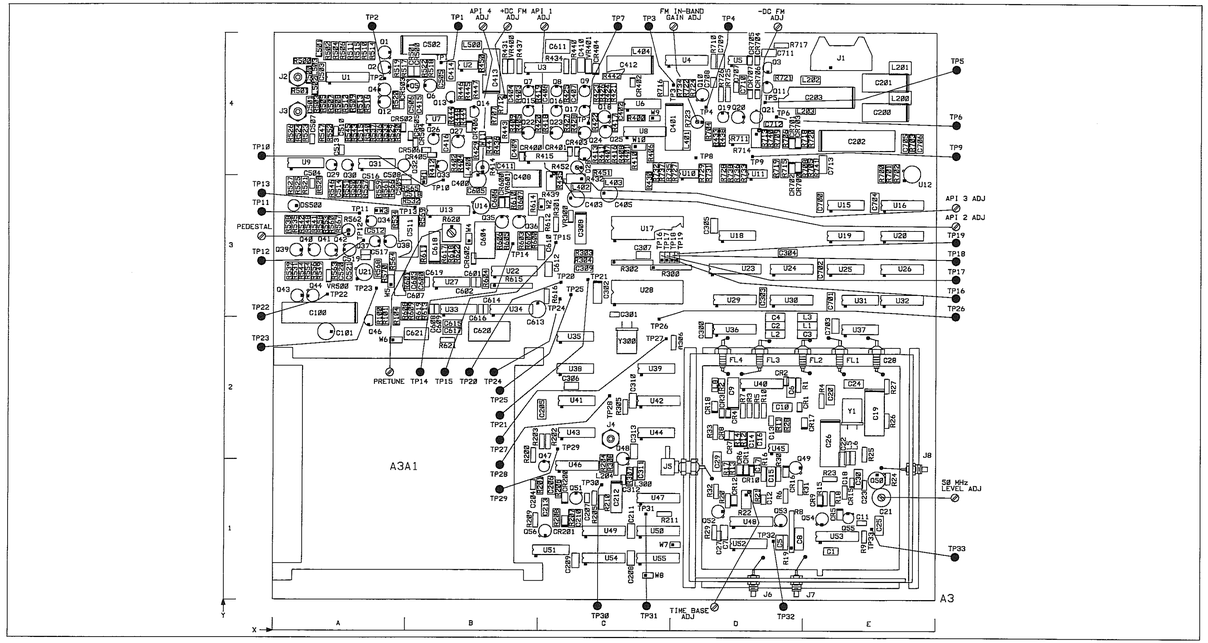


Figure Ø. Service Sheet 11 Information

Component Locator

NOTES

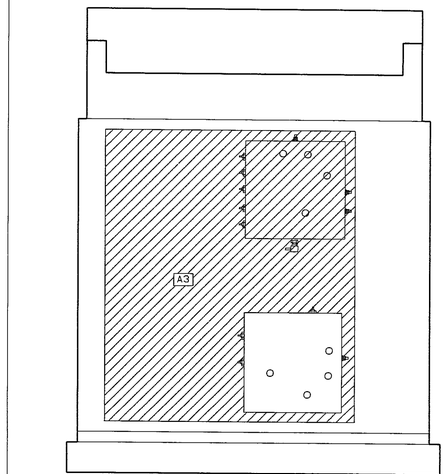
1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Nominal value of RF choke is 2.5-6uH.
3. Chassis ground is achieved by mechanical contact through nuts holding PC board to cover and W4.
4. Reference designations on this service sheet C, CR, L, R and VR have numbers ranging from 300 to 399 only.
5. Jumper for TP16-19 is installed only for troubleshooting.

LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	0.8V	1.5V
IS MORE NEG. THAN		
IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A3 LOW FREQUENCY LOOP DIVIDE-BY-2 AND PRESCALER SS1Ø

SEE REVERSE SIDE



Service Sheet 11

LOW FREQUENCY LOOP FRACTIONAL-N, DIVIDE-BY-N, AND DIGITAL TIMING LOGIC

PRINCIPLES OF OPERATION

General

Serial data is generated by the main Microprocessor A13U14 (refer to Service Sheet 17) A13U14 writes data to the Serial I/O Control Register A13U16 (refer to Service Sheet 18). Serial Low Frequency Loop data is passed through the LF Loop Serial Data Bus Buffer A13U4B (refer to Service Sheet 18) when it is enabled. Serial Data is transferred to the Low Frequency Loop when its frequency is changed, when frequency modulation (AC or DC) is selected, turned off, changed or calibrated, or when phase is incremented or decremented. An Out-Of-Lock status bit is transferred from the Low Frequency Loop to the Microprocessor Assembly during diagnostic tests. An automatic indication that the Low Frequency Loop is out-of-lock is displayed on the A3 assembly by a lit LED. Serial LF Loop Data (LDA) is clocked into the LF Loop Microprocessor A3U28 by the LF Loop Clock (LCL). Serial LF Loop Data is clocked into the LF Loop Microprocessor by active low LCL pulses. At the completion of the data transfer, the LF Loop Serial Data Bus Buffer is disabled and the LF Loop Clock is discontinued. Timing for data transfer and clock generation is firmware controlled.

Microprocessor

Serial LF Loop Data written to the LF Loop Microprocessor, U28 at pin 9, consists of instructions and data. The LF Loop Microprocessor uses a firmware routine to input the serial data, and to handle all timing constraints. Instructions and data transferred to the LF Loop Microprocessor tell the LF Loop what operations to perform. For example, some instructions select frequency modulation and calibration. Instructions and data sent to the Fractional-N Controller tell it what operation to perform. The LF Loop Microprocessor stores the data sent over the serial data bus and very quickly transfers it to the Fractional-N Controller as a series of four-bit words. The first word transferred is always an instruction followed by a 70 μs wait to assure that Fractional-N Controller has received a Cycle Start Pulse. Sixteen data words are then sent followed by an instruction word to define the data, and an instruction to terminate the data transfer.

The Microprocessor has three I/O Ports. Two eight-bit ports PA, PB and one four-bit port PC. The eight-bits of I/O port PA and four-bits of I/O port PB function as outputs. PA0 (pin 20) through PA3 (pin 23) transfer instructions and data words to the Fractional-N Controller, U17. PA4 (pin 24) is the external clock (EXT CLK) that clocks the data words into the Fractional-N Controller, and PA5 (pin 25) is the instruction valid (INST VLD) input that clocks the instructions into the Fractional-N Controller. Outputs PA6 (pin 26), PA7 (pin 27) and PB0 through PB3 (pins 12 through 15) enable frequency modulation, turn frequency modulation off, select DC FM and activate B+C(L) and S(L)/H1 control lines for frequency modulation calibration. The other four PB I/O Ports function as inputs. TP18 (PB5) and TP17 (PB6) are connected to ground to initiate microprocessor controlled service routines. The LF Loop Microprocessor mode input TP26 must also be grounded. TP16 (PB7) is not used. See Table 1 for further information.

With TP19 (PB4) connected to ground and TP26 not grounded the frequency switching speed is increased by eliminating the FM calibration cycle. Jumper W2 connecting the B+C(L) to U22 (refer to Service Sheet 14), must be removed also. The FM Calibration DAC (U34) is then set to 75% of its range. To exit the service routines, the instrument's POWER switch is set to STBY and then to ON.

An external 4 MHz crystal Y300 is directly connected to the LF Loop Microprocessor (pins 4 and 5). Capacitor C301 is used to keep the frequency stable. The Microprocessor converts the 4 MHz crystal to a 1 MHz clock.

Table 1. LF Loop Microprocessor Initiated Tests.

Test Point Grounded	TP26 Grounded	LF Loop Microprocessor Test Initiated
	Yes	Increment Signal Generator's frequency by 10 MHz. An FM calibration is performed every 100 mSec until ground is removed.
TP17	Yes	Signature Analysis
TP18	Yes	Low Frequency Loop VCO's frequency is set to 66.80001 MHz
TP19	No	No FM calibration with VCO's frequency changed, switching speed is increased.

The LF Loop Microprocessor can be RESET by briefly shorting TP21 (Reset) to TP20 (ground). The mode input for the LF Loop Microprocessor is the PC2 input (pin 10). The mode input is high for normal Low Frequency Loop operation. The special Low Frequency Loop service mode is entered when the instrument is powered up with the mode input TP26 grounded. Then, the LF Loop Microprocessor will not receive data or clock inputs from the main Microprocessor (A11U9). TP26 is grounded when TP17 or 18 are grounded to access the Low Frequency Loop service routines.

Fractional-N Controller

Six of the eight inputs to the Fractional-N Controller (U17) are the four data inputs (C1-C4), the instruction valid input (INST VLD), and the external clock input (EXT CLK). The other two inputs are the chip clock input (CHIP CLK), and the cycle start input (CYCLE START). CHIP CLK is the LF Loop VCO frequency divided-by-20, and is the output of the Prescaler at pin 9 of U50B. The Chip Clock frequency varies from 3.0 to 5.5 MHz and is the clock for the Fractional-N Controller. Cycle Start is the LF Loop VCO frequency divided-by-N.F. (refer to Block Diagram 3).Cycle Start is synchronized with the Chip Clock by the Cycle Start Synchronization flip-flop U19A. The Cycle Start input initiates a Fractional-N Controller cycle. The Cycle Start pulse is one Chip Clock long (refer to the Low Frequency Loop Timing Diagram, Figure 1). At the termination of the Cycle Start pulse, the Sample and Hold pulse at pin 11 is active for two Chip Clocks. The Low Frequency Loop VCO control voltage from the integrator is stored on the Sample and Hold Capacitor C519 (refer to Service Sheet 13). One Chip Clock after the Sample and Hold Pulse is terminated, the Bias Pulse at pin 10 is active for thirteen Chip Clocks. The Bias pulse is synchronized with the Chip Clock at flip-flop U6B (refer to Service Sheet 12), initiating the Delayed Bias Pulse. During the Bias Pulse, a current resets the LF Loop Integrator. The Integrator is readied for the next output from the Phase Detector. The Fractional-N Controller Analog Phase Interpolation (API) outputs, at pins 2 through 6, are active during the Bias Pulse. Each of the five API outputs is pulse width modulated to sum the correct current into the Integrator to compensate for Fractional-N (F.N.) variations in phase differences. F.N. phase difference variations occur when the LF Loop VCO frequency is not an even multiple of the 100 kHz reference. The Fractional-N Controller keeps track of the F.N. phase difference between the VCO divided-by-N.F. and the 100 kHz reference. When the phase difference changes by 360/N degrees, the Prescaler is instructed to remove a cycle. A cycle is removed by the Prescaler to compensate for fractional frequencies. A cycle is removed or added by the Prescaler when frequency modulating at large modulation indexes (m). The LF Loop Integrator is reset during the Bias Pulse by the Bias Current. Therefore, all Chip Clocks must be of equal length when Bias Current is on, and the Prescaler does not remove or add cycles. The Bias Pulse directs the Bias Current to the Integrator and closes the API FET switches (refer to Service Sheet 12). When the FET switches are open, the API currents are directed to the Phase Detector and FM Current Switches (refer to Service Sheets 13 and 14). Otherwise the API currents are directed to the API switches. The Integrator is reset before the next input from the Phase Detector is received. The Fractional-N Controller determines the pulse width of the API Pulses, and terminates the API Pulses one Chip

Clock before the end of the Bias Pulse (refer to Figure 1). The pulse width of the negative API Pulses varies when a fractional frequency is selected. A fractional frequency is any LF Loop frequency that is not an even multiple of the 100 kHz reference. The timing of the Remove Cycle input to the Prescaler is initiated when the API 1 pulse goes high. The data sent to the Fractional-N Controller includes the divide number for the Divide-By-N-Counters, U24, U30, and U36. The data is received as a four bit BCD number, changed to its nine's complement and sent serially least significant digit first to the nine's complement latches U23 and U29. The data is clocked into the latches by the Fractional-N Controller's divide-by-N clock output. The nine's complement data is then loaded into the Divide-By-N-Counters each 100 kHz cycle of the Low Frequency Loop, every 10 μs. U24, U30, and U36 function as up counters, their faster mode of operation.

Divide-By-N

The Divide-By-N-Counters use "Prescaler Counting" to divide the Low Frequency Loop VCO's frequency to 100 kHz pulses. The VCO frequencies of 60 MHz to 110 MHz are divided-by-N.F. (N.F. refers to the possible fractional division ratios using Fractional-N technology) to output a pulse every 10 μs. Prescaler counting does not require the use of high-speed counters for direct counting. The VCO's frequency is divided-by-2 and the Prescaler divides this frequency by 11 when the 100 kHz counter is counted, and by 10 otherwise.

Figure 2 shows the output of the counters when the Signal Generator's RF output is 800.2 MHz. The frequency of the Low Frequency Loop VCO is 99.80 MHz; 49 Chip Clocks are required for the 10 μs Low Frequency Loop cycle. The VCO frequency of 99.80 MHz divided-by-2 is 49.90 MHz. Less two 1 MHz counts for Cycle Start Synchronization, and reloading data into the Counters will give a divide number of 479 to the 100 kHz VCO Divided-By-N.F. input to the Phase Detector. The nine's complement of 479 is 520. At the completion of the Cycle Start Pulse (U19A), the first seven Chip Clocks count the 1 MHz counter from 2 to 9 . This counter is then repeatedly counted from 0 to 9, ten Chip Clocks, for the remaining Chip Clocks in a 10 μs cycle. Four clocks from the 1 MHz counter count the 10 MHz counter from 5 to 9, and nine Chip Clocks count the 100 kHz counter from 0 to 9 once each Low frequency Loop cycle.

The Chip Clock is the Low Frequency Loop VCO frequency divided-by-20 or divided-by-22. The VCO frequency is divided-by-22 when the 100 kHz counter is counting and the Prescaler's modulus is 11. The frequency of the Chip Clock is 4.990 MHz for 40 Chip Clocks and each clock is 0.2004 μs. The frequency of the Chip Clock is 4.536 MHz for 9 Chip clocks and each clock is 0.22044 μs.

$$(0.2004\ \mu s \times 40) + (0.22044\ \mu s \times 9) = 10\ \mu s$$

The nine's complement data held in the Latches (nine's Complement) is loaded into the 100 kHz, 1 MHz, and 10 MHz up Counters when their load input at pin 11 is set low. When the counters are loaded their carry output at pin 12 is set low. The enable input at pin 4 of the 100 kHz counter is active low and is controlled by its carry output at pin 12. The enable input at pin 4 of the 1 MHz counter is tied low and is therefore active. The enable input, at pin 4, of the 10 MHz counter is controlled by the Ripple Count output of the 1 MHz counter at pin 13. The Chip Clock input to the counters will begin to count the 100 kHz and 1 MHz counters up as soon as the data is loaded. At this time, the 10 MHz Counter is not enabled to count. Refer to the Counter Timing diagram, Figure 2. The 100 kHz Counter is enabled when its carry output is low. The carry output is set low on each cycle when the data is reloaded. The low carry output at pin 12 is connected to the enable input at pin 4. The low carry output that enables the 100 kHz Counter is also gated through the remove cycle gates of U41A, U41B, and U51A to set the Remove Cycle input to the Prescaler high. Each cycle of the Prescaler that the Remove Cycle input is high, the VCO Divided-By-2 input is divided-by-11. The Chip Clock counts the 100 kHz counter up to nine. The carry output and enable input are set high, and the counter is disabled until the next Low Frequency Loop cycle. The high carry output sets the output of U41A low, and the low is gated through the remove cycle gates to set the Remove Cycle input to the Prescaler low.

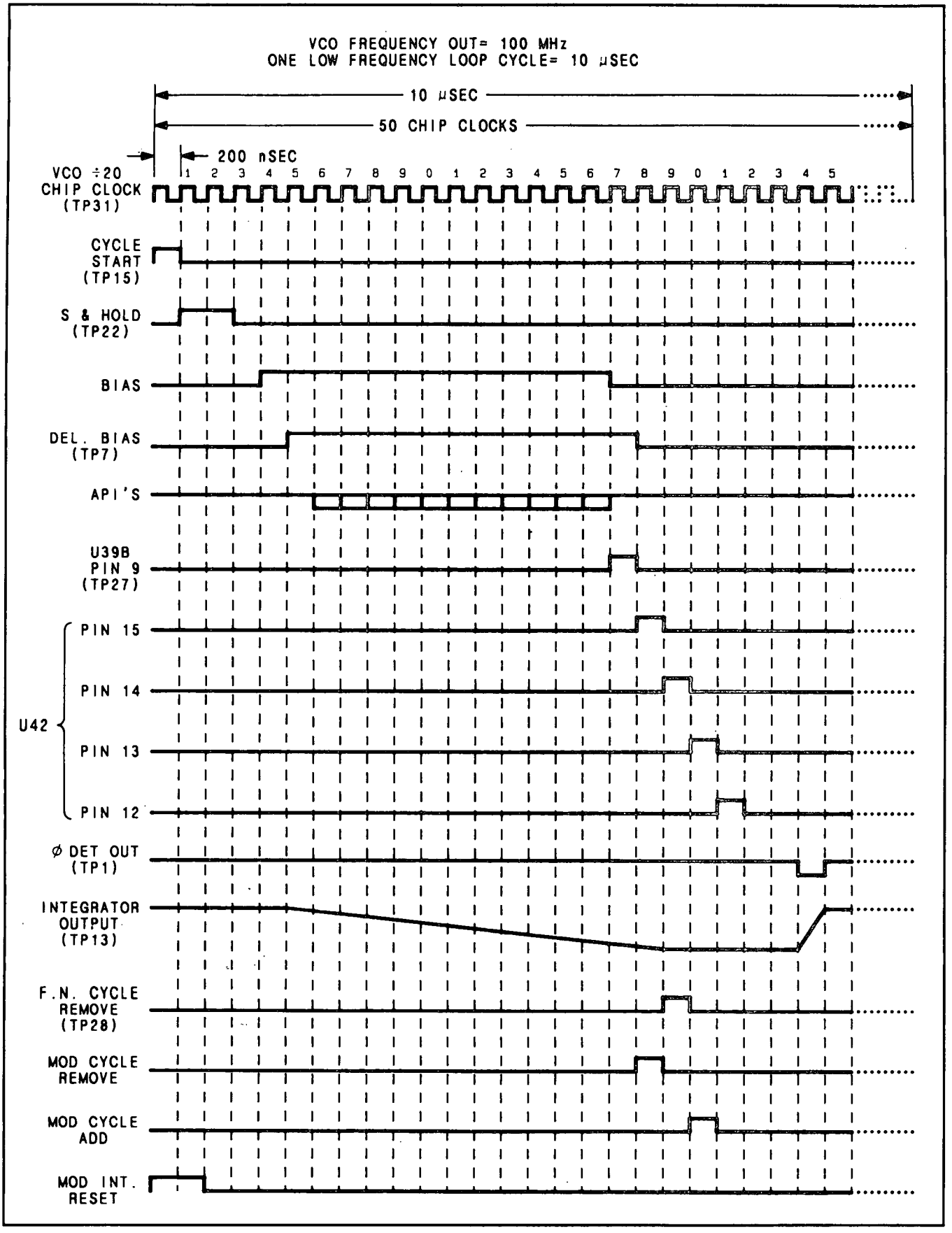


Figure 1. *Low Frequency Loop Timing Diagram.*

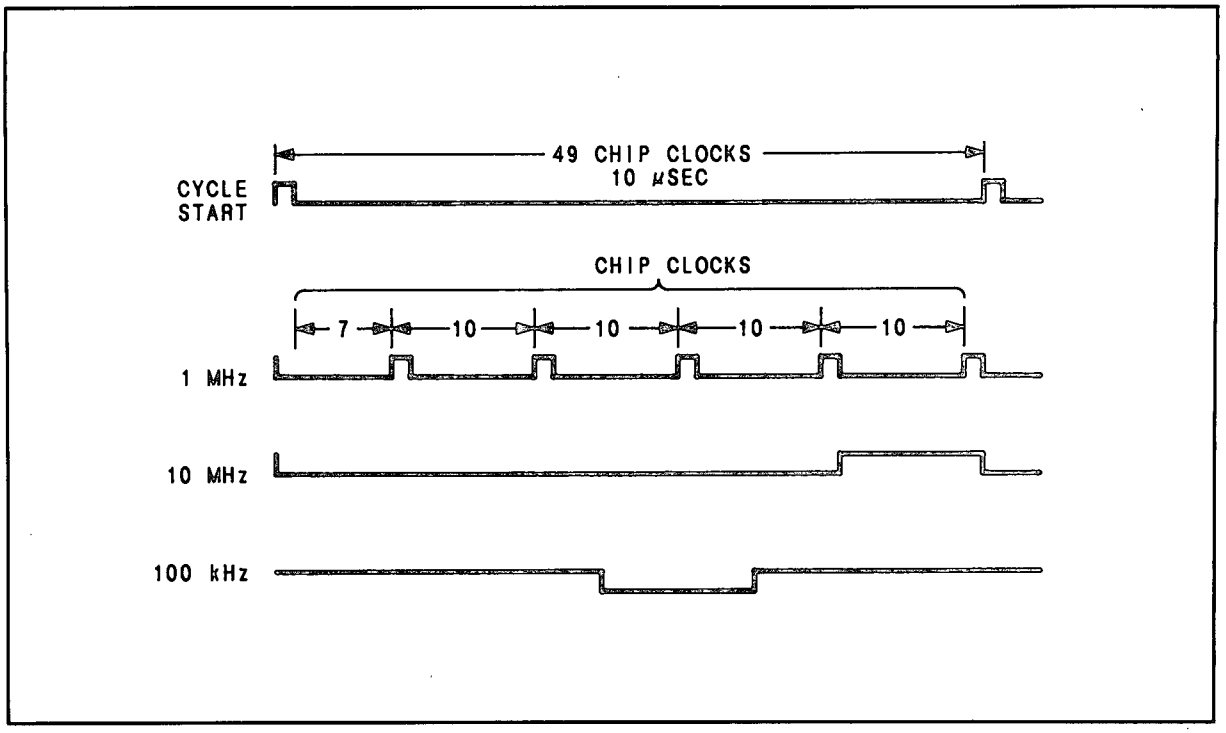


Figure 2. Counter Timing.

When the 1 MHz counter, U30, is counted up to nine, its ripple count output at pin 13 goes low, and the 10 MHz counter is enabled for one count. Each time the 1 MHz counter is counted up to nine, the 10 MHz counter is counted up one count. The carry output of U30, the 1 MHz counter, at pin 12 goes high for one count. The high output is one input to the AND gate U18C. The 1 MHz counter continues to count, and the 10 MHz counter is counted up to nine. The carry output at pin 12 is high. Both inputs to AND gate U18C are high at this time and its output is high. The D input to U19A is set high, and on the next Chip Clock the Q output is set high initiating the Cycle Start Pulse. The not Q output of U19A is low and the load enable input at pin 11 for the 1 MHz and the 10 MHz counters is low. The data in Latch, U23, is loaded in the 1 MHz and 10 MHz counters. The two counters are ready for the next Low Frequency Loop cycle. The carry output of the counters is set low when they are reloaded. The inputs to AND gate U18C are low and the output of U18C is returned to the low state. On the next Chip Clock, the outputs of U19A are set pin 5 low and pin 6 high terminating the Cycle Start pulse and disabling the 1 MHz and 10 MHz counters load input. The Cycle Start Synchronization circuit, U18C and U19A synchronize the Cycle Start pulse with the Chip Clock which is required for high speed operation of the counters. The synchronization takes two Chip Clocks, and the number loaded into the 1 MHz counter is two less. When the RF output frequency of the Signal Generator is 733.2 MHz, the frequency of the Low Frequency Loop VCO's frequency is 66.8 MHz. The nine's complement loaded into the latches is 685. The Low Frequency Loop VCO frequency is divided-by-2 (refer to Service Sheet 10), for a frequency of 33.4 MHz. Then 2 MHz is subtracted for Cycle Start Synchronization, 33.4 MHz – 2.0 MHz = 31.4 MHz. The nine's complement of 314 is 685.

Digital Timing Logic

The Cycle Start pulse is received by the Fractional-N Controller, and a Low Frequency Loop cycle is started. The Fractional-N Controller sends out the Sample and Hold, Bias, and API outputs as previously described. When the negative API 1 pulse is terminated, the low to high transition clocks the Edge Detector's U39A output at pin 5 high. The high output is applied to the D input of U39B. U39B's output at pin 9 is clocked high, and its output at pin 8 low by the next Chip Clock. The low output at pin 8 is applied to the Reset input of U39A at pin 1, and the output at pin 5 of U39A is reset low. The D input of U39B then goes low. On the next Chip Clock, the output at pin 9 of U39B is set low

and the output at pin 8 high. The positive pulse which was generated from pin 9 of U39B is applied to the Timing Latches shift register U42 at pin 2. The pulse is clocked through the shift register, by the Chip Clock(L), to the outputs at pins 15, 14, 13, and 12. The output at pin 15 sets U43B's input pin 5 high and, enables a frequency modulation remove cycle high input at pin 4 to be gated to the Prescaler. The output at pin 14 sets U43D's input at pin 12 high, and enables a Fractional-N remove cycle high input at pin 13 to be gated to the Prescaler. The output at pin 13 sets U43C's input at pin 9 high, and enables a frequency modulation add cycle high input at pin 10 to be gated to the Prescaler. The output at pin 13 is also applied to the J input of Synchronization J/K flip-flop U47A to resynchronize the Low Frequency Loop VCO Divide-By-N.F. input to the Phase Detector. The output at pin 12 is applied to the D input of U44B. On the next Chip Clock, the high D input is clocked to the output at pin 9, and the output at pin 8 is clocked low. The output's of U44B are at this state for one cycle of the Chip Clock(L). The high output pulse from pin 9 of U44B is applied to the NOR gates U41A, and U35D to set their outputs low. The low output of U35D resets Cycle Remove Latch U38B. The low output pulse of U44B at pin 8 resets Cycle Add/Remove Latches U38A, and U44A. It also resets the Cycle Start Synchronization flip-flop U19A, and enables the load input at pin 11 of the 100 kHz counter.

The instructions to add or remove a cycle are latched into the Cycle Add/Remove Latches U38A, U38B and U44A. Cycles are added or removed during frequency modulation. Cycles are also removed when the Low Frequency Loop VCO is operating at a fractional frequency. The Fractional-N Controller U17 determines when a cycle is removed for fractional frequencies. The active Cycle Remove output at pin 12 clocks the Remove Cycle Latch U44A. The D input at pin 1 of U44A is tied high and is clocked to the output at pin 5. This is one input to AND gate U43D. As described above the output at pin 14 of the Shift Register U42 gates the output of U43D high which gates the output of NOR gate U41B low. The low output of U41B gates the output of U51A high and the Prescaler removes a cycle.

The High Threshold and Low Threshold inputs are activated during frequency modulation (refer to Service Sheet 15). The High Threshold cycle remove control is the D input at pin 12 of the Cycle Remove Latch U38B. The high D input is clocked to its output at pin 9 by the Cycle Start pulse. The output at pin 9 is one input to AND gate U43B, and is the Remove Cycle input to the FM Digital Circuits. As described above the output at pin 15 of the Shift Register U42 gates the output of U43B high which gates the output of NOR gate U41B low. The low output of U41B gates the output of U51A high and the Prescaler removes a cycle. Refer to the Timing Diagram, Figure 1. The Low Threshold cycle add control is the D input at pin 2 of Cycle Add Latch U38A. The high D input is clocked to its output at pin 5 by the Cycle Start pulse. The output at pin 5 is one input to AND gate U43C, and is the Add Cycle input to the FM Digital Circuits. As described above the output at pin 13 of the Shift Register U42 gates the output of U43C high, and the Prescaler adds a cycle.

Synchronization

The Synchronization J/K flip-flop's U47A and U47B resynchronize the Low Frequency VCO Divided-By-N.F. output pulse to the Phase Detector (refer to Service Sheet 13). As described above, the output at pin 13 of Shift Register U42 is applied to the J input of J/K flip-flop U47A at pin 3. The K input is then low. The next high to low transition of Chip Clock(L) clocks the output at pin 5 high and the output at pin 6 low. The high output at pin 5 is applied to the J input of J/K flip-flop U47B at pin 11. The K input at pin 12 is then low. The high to low transition of the VCO Divide-By-2 input at pin 13 clocks the output at pin 9 high. The output at pin 5 of U47A is also its K input at pin 2. The J input was set low when the high pulse of the Shift Register U42 was clocked through the register. The next high to low transition of Chip Clock(L) clocks the output at pin 5 low and the output at pin 6 high. The next high to low transition of the VCO Divide-By-2 input clocks the output at pin 9 of U47B low. When the output at pin 9 of U47B is high, transistor Q48 is turned off. The collector is connected to ground through resistor R308 and R500 (refer to Service Sheet 13). The output of Q48 is approximately 0.0 Vdc. On the high to low transition of U47B's pin 9 output, Q48 is turned on and its output is pulsed to approximately +4V. The Phase Detector is clocked on the low to high transition of the output of Q48. Capacitor C312 turns transistor Q48 on and off very quickly.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Procedures for checking part of the A3 Low Frequency Loop Assembly circuits are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, for example, ⟨✓1⟩. Troubleshooting is done on the LF Loop Microprocessor using Signature Analysis. The LF Loop's Microprocessor troubleshooting routines are used to check the Fractional-N Controller and the Divide-By-N-Counters.

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Signature Analyzer	HP 5005A
Audio Source	HP 8903B
Frequency Counter	HP 5328A
Oscilloscope	HP 54100A
Oscilloscope Probe	HP 54003-61617
Oscilloscope Active Probe, Chan 1	HP 54001A
Oscilloscope 1 Megohm Probe Pod, Chan 2	HP 54003A

⟨✓1⟩Low Frequency Loop Microprocessor

1. Connect the signature analyzer as follows:

GND	GND (See Note below)
CLK	DSA CLK A3TP24
START	DSA S/S A3TP25
STOP	DSA S/S A3TP25

NOTE

Connect to ground as close to the circuitry being probed as possible. Bad grounding can cause unstable signatures.

2. Set the signature analyzer's controls as follows:

CLK	Positive Edge
START	Positive Edge
STOP	Negative Edge

CAUTION

The LF Loop Clock input (LCL) at pin 2 and the LF Loop Data input (LDA) at pin 9 from the A11 Assembly must be opened before A3TP17 and A3TP26 are connected to ground. Open LCL and LDA inputs by removing W16 from A11J4. The LF Loop Microprocessor U28 does not require data from the main Microprocessor to run the signature analysis checks.

3. Set up the Signal Generator as follows:
   a. Connect A3TP26 to A3TP20 (ground).
   b. Connect A3TP17 to ground. Use the jumper provided.
   c. Turn the Signal Generator's POWER switch to STANDBY and then back to ON.
4. Connect the signature analyzer probe to each node indicated in Table 2 and verify that each signature is correct and stable.

   The alternate Microprocessor signatures at pins 14 and 20 to 27 check the input at pins 2, 8 to 11 and 16 to 19. When the input is low, the signature at the related pin is the alternate signature.

Table 2. Low Frequency Loop Microprocessor Signatures.

Node A3U28 Pin	Normal Signature	Alternate Signature	Alternate Signature Determining Factor
#1	0000	--	
#2	7U39	0000	Pin tied low
#3	7U39	--	
#6	0000	--	
#7	7U39	--	
#8	0000	--	
#9	0000	7U39	Pin pulled high
#10	7U39	0000	Pin tied low
#11	7U39	0000	Out-of-lock LED on
#14	0021	0020	Pin 2 low
#15	0010	40C5	RAM error
#16	7U39	0000	Pin tied low
#17	7U39	0000	Pin tied low
#18	7U39	0000	Pin tied low
#19	7U39	0000	Pin tied low
#20	2050	2052	Pin 8 low
#21	102C	1029	Pin 9 low
#22	0816	0814	Pin 10 low
#23	0408	040A	Out-of-lock LED on
#24	0201	0205	Pin 16 low
#25	0106	0102	Pin 17 low
#26	0085	0081	Pin 18 low
#27	0044	0040	Pin 19 low
#28	7U39	--	

5. After the signatures are taken, remove A3TP26 and A3TP17 from ground. Store the jumper between the ground pins of A3TP16-19.

   Turn the Signal Generator's POWER switch to STBY and then back to ON.

✓2 Fractional-N and Latches

1. Set the Signal Generator's POWER switch to STBY.
2. Connect A3TP26 to ground. Connect A3TP18 to ground using the jumper provided.
3. Set the Signal Generator's POWER switch to ON.
4. The LF Loop's Microprocessor troubleshooting routine is now entered as a result of completing step 2. The nine's complement data loaded into the Divide-By-N-Counters is 685, and the LF Loop VCO's frequency is set to 66.8 MHz.

   If the LF Loop VCO's frequency is not 66.8 MHz, check the nine's complement data loaded into the nine's Complement Latches. The nine's compliment data should be as follows:

   a. 100 kHz DIGIT: U29 pin 2 (H), pin 7 (L), pin 10 (H), pin 15 (L)

   b. 1 MHz DIGIT: U23 pin 12 (L), pin 15 (L), pin 16 (L), pin 19 (H)

   c. 10 MHz DIGIT: U23 pin 2 (L), pin 5 (H), pin 6 (H), pin 9 (L)
5. Use the oscilloscope to check that the API outputs of U17 at pins 2 to 6 pulse low every 10 μs.
6. Use the oscilloscope to check that the Bias output of U17 at pin 10 pulses high for 13 Chip Clocks every 10 μs.
7. Disconnect A3TP20 from A3TP26. Disconnect A3TP18 from ground.

✓3 Counters and Cycle Start Synchronization

1. Remove jumper A3W6 (refer to Service Sheet 14). The VCO TUNE voltage goes to approximately 0.0V.
2. Connect the frequency counter to A3TP29 (60 to 110 MHz) (refer to Service Sheet 10) and measure the VCO frequency. The VCO frequency should be 96 MHz ±7 MHz.
3. Subtract the VCO frequency from 1050 MHz and select the difference frequency as the RF output frequency of the Signal Generator to 5 significant digits, for example, 950.73 MHz.

   a. RF Output Frequency = (800 − VCO) +Notch Filter Frequency

   b. The Notch Filter Frequency is 250 MHz

   c. RF output Frequency = 800 − VCO + 250 = 1050 − VCO

   d. The nine's complement data in the nine's Complement Latches is the data required to lock the Low Frequency Loop VCO.
4. Set the Oscilloscope as follows:

   Chan 1

   Ch 1 Mode ..... Normal
   Ch 1 Display ..... On
   VOLTS/DIV 1.0V
   OFFSET 0.0V

   Chan 2

   Ch 2 Mode ..... Normal
   Ch 2 Display ..... On
   VOLTS/DIV 2.0V
   OFFSET 1.0V

Timebase

SEC/DIV ..... 1.0 μs
DELAY 0.0s
Delay Ref at ..... Left
Sweep ..... Trg'd

Trigger

Trigger Mode ..... Edge
Trig Src ..... Chan 1
TRIG LEVEL 1.5V
Slope ..... Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 200 ms
Split Screen ..... ON
Graticle ..... ON

5. Connect Chan 1 to A3TP15 (CYCLE START), and Chan 2 to pin 12 of each Counter A3U24, U30, and U36.

   Figure 2 shows the oscilloscope display for the 1 MHz, 10 MHz, and 100 kHz Counters for a VCO frequency of 99.8 MHz. With a VCO frequency of 96 MHz ±7 MHz the oscilloscope display of the Counter output is the same except for timing.

⟨4⟩ Edge Detector, Timing Latches, and Synchronization

1. Remove jumper A3W6 (refer to Service Sheet 14). The VCO TUNE voltage goes to approximately 0.0V.
2. Timing pulse generation and clocking is checked.
3. Set the Oscilloscope as follows:

Chan 1

Ch 1 Mode ..... Normal
Ch 1 Display ..... On
VOLTS/DIV 2.0V
OFFSET 0.0V

Chan 2

Ch 2 Mode ..... Normal
Ch 2 Display ..... On
VOLTS/DIV 2.0V
OFFSET 1.0V

Timebase

SEC/DIV ..... 200 ns
DELAY 0.0s
Delay Ref at ..... Left
Sweep ..... Trg'd

Trigger

Trigger Mode ..... Edge
Trig Src ..... Chan 2
TRIG LEVEL ..... 200 mV
Slope ..... Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 200 ms
Split Screen ..... ON
Graticle ..... ON

4. Connect Chan 1 to A3TP31 (CHIP CLOCK) (refer to Service Sheet 10), and Chan 2 to A3TP27 (START SHIFT). The Start Shift pulse should be present and have a pulse width of one Chip Clock.

5. With the Chan 1 probe, check that the pulse is clocked through the Timing Latches, U42, U44B and Synchronization flip/flop U47. The VCO divide-by-N.F. output of Q48 is a narrow pulse.

⟨✓5⟩ Cycle Add/Remove Latches and Add/Remove Cycle Gates

1. Remove jumper A3W6 (refer to Service Sheet 14). The VCO TUNE voltage goes to approximately 0.0V.

2. The 100 kHz Counter remove cycle pulse is checked.

3. Set the Oscilloscope as follows:

Chan 1

Ch 1 Mode ..... Normal
Ch 1 Display ..... On
VOLTS/DIV 2.0V
OFFSET 0.0V

Chan 2

Ch 2 Mode ..... Normal
Ch 2 Display ..... On
VOLTS/DIV 2.0V
OFFSET 1.0V

Timebase

SEC/DIV ..... 1.0 μs
DELAY 0.0s
Delay Ref at ..... Center
Sweep ..... Trg'd

Trigger

Trigger Mode ..... Edge
Trig Src ..... Chan 2
TRIG LEVEL 1.5V
Slope ..... Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 200 ms
Split Screen ..... ON
Graticle ..... ON

4. Connect Chan 1 to A3TP27 (START SHIFT), and check that the 100 kHz Counter remove cycle pulse is gated through U41A, U41B and U51A.

5. Replace jumper W6.
6. Set the function generator as follows:

   Frequency ..... 20 Hz
   Level 1.41V

7. Connect the function generator to the Signal Generator's MOD INPUT/ OUTPUT connector.
8. Set the Signal Generator as follows:

   Frequency ..... Any
   Amplitude ..... Any
   Modulation ..... FM, 5 kHz
   Source ..... External

9. Connect Chan 2 to U38A, U38B, U43C, U43B, U51A, and A3TP15, and check that the Add and Remove Cycle pulses are gated through them.

A3 Component Coordinates (1 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	E,1	C213	C,1	C513	A,4	CR1	D,2	FL1	E,2	Q10	D,4
C2	D,2	C300	D,2	C514	A,3	CR2	D,2	FL2	E,2	Q11	D,4
C3	E,2	C301	C,3	C515	A,4	CR3	D,2	FL3	D,2	Q12	A,4
C4	D,2	C302	C,3	C516	A,3	CR4	D,2	FL4	D,2	Q13	B,4
C5	D,1	C303	D,3	C517	A,3	CR5	E,1			Q14	B,4
C6	D,2	C304	D,3	C518	B,3	CR6	D,1	J1	E,4	Q15	B,4
C7	D,1	C305	D,3	C519	A,3	CR7	D,2	J2	A,4	Q16	C,4
C8	D,1	C306	C,2	C520	A,3	CR8	D,2	J3	A,4	Q17	C,4
C9	D,2	C307	C,3	C521	A,3	CR9	E,1	J4	C,2	Q18	C,4
C10	D,2	C308	C,3	C600	B,3	CR10	D,1	J5	C,1	Q19	D,4
C11	E,1	C309	C,3	C601	B,3	CR11	D,1	J6	D,1	Q20	D,4
C12	D,1	C310	C,2	C602	B,3	CR12	D,1	J7	E,1	Q21	D,4
C13	D,2	C311	C,1	C603	B,3	CR15	E,1	J8	E,2	Q22	B,4
C14	D,2	C312	C,1	C604	B,3	CR16	D,1			Q23	C,4
C15	D,1	C313	C,2	C605	B,3	CR17	E,2	L1	E,2	Q24	C,4
C16	D,2	C400	B,3	C606	B,3	CR18	D,2	L2	D,2	Q25	C,4
C17	D,1	C401	D,4	C607	B,3	CR200	C,1	L3	E,2	Q26	B,4
C18	E,1	C402	C,4	C608	B,3	CR201	C,1	L5	E,2	Q27	B,4
C19	E,2	C403	C,3	C609	B,3	CR400	B,4	L6	E,2	Q28	C,4
C20	E,2	C404	B,4	C610	C,3	CR401	C,4	L8	D,2	Q29	A,4
C21	E,1	C405	C,3	C611	C,4	CR402	C,4	L200	E,4	Q30	A,4
C22	E,2	C406	C,4	C612	C,3	CR403	C,4	L201	E,4	Q31	A,4
C23	E,1	C407	C,4	C613	B,3	CR404	C,4	L202	E,4	Q32	A,4
C24	E,2	C408	B,3	C614	B,3	CR405	B,4	L203	E,4	Q33	B,4
C25	E,1	C409	B,4	C615	B,2	CR406	B,4	L204	C,1	Q34	A,3
C26	E,2	C410	C,4	C616	B,3	CR500	B,4	L300	C,1	Q35	B,3
C27	D,1	C411	B,4	C617	B,2	CR501	B,4	L400	B,4	Q36	B,3
C28	E,2	C412	C,4	C618	B,3	CR502	A,4	L401	D,4	Q37	A,3
C29	D,1	C413	B,4	C619	B,3	CR503	A,4	L402	C,3	Q38	A,3
C30	E,1	C414	B,4	C620	B,2	CR504	B,4	L403	C,3	Q39	A,3
C100	A,3	C415	B,4	C621	B,2	CR505	B,4	L404	C,4	Q40	A,3
C101	A,2	C416	B,4	C700	E,3	CR506	B,4	L500	B,4	Q41	A,3
C200	E,4	C500	A,4	C701	E,3	CR600	B,3	L501	A,4	Q42	A,3
C201	E,4	C501	A,4	C702	E,3	CR602	B,3	L502	A,4	Q43	A,3
C202	E,4	C502	B,4	C703	E,2	CR700	D,4	L503	A,4	Q44	A,3
C203	E,4	C503	A,4	C704	E,3	CR701	D,4			Q46	A,2
C204	B,1	C504	A,3	C705	E,4	CR702	D,4	Q1	A,4	Q47	C,1
C205	C,2	C505	B,4	C706	E,4	CR703	D,4	Q2	A,4	Q48	C,2
C206	C,1	C506	B,4	C707	D,4	CR704	D,4	Q3	D,4	Q49	D,1
C207	C,1	C507	A,4	C708	D,4	CR705	D,4	Q4	A,4	Q50	E,1
C208	C,1	C508	B,3	C709	D,4	CR706	D,4	Q5	B,4	Q51	C,1
C209	C,1	C509	B,3	C710	D,4	CR707	D,4	Q6	B,4	Q52	D,1
C210	C,1	C510	A,4	C711	D,4			Q7	B,4	Q53	D,1
C211	C,1	C511	B,3	C712	D,4			Q8	C,4	Q54	E,1
C212	C,1	C512	A,3	C713	E,4	DS500	A,3	Q9	C,4	Q55	E,1

A3 Component Coordinates (2 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
Q56	C,1	R207	C,1	R431	B,4	R523	A,4	R568	A,3	R719	D,4
		R208	C,1	R432	C,3	R524	A,4	R569	B,3	R720	E,4
R1	D,2	R209	B,1	R433	D,4	R525	A,3	R570	A,3	R721	D,4
R2	D,2	R210	C,1	R434	C,4	R526	A,4	R600	B,3	R722	D,4
R3	D,2	R211	C,1	R435	C,3	R527	A,3	R601	B,3	R723	D,4
R4	E,2	R300	C,3	R436	B,4	R528	A,3	R602	B,3	R724	D,4
R5	D,2	R301	C,3	R437	B,4	R529	A,4	R603	B,3	R725	D,4
R6	D,1	R302	C,3	R438	D,4	R530	A,4	R604	B,3	R726	D,4
R7	D,2	R303	C,3	R439	C,3	R531	A,3	R605	B,3	R727	D,4
R8	D,1	R304	C,3	R440	C,4	R532	B,3	R606	B,3	R728	D,4
R9	E,1	R305	C,2	R441	B,4	R533	A,4	R607	B,3	R729	D,4
R10	D,2	R306	D,2	R442	C,4	R534	A,3	R608	A,3	R731	D,4
R11	D,2	R307	C,1	R443	B,4	R535	A,3	R609	B,3	R732	C,4
R12	D,2	R308	C,1	R444	B,4	R536	A,4	R610	B,3	R733	D,4
R13	D,1	R400	C,4	R445	B,4	R537	A,4	R611	B,3	R734	D,4
R14	D,2	R401	C,4	R446	B,4	R538	A,3	R612	C,3	R735	C,4
R15	E,1	R402	B,4	R447	B,4	R539	A,3	R613	B,3	R736	D,4
R16	D,1	R403	B,4	R448	B,4	R540	A,4	R614	B,3	R737	C,4
R17	D,1	R404	B,4	R449	B,4	R541	A,3	R615	B,3	R738	D,4
R18	E,1	R405	B,4	R450	B,4	R542	A,3	R616	C,3	R740	D,4
R19	D,1	R406	C,4	R451	C,4	R543	A,4	R617	B,3	R741	E,4
R20	D,1	R407	C,4	R452	C,4	R544	A,3	R618	B,3		
R21	D,1	R408	C,4	R500	A,4	R545	A,4	R619	B,3	TP1	B,4
R22	D,1	R409	B,4	R501	A,4	R546	A,3	R620	B,3	TP2	A,4
R23	E,1	R410	C,4	R502	A,4	R547	A,4	R621	B,2	TP3	D,4
R24	E,1	R411	C,4	R503	A,4	R548	A,3	R622	B,3	TP4	D,4
R25	E,2	R412	B,4	R504	A,4	R549	A,3	R700	E,4	TP5	D,4
R26	E,2	R413	C,4	R505	A,4	R550	A,3	R701	E,4	TP6	D,4
R27	E,2	R414	B,4	R506	A,4	R551	A,3	R702	E,4	TP7	C,4
R28	D,2	R415	C,4	R507	A,4	R552	A,4	R703	E,4	TP8	D,4
R29	D,1	R416	C,4	R508	A,4	R553	A,3	R704	D,4	TP9	D,4
R30	D,1	R417	C,4	R509	A,4	R554	A,3	R705	E,4	TP10	B,3
R31	D,1	R418	C,4	R510	A,4	R555	A,3	R706	D,4	TP11	A,3
R32	D,1	R419	B,4	R511	A,4	R556	A,3	R707	B,4	TP12	A,3
R33	D,2	R420	B,4	R512	A,4	R557	A,3	R708	E,4	TP13	B,3
R100	A,2	R421	C,4	R513	A,4	R558	A,3	R709	D,4	TP14	B,3
R101	A,2	R422	C,4	R514	A,4	R559	A,3	R710	D,4	TP15	C,3
R104	A,2	R423	C,4	R515	A,4	R560	A,3	R711	D,4	TP16	C,3
R200	B,2	R424	C,4	R516	A,4	R561	A,3	R712	B,4	TP17	C,3
R201	C,1	R425	C,4	R517	A,4	R562	A,3	R713	D,4	TP18	D,3
R202	C,2	R426	C,4	R518	B,4	R563	A,3	R714	D,4	TP19	D,3
R203	C,2	R427	C,4	R519	A,4	R564	A,3	R715	D,4	TP20	C,3
R204	C,1	R428	C,4	R520	A,4	R565	B,3	R716	C,4	TP21	C,3
R205	C,1	R429	B,4	R521	A,3	R566	A,3	R717	D,4	TP22	A,3
R206	C,1	R430	C,3	R522	B,4	R567	A,3	R718	E,4	TP23	A,3

A3 Component Coordinates (3 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
TP24	C,3	U35	C,2						
TP25	C,3	U36	D,2						
TP26	C,2	U37	E,2						
TP27	C,2	U38	C,2						
TP28	C,2	U39	C,2						
TP29	C,2	U40	D,2						
TP30	C,1	U41	C,2						
TP31	C,1	U42	C,2						
TP32	D,1	U43	C,2						
TP33	E,1	U44	C,2						
		U45	D,2						
U1	A,4	U46	C,1						
U2	B,4	U47	C,1						
U3	C,4	U48	D,1						
U4	D,4	U49	C,1						
U5	D,4	U50	C,1						
U6	C,4	U51	C,1						
U7	B,4	U52	D,1						
U8	C,4	U53	E,1						
U9	A,4	U54	C,1						
U10	D,4	U55	C,1						
U11	D,4								
U12	E,3	VR300	C,3						
U13	B,3	VR400	B,4						
U14	B,3	VR401	C,4						
U15	E,3	VR500	A,3						
U16	E,3	VR601	B,3						
U17	C,3								
U18	D,3	W1	B,3						
U19	E,3	W2	C,3						
U20	E,3	W3	A,3						
U21	A,3	W4	B,3						
U22	B,3	W5	A,3						
U23	D,3	W6	A,2						
U24	D,3	W7	D,1						
U25	E,3	W8	C,1						
U26	E,3	W9	C,4						
U27	B,3	W10	C,4						
U28	C,3	W11	B,4						
U29	D,3								
U30	D,3	Y1	E,2						
U31	E,3	Y300	C,2						
U32	E,3								
U33	B,3								
U34	B,3								

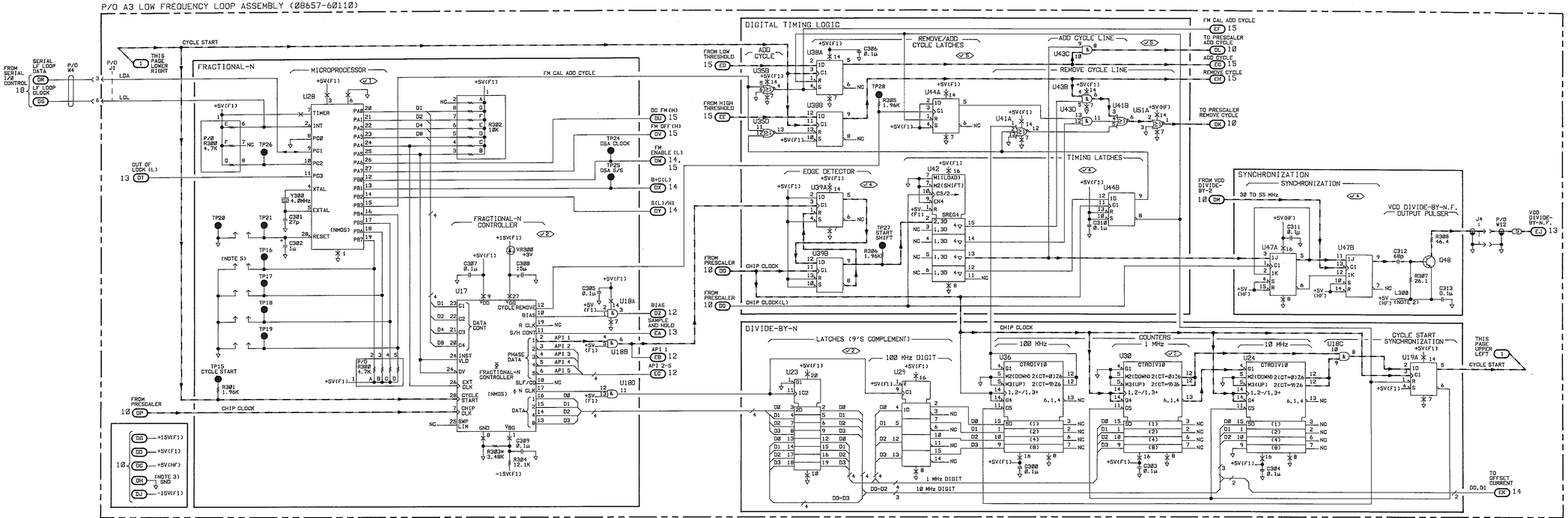


Figure 3
Service Sheet 11 17

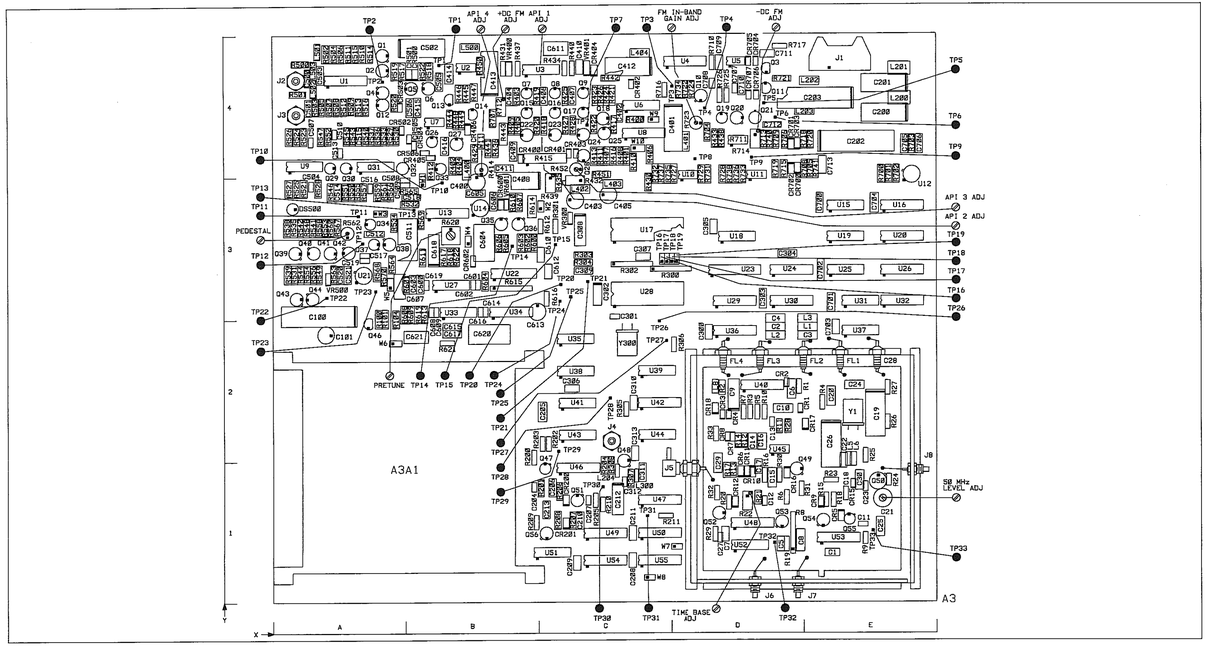


Figure Ø. Service Sheet 12 Information

Component Locator

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Chassis ground is achieved by mechanical contact through nuts holding PC board to cover and W4.
3. Isolation (guard) trace.
4. Reference designations on this service sheet C, CR, L, R and VR have numbers ranging from 400 to 499 only.

LOGIC LEVELS

	TTL
HIGH	2V
LOW	Ø.8V
	IS MORE NEG. THAN
	IS MORE POS. THAN
OPEN	HIGH
GROUND	LOW

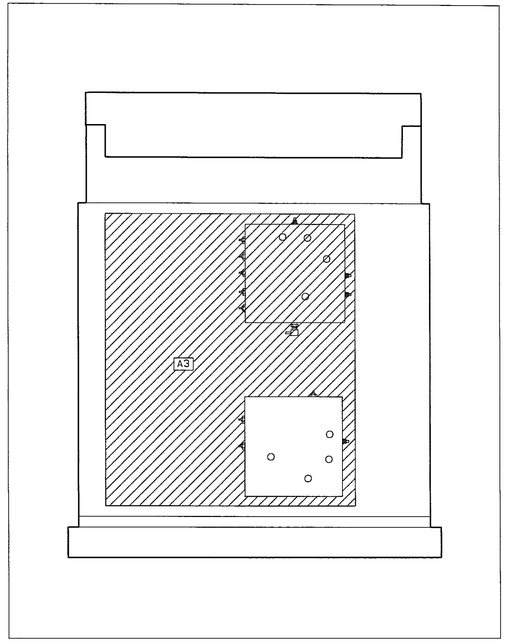
A3U2,7
TOP VIEW

A3Ø7-9,15-17
TOP VIEW

A3Ø26
TOP VIEW

P/O A3 — LOW FREQUENCY LOOP FRACTIONAL-N, DIVIDE-BY-N AND DIGITAL TIMING LOGIC — SS11

SEE REVERSE SIDE



Ø Service Sheet 12

Service Sheet 12

LOW FREQUENCY LOOP ANALOG PHASE INTERPOLATION (API), CURRENT SOURCES, CURRENT SUMMING, AND BIAS

PRINCIPLES OF OPERATION

General

The Bias pulse from the Fractional-N Controller U17 is the D input at pin 12 of D flip-flop U6B. CHIP CLOCK at pin 11 clocks the high D input of U6B to the output at pin 9, Delayed Bias. The Bias and Delayed Bias pulses remain high for 13 CHIP CLOCK pulses. The Fractional-N Controller sets its BIAS output high one Chip Clock after its Sample and Hold output was set inactive (low). The Integrator's correction voltage has been stored on the Sample and Hold capacitor. See Figure 1, the Low Frequency Loop Timing Diagram. The Integrator is reset before the next phase correction input is received from the Phase Detector. The Delayed Bias Pulse resets the Integrator by directing Bias Current to the Integrator. Figure 2 shows the API and Bias Currents.

Bias Control

Bias Pulse Off

The Bias pulse from the Fractional-N Controller is off, low. The low Delayed Bias output at pin 9 of U6B sets the base of emitter follower Q33 to approximately −1.6V. The emitter voltage is approximately −1.0V. Bias current-steering diode CR405 is turned on, and CR506 is turned off (refer to Service Sheet 13). The Bias Current is directed to the Bias Control transistor Q33.

Bias Pulse On

The Bias pulse from the Fractional-N Controller is on, high. The high Delayed Bias output at pin 9 of U6B sets the base of Q33 to approximately +3.0V. The emitter voltage increases to approximately +3.7V. Q33's increased positive emitter voltage turns Bias Current steering diodes CR405 off and CR506 on. The Bias Current is directed to the Integrator.

Current Routing Control

The base of Q28 is biased at approximately +5 Vdc from the +5 Vdc (F2) supply voltage through resistor R408. The collector of Q25 is connected to −15 Vdc (F1). The base voltage of Q18 is biased at approximately +1.2 Vdc divided from the +15 Vdc by resistors R424 and R426 to ground.

Bias Pulse Off

The Bias pulse from the Fractional-N Controller is off, low. The low Delayed Bias pulse output at pin 9 of U6B turns off Q28. The emitter voltage of Q28 is approximately +5V, divided from the +15 Vdc supply voltage by resistors R411 and R413. The dc bias for Q25 is divided from the −15 Vdc (F1) supply voltage by resistors R416 and R417 to ground. The base voltage of Q25 is approximately −1.9V. Q25 is turned on since its emitter is connected to +15 Vdc by R421. The voltage on the emitter is approximately −1.2V. The emitter voltage of Q25 is also the emitter voltage of Q18, and the negative emitter voltage turns Q18 off. Its collector voltage is −7.5V, divided from the −15 Vdc (F1) supply voltage by resistors R422 and R423 to ground. The −7.5V is connected to the gates of FET switches, Q15, Q16, and Q17 turning them off. With the FET switches turned off the current for the current sources of U3 is directed to Q3 and Q21 (refer to Service Sheet 15), and Q5 (refer to Service Sheet 13).

Bias Pulse On

The Bias pulse from the Fractional-N Controller is on, high. The high Delayed Bias pulse output at pin 9 of U6B turns on Q28. When the Delayed Bias pulse goes high, the emitter voltage of Q28 increases to approximately +5.7V. Transistor Q28 is turned on and the collector voltage increases to approximately +5.7V. The collector voltage of Q28 is the base voltage for Q25, and is used to turn Q25 off. Q25 is turned off during the Bias pulse. With Q25 turned off its emitter voltage goes positive. The emitter voltage of Q25 is also the emitter voltage of Q18, and is used to turn Q18 on. When Q18 is turned on, its collector increases from approximately −7.5V to approximately +2V. The three FET switches, Q15, Q16, and Q17 are turned on. The current for the current sources from U3 is directed from the three API transistors, Q22, Q23, and Q24. The API transistors Q22 (API 1), Q23 (API 2), and Q24 (API 3) are turned on. When the the API transistors are turned on API current steering diodes CR400, CR401 and CR403 are turned off.

During the Bias pulse from the Fractional-N Controller the Analog Phase Interpolation (API) pulses are also active. The API pulses are controlled by the Fractional-N Controller. The API pulses control the amount of phase correction current subtracted from the Bias Current during the Bias pulse. The Bias Current resets the Integrator after the Integrator voltage has been stored on the Sample and Hold capacitor (refer to Service Sheet 13). The Integrator's voltage is dependent on the phase difference between the VCO and the reference signals. The Fractional-N Controller controls the pulse duration for each of the 5 API signals. When the Low Frequency Loop VCO is tuned to a whole number, multiple of 100 kHz, the API pulses are active for a fixed length of time during each Bias pulse. The phase of the Low Frequency Loop VCO is not changing in relation to the 100 kHz reference. The length of the API pulses change when the Phase Increment mode is selected, and the phase of the RF output is incremented.

When the Low Frequency VCO is operating at a fractional frequency, the length of time each API pulse is active varies from one cycle to the next cycle. The Low Frequency Loop VCO is not tuned to a whole number multiple of 100 kHz. The API pulses when viewed with an oscilloscope are not nice and steady, but are changing each cycle. The phase between the Low Frequency Loop VCO divided-by-N.F. and the 100 kHz reference is continually changing. When the phase difference between the 100 kHz reference, and the VCO divided-by-N.F. signals changes by 360 degrees, a cycle is removed by the Prescaler. The Fractional-N Controller measures the phase difference between the VCO divided-by-N.F. and the reference signals, and it controls the Prescaler. Each time a cycle is removed by the Prescaler, the phase difference between the VCO and reference returns to the same nominal offset.

The API pulses compensate for the Fractional-N phase changes between the Low Frequency Loop VCO and the reference. When the Bias pulse is high, the Integrator is reset. API current is subtracted from the Bias Current. The API pulses are active low and the Integrator's output voltage is offset. The Integrator's output voltage is offset to compensate for the Phase Detector's output that results from the fractional frequency phase difference between the VCO Divided-By-N.F., and the 100 kHz reference.

When transistor Q22 is turned off by the API 1 pulse, the API 1 current steering diode CR400 is turned on. API 1 current to Current Buffer Q7 and part of Current Source U3 is summed with the Bias Current at Current Summing Amplifier U7. The two currents are summed together for the length of time the API 1 pulse is active. Q22 is turned on, turning off CR400 and steering the API 1 current through Q22.

The API pulses are active low and are controlled by the Fractional-N Controller. The D input to U6A, part of the API Digital Control circuits, is high when API 1 is not active. The high D input is clocked to the output at pin 5 by the Chip Clock. The +15 Vdc is divided by R405 and R409 to the +5V at U6A pin 5. The base of Q22 is approximately +6V. Its emitter voltage is approximately +5.4V. Q22 is turned on, and CR400 is turned off since the anode of CR400 is connected to the virtual +5 Vdc summing node through resistor network of R435, R439, and R415A and B. A low API 1 pulsed input at pin 2 of U6A is clocked to the output at pin 5. The +15 Vdc is divided to approximately 0V at pin 5 by R405 and R409. The base of Q22 is approximately +3V, and the emitter voltage wants to decrease to turn on Q22. But when its voltage gets to approximately +4.4V

CR400 is turned on. Q22 is turned off until the API 1 pulse returns high. Transistors Q23 and Q24 operate the same for API 2 and 3 currents. The amount of the API currents is precisely controlled by the current sources, by the adjustments, and by resistor R415.

The four Current Sources of U3, and the three Current Buffers Q7, Q8 and Q9 are always turned on. The base of all transistors in U3 are biased at −8.2 Vdc, and are controlled by the 6.2V Zener diode VR401, and the diode voltage drop of CR404. Their emitter voltages are then −8.8 Vdc. Each Current Source produces a precise amount of current determined by the voltage drop of each emitter resistor (1.15k for 5.4 mA, 2.3k for 2.7 mA, and 12.1k for 0.5 mA). When API 1 is active, the 5.4 mA of the Current Source is divided by resistors R435, R439, and R415A and B. The current summed with the Bias Current is approximately 54 μA. The actual value of the current is adjusted by R439 for minimum API 1 spurs. When API 2 is active, the 2.7 mA of the Current Source is divided by resistors R432, and R415C and F. The current summed with the Bias Current is approximately 5.4 μA. The actual value of the current is adjusted by R432 for minimum API 2 spurs. When API 3 is active the 2.7 mA of the Current Source is divided by resistors R452, R51, and R415D and R415E. The current summed with the Bias Current is approximately 0.54 μA. The actual value of the current is adjusted by R452 for minimum API 3 spurs. When API 4 is active, the low output of U8 at pin 7 causes a current to flow from the +5 Vdc to the low at pin 7. The current is divided by resistors R429, R414, and R406. The current summed with the Bias Current is approximately 50 nA. The actual value of the API 4 current is adjusted by R414 for minimum API 4 spurs. When API 5 is active, the low output of U8 at pin 10 causes a current to flow from the +5 Vdc to the low at pin 10. The current is divided by resistors R436, and R441. The current summed with the Bias Current is approximately 5.0 nA. The API 5 current is not adjustable.

The API currents are summed with the Bias Current at the Current Summing Amplifier U7. The currents are summed into the virtual +5 Vdc node at pin 2 of U7, and all of the current flows through FET Q26 to the Integrator. This all occurs during the Bias pulse. The length of time that the Bias pulse is active varies depending upon the Low Frequency Loop's VCO's frequency, 60 to 110 MHz. After 12 Chip Clocks the API pulses are all turned off, and at the completion of the 13th Chip Clock the Bias pulse is turned off. The Integrator is reset and ready for the next input from the Phase Detector. When the Bias pulse is turned off, the Delayed Bias pulse at pin 9 of U6B also goes low. Q33 is turned on, CR405 is turned on, and CR506 is turned off. The Bias Current flows through Q33. The FET switches Q15, Q16, and Q17 are turned off by the −7.5V at the collector of Q18.

A Bias Current of 0.5 mA is continually provided by Q27, and is controlled by the 0.5 mA from the Current Source U3 and Q14. Transistor Q14 senses variations in the +5 Vdc summing node and compensates for the variations. The +5 Vdc of the summing node must be kept constant to prevent spurs on the RF output of the Signal Generator.

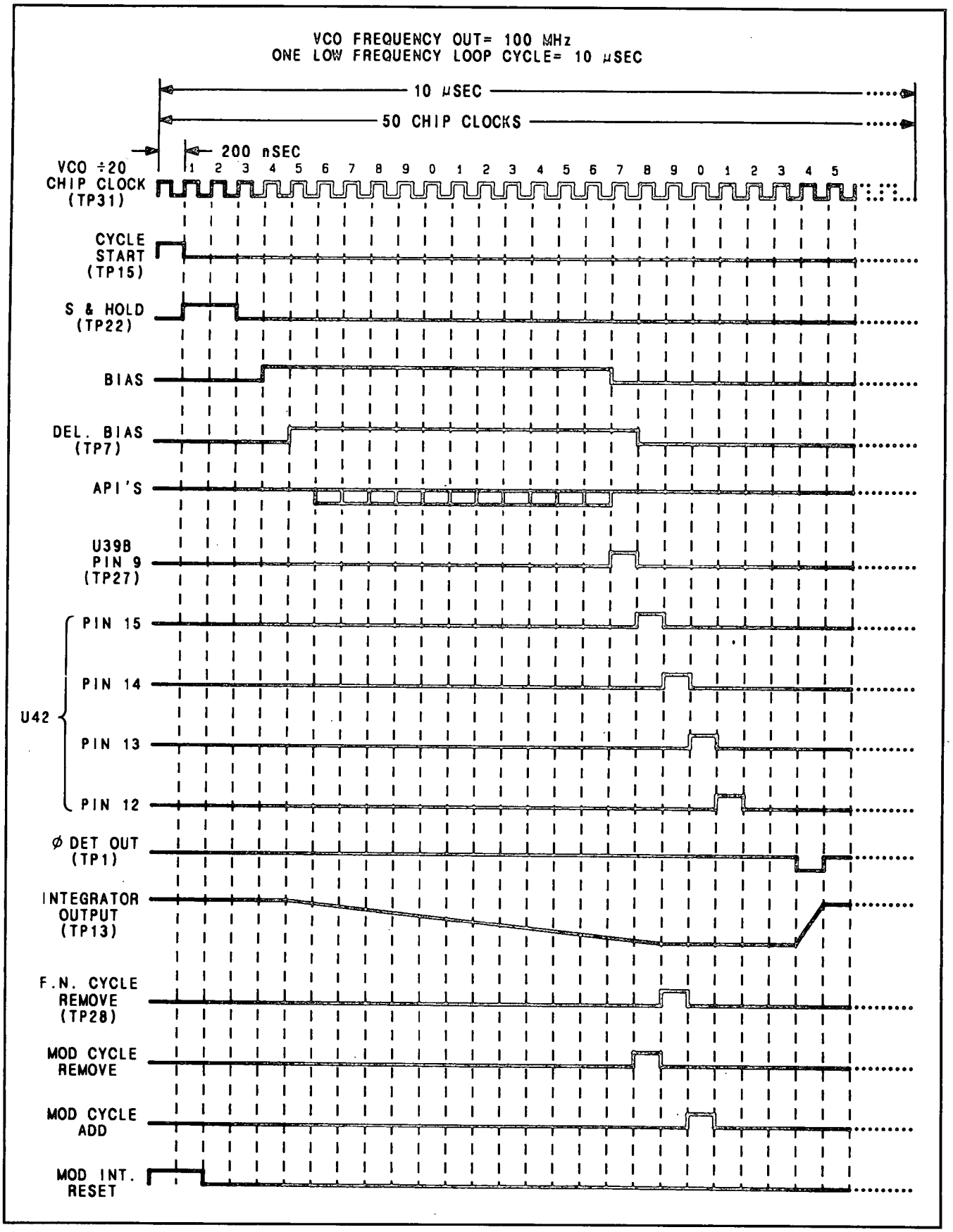


Figure 1. Low Frequency Loop Timing Diagram.

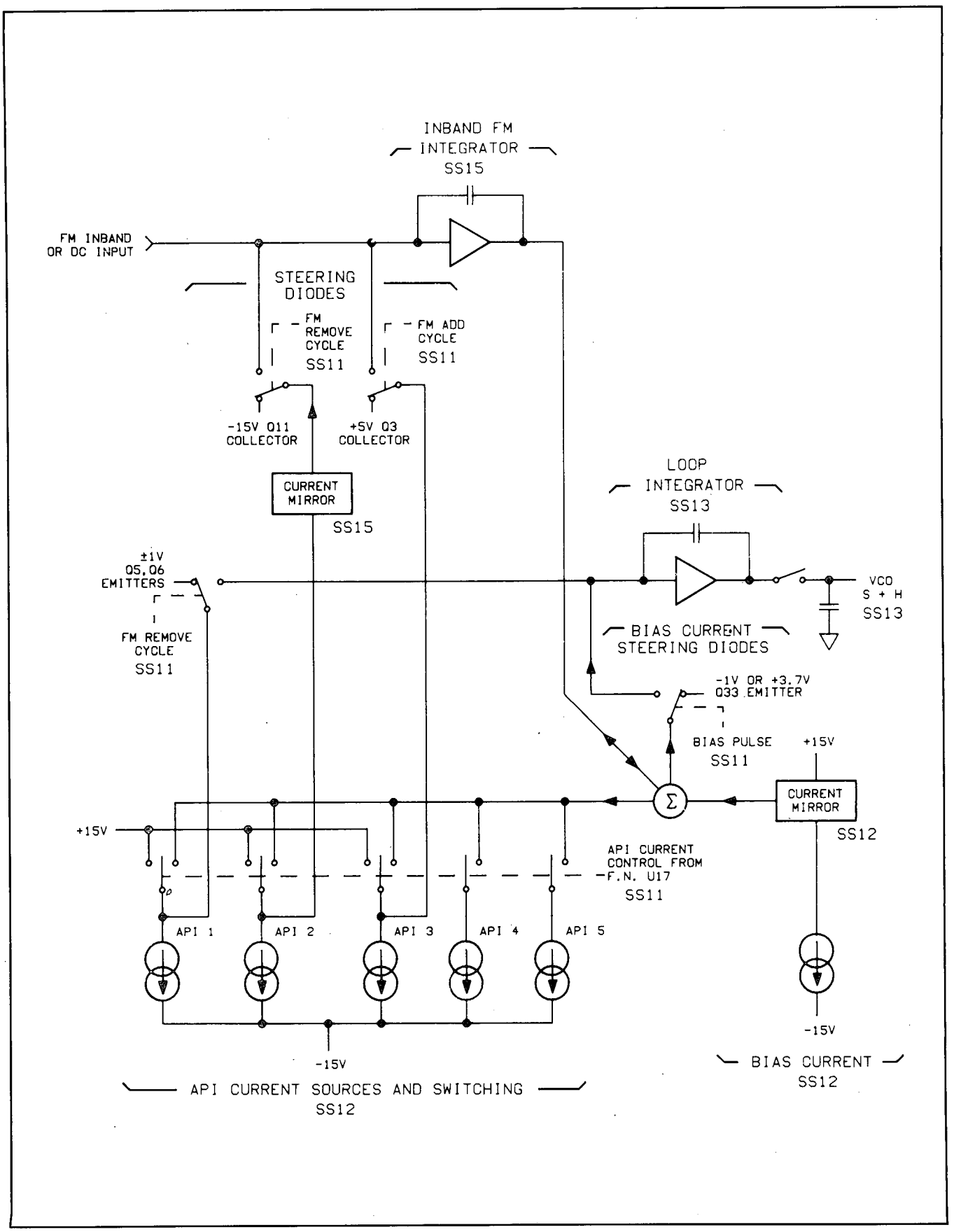


Figure 2. *Low Frequency Loop API and Bias Currents.*

TROUBLESHOOTING

Procedures for checking part of the A3 Low Frequency Loop Assembly circuits are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, for example, ⟨✓1⟩ Transistor bias voltages are shown without tolerances. If the Low Frequency Loop does not lock, circuit problems could be in the Bias Control, in the Current Routing Control, in the Current Sources, in the API 1 current or in the Bias Current. If spurious signals (spurs) are high, the problem could be in the Current Routing of API Currents or in the API Current Sources.

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Digital Multimeter	HP 3466A
Oscilloscope	HP 54100A
Oscilloscope Active Probe Chan 1	HP 54001A
Oscilloscope 1 Megohm Probe Pod Chan 2	HP 54003A
Oscilloscope Probe	HP 54003-61617

⟨✓1⟩ Bias Control and P/O Current Routing Control

1. Check the Bias pulse at pin 12 of U6B, and the Delayed Bias pulse at pin 9. The pulses are at TTL levels and 13 Chip Clocks long. If the Low Frequency Loop is not locked, and the pulses are still 13 Chip Clocks long, but the pulse width changes as the frequency of the Chip Clock changes, refer to Figure 1 and continue with check 1.
2. The pulse at TP10 (BIAS SW) is a TTL high during the Bias pulse, and should be the same pulse width as the Bias pulse. Bias Current steering diode CR405 is turned off.
3. The pulse at TP7 (DELAYED BIAS) is approximately 0V during the Bias pulse, and approximately −7.5V when the Bias pulse is off.
4. Transistor Q28 is on, Q25 is off, and Q18 is on during the Bias pulse.

⟨✓2⟩ API Digital Control and P/O Current Routing Control

1. Enter a frequency of 100 MHz from the keyboard. The Low Frequency Loop does not have to be locked.
2. Check the low API pulses at the outputs of U6A and U8. The pulses are at TTL levels and 12 Chip Clocks long. If the loop is not locked, the pulses are still 12 Chip Clocks long but vary as the frequency of the Chip Clock changes.
3. Check that transistors Q22, Q23, and Q24 are turned off and API current steering diodes CR400, CR401, and CR403 are turned on when their API pulses are active low.

⟨√3⟩Current Sources and Current Dividers

1. Enter a frequency of 100 MHz from the keyboard.
2. Measure the dc voltages for the Current Sources and the Current Buffers.
3. Measure the voltage drop across the Current Source's emitter resistors and calculate the current through the resistors.
4. Measure for a voltage drop across resistors R415A, B, C, D, E, F, when the API pulses are active low.

⟨√4⟩Current Summing and Bias

1. Measure the dc voltages of Q14, Q27, and Q26.
2. Measure the reference voltage +5V (Ref).

A3 Component Coordinates (1 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	E,1	C213	C,1	C513	A,4	CR1	D,2	FL1	E,2	Q10	D,4
C2	D,2	C300	D,2	C514	A,3	CR2	D,2	FL2	E,2	Q11	D,4
C3	E,2	C301	C,3	C515	A,4	CR3	D,2	FL3	D,2	Q12	A,4
C4	D,2	C302	C,3	C516	A,3	CR4	D,2	FL4	D,2	Q13	B,4
C5	D,1	C303	D,3	C517	A,3	CR5	E,1			Q14	B,4
C6	D,2	C304	D,3	C518	B,3	CR6	D,1	J1	E,4	Q15	B,4
C7	D,1	C305	D,3	C519	A,3	CR7	D,2	J2	A,4	Q16	C,4
C8	D,1	C306	C,2	C520	A,3	CR8	D,2	J3	A,4	Q17	C,4
C9	D,2	C307	C,3	C521	A,3	CR9	E,1	J4	C,2	Q18	C,4
C10	D,2	C308	C,3	C600	B,3	CR10	D,1	J5	C,1	Q19	D,4
C11	E,1	C309	C,3	C601	B,3	CR11	D,1	J6	D,1	Q20	D,4
C12	D,1	C310	C,2	C602	B,3	CR12	D,1	J7	E,1	Q21	D,4
C13	D,2	C311	C,1	C603	B,3	CR15	E,1	J8	E,2	Q22	B,4
C14	D,2	C312	C,1	C604	B,3	CR16	D,1			Q23	C,4
C15	D,1	C313	C,2	C605	B,3	CR17	E,2	L1	E,2	Q24	C,4
C16	D,2	C400	B,3	C606	B,3	CR18	D,2	L2	D,2	Q25	C,4
C17	D,1	C401	D,4	C607	B,3	CR200	C,1	L3	E,2	Q26	B,4
C18	E,1	C402	C,4	C608	B,3	CR201	C,1	L5	E,2	Q27	B,4
C19	E,2	C403	C,3	C609	B,3	CR400	B,4	L6	E,2	Q28	C,4
C20	E,2	C404	B,4	C610	C,3	CR401	C,4	L8	D,2	Q29	A,4
C21	E,1	C405	C,3	C611	C,4	CR402	C,4	L200	E,4	Q30	A,4
C22	E,2	C406	C,4	C612	C,3	CR403	C,4	L201	E,4	Q31	A,4
C23	E,1	C407	C,4	C613	B,3	CR404	C,4	L202	E,4	Q32	A,4
C24	E,2	C408	B,3	C614	B,3	CR405	B,4	L203	E,4	Q33	B,4
C25	E,1	C409	B,4	C615	B,2	CR406	B,4	L204	C,1	Q34	A,3
C26	E,2	C410	C,4	C616	B,3	CR500	B,4	L300	C,1	Q35	B,3
C27	D,1	C411	B,4	C617	B,2	CR501	B,4	L400	B,4	Q36	B,3
C28	E,2	C412	C,4	C618	B,3	CR502	A,4	L401	D,4	Q37	A,3
C29	D,1	C413	B,4	C619	B,3	CR503	A,4	L402	C,3	Q38	A,3
C30	E,1	C414	B,4	C620	B,2	CR504	B,4	L403	C,3	Q39	A,3
C100	A,3	C415	B,4	C621	B,2	CR505	B,4	L404	C,4	Q40	A,3
C101	A,2	C416	B,4	C700	E,3	CR506	B,4	L500	B,4	Q41	A,3
C200	E,4	C500	A,4	C701	E,3	CR600	B,3	L501	A,4	Q42	A,3
C201	E,4	C501	A,4	C702	E,3	CR602	B,3	L502	A,4	Q43	A,3
C202	E,4	C502	B,4	C703	E,2	CR700	D,4	L503	A,4	Q44	A,3
C203	E,4	C503	A,4	C704	E,3	CR701	D,4			Q46	A,2
C204	B,1	C504	A,3	C705	E,4	CR702	D,4	Q1	A,4	Q47	C,1
C205	C,2	C505	B,4	C706	E,4	CR703	D,4	Q2	A,4	Q48	C,2
C206	C,1	C506	B,4	C707	D,4	CR704	D,4	Q3	D,4	Q49	D,1
C207	C,1	C507	A,4	C708	D,4	CR705	D,4	Q4	A,4	Q50	E,1
C208	C,1	C508	B,3	C709	D,4	CR706	D,4	Q5	B,4	Q51	C,1
C209	C,1	C509	B,3	C710	D,4	CR707	D,4	Q6	B,4	Q52	D,1
C210	C,1	C510	A,4	C711	D,4			Q7	B,4	Q53	D,1
C211	C,1	C511	B,3	C712	D,4			Q8	C,4	Q54	E,1
C212	C,1	C512	A,3	C713	E,4	DS500	A,3	Q9	C,4	Q55	E,1

A3 Component Coordinates (2 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
Q56	C,1	R207	C,1	R431	B,4	R523	A,4	R568	A,3	R719	D,4
		R208	C,1	R432	C,3	R524	A,4	R569	B,3	R720	E,4
R1	D,2	R209	B,1	R433	D,4	R525	A,3	R570	A,3	R721	D,4
R2	D,2	R210	C,1	R434	C,4	R526	A,4	R600	B,3	R722	D,4
R3	D,2	R211	C,1	R435	C,3	R527	A,3	R601	B,3	R723	D,4
R4	E,2	R300	C,3	R436	B,4	R528	A,3	R602	B,3	R724	D,4
R5	D,2	R301	C,3	R437	B,4	R529	A,4	R603	B,3	R725	D,4
R6	D,1	R302	C,3	R438	D,4	R530	A,4	R604	B,3	R726	D,4
R7	D,2	R303	C,3	R439	C,3	R531	A,3	R605	B,3	R727	D,4
R8	D,1	R304	C,3	R440	C,4	R532	B,3	R606	B,3	R728	D,4
R9	E,1	R305	C,2	R441	B,4	R533	A,4	R607	B,3	R729	D,4
R10	D,2	R306	D,2	R442	C,4	R534	A,3	R608	A,3	R731	D,4
R11	D,2	R307	C,1	R443	B,4	R535	A,3	R609	B,3	R732	C,4
R12	D,2	R308	C,1	R444	B,4	R536	A,4	R610	B,3	R733	D,4
R13	D,1	R400	C,4	R445	B,4	R537	A,4	R611	B,3	R734	D,4
R14	D,2	R401	C,4	R446	B,4	R538	A,3	R612	C,3	R735	C,4
R15	E,1	R402	B,4	R447	B,4	R539	A,3	R613	B,3	R736	D,4
R16	D,1	R403	B,4	R448	B,4	R540	A,4	R614	B,3	R737	C,4
R17	D,1	R404	B,4	R449	B,4	R541	A,3	R615	B,3	R738	D,4
R18	E,1	R405	B,4	R450	B,4	R542	A,3	R616	C,3	R740	D,4
R19	D,1	R406	C,4	R451	C,4	R543	A,4	R617	B,3	R741	E,4
R20	D,1	R407	C,4	R452	C,4	R544	A,3	R618	B,3		
R21	D,1	R408	C,4	R500	A,4	R545	A,4	R619	B,3	TP1	B,4
R22	D,1	R409	B,4	R501	A,4	R546	A,3	R620	B,3	TP2	A,4
R23	E,1	R410	C,4	R502	A,4	R547	A,4	R621	B,2	TP3	D,4
R24	E,1	R411	C,4	R503	A,4	R548	A,3	R622	B,3	TP4	D,4
R25	E,2	R412	B,4	R504	A,4	R549	A,3	R700	E,4	TP5	D,4
R26	E,2	R413	C,4	R505	A,4	R550	A,3	R701	E,4	TP6	D,4
R27	E,2	R414	B,4	R506	A,4	R551	A,3	R702	E,4	TP7	C,4
R28	D,2	R415	C,4	R507	A,4	R552	A,4	R703	E,4	TP8	D,4
R29	D,1	R416	C,4	R508	A,4	R553	A,3	R704	D,4	TP9	D,4
R30	D,1	R417	C,4	R509	A,4	R554	A,3	R705	E,4	TP10	B,3
R31	D,1	R418	C,4	R510	A,4	R555	A,3	R706	D,4	TP11	A,3
R32	D,1	R419	B,4	R511	A,4	R556	A,3	R707	B,4	TP12	A,3
R33	D,2	R420	B,4	R512	A,4	R557	A,3	R708	E,4	TP13	B,3
R100	A,2	R421	C,4	R513	A,4	R558	A,3	R709	D,4	TP14	B,3
R101	A,2	R422	C,4	R514	A,4	R559	A,3	R710	D,4	TP15	C,3
R104	A,2	R423	C,4	R515	A,4	R560	A,3	R711	D,4	TP16	C,3
R200	B,2	R424	C,4	R516	A,4	R561	A,3	R712	B,4	TP17	C,3
R201	C,1	R425	C,4	R517	A,4	R562	A,3	R713	D,4	TP18	D,3
R202	C,2	R426	C,4	R518	B,4	R563	A,3	R714	D,4	TP19	D,3
R203	C,2	R427	C,4	R519	A,4	R564	A,3	R715	D,4	TP20	C,3
R204	C,1	R428	C,4	R520	A,4	R565	B,3	R716	C,4	TP21	C,3
R205	C,1	R429	B,4	R521	A,3	R566	A,3	R717	D,4	TP22	A,3
R206	C,1	R430	C,3	R522	B,4	R567	A,3	R718	E,4	TP23	A,3

A3 Component Coordinates (3 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
TP24	C,3	U35	C,2						
TP25	C,3	U36	D,2						
TP26	C,2	U37	E,2						
TP27	C,2	U38	C,2						
TP28	C,2	U39	C,2						
TP29	C,2	U40	D,2						
TP30	C,1	U41	C,2						
TP31	C,1	U42	C,2						
TP32	D,1	U43	C,2						
TP33	E,1	U44	C,2						
		U45	D,2						
U1	A,4	U46	C,1						
U2	B,4	U47	C,1						
U3	C,4	U48	D,1						
U4	D,4	U49	C,1						
U5	D,4	U50	C,1						
U6	C,4	U51	C,1						
U7	B,4	U52	D,1						
U8	C,4	U53	E,1						
U9	A,4	U54	C,1						
U10	D,4	U55	C,1						
U11	D,4								
U12	E,3	VR300	C,3						
U13	B,3	VR400	B,4						
U14	B,3	VR401	C,4						
U15	E,3	VR500	A,3						
U16	E,3	VR601	B,3						
U17	C,3								
U18	D,3	W1	B,3						
U19	E,3	W2	C,3						
U20	E,3	W3	A,3						
U21	A,3	W4	B,3						
U22	B,3	W5	A,3						
U23	D,3	W6	A,2						
U24	D,3	W7	D,1						
U25	E,3	W8	C,1						
U26	E,3	W9	C,4						
U27	B,3	W10	C,4						
U28	C,3	W11	B,4						
U29	D,3								
U30	D,3	Y1	E,2						
U31	E,3	Y300	C,2						
U32	E,3								
U33	B,3								
U34	B,3								

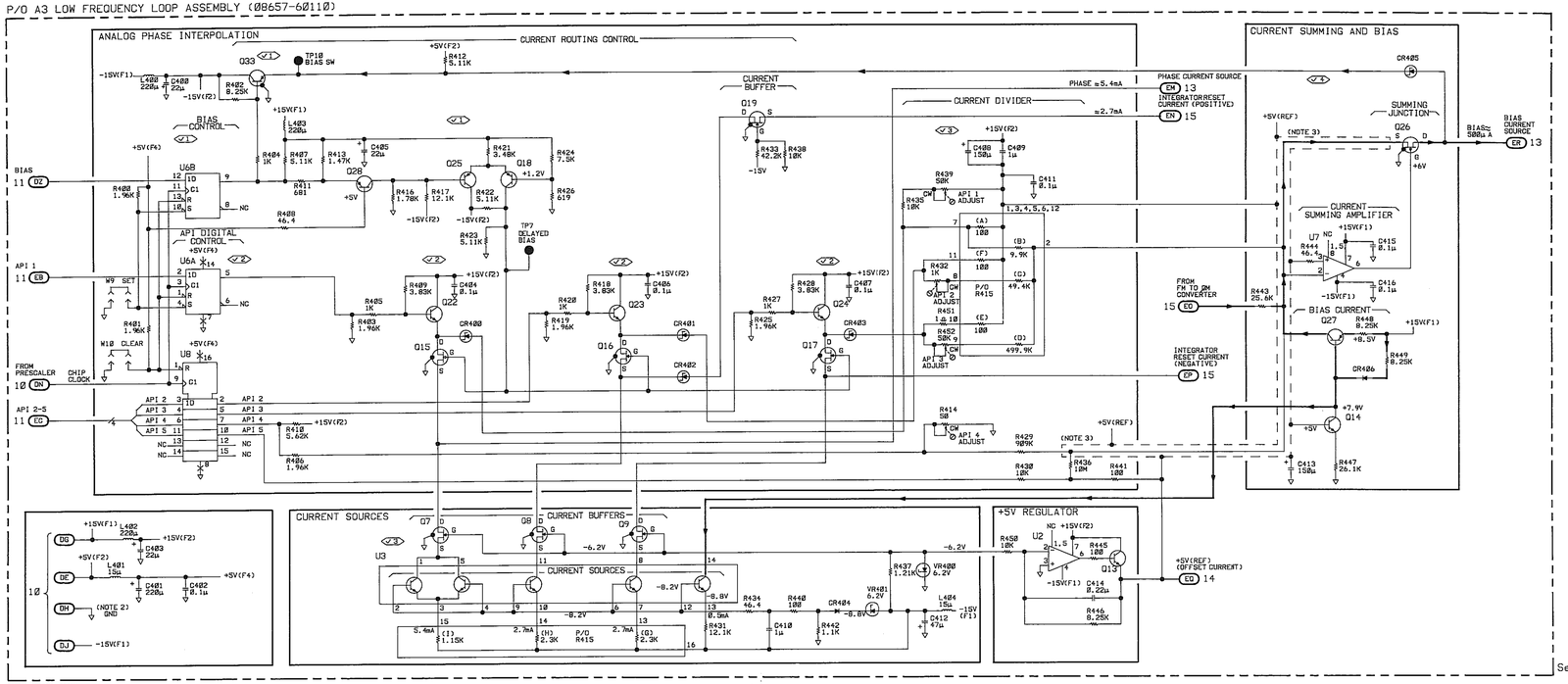


Figure 3
Service Sheet 12 13

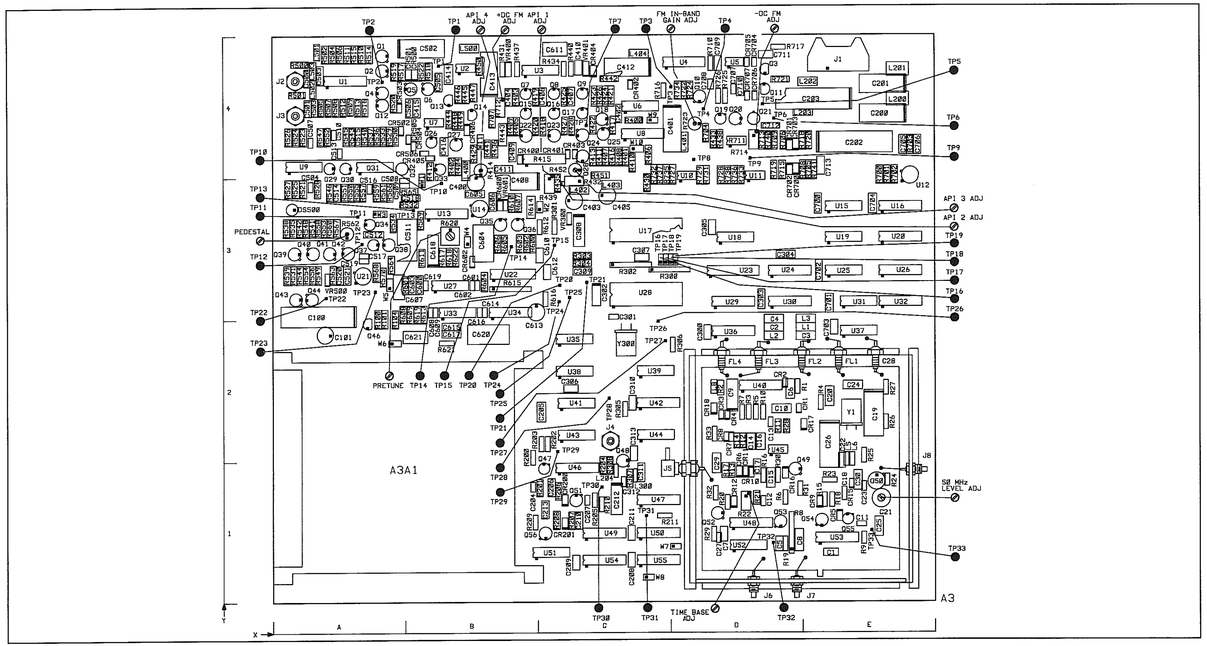


Figure Ø. Service Sheet 13 Information

Component Locator

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Nominal value of RF choke is 2.5-6uH.
3. Chassis ground is achieved by mechanical contact through nuts holding PC board to cover and W14.
4. Isolation (Guard) trace.
5. Reference designations on this service sheet C, CR, L, R and VR have numbers ranging from S00 to S99 only.
6. Inverting input of U21 is internally connected to the output pin 6.

LOGIC LEVELS

	TTL
HIGH	2V
LOW	0.8V
IS MORE NEG. THAN	IS MORE POS. THAN
OPEN	HIGH
GROUND	LOW

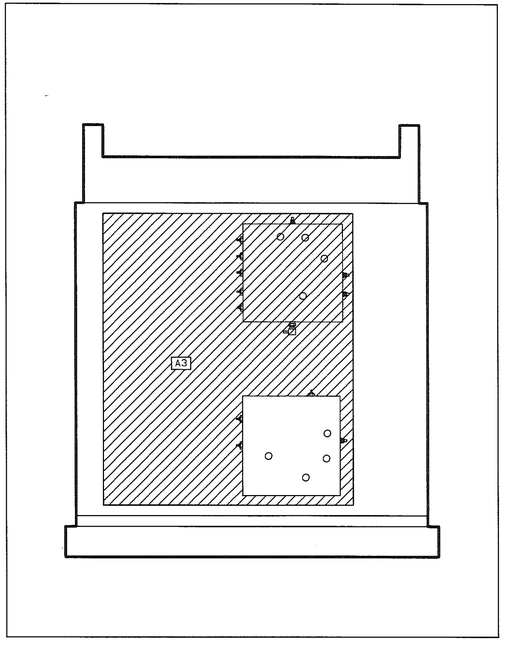
A3U21 TOP VIEW

A3U34,37 TOP VIEW

A3U32 TOP VIEW

P/O A3 LOW FREQUENCY LOOP ANALOG PHASE INTERPOLATION (API), CURRENT SOURCES, CURRENT SUMMING AND BIAS SS12

SEE REVERSE SIDE



Service Sheet 13

LOW FREQUENCY LOOP PHASE DETECTOR, INTEGRATOR, AND SAMPLE AND HOLD

PRINCIPLES OF OPERATION

General

The Phase Detector determines the phase difference between the VCO Divide-By-N.F., and reference inputs. The VCO Divide-By-N.F. input pulse is the Low Frequency Loop VCO's frequency divided by an integer (N.), and a fractional part (F.) for fractional frequencies (refer to Block Diagram 3). The Phase Detector's output pulse width is proportional to the phase difference between the VCO Divide-By-N.F., and the reference inputs. The pulse width determines the length of time current is supplied by the Integrator to ramp its output voltage up. The Sample and Hold circuits stores the Integrator's output voltage on the Sample and Hold Capacitor. The voltage stored on the Sample and Hold Capacitor is the tune voltage for the Low Frequency Loop VCO.

Phase Comparator

The Phase Comparator determines the phase difference between the VCO Divide-By-N.F. input and the Reference input. The pulse width of the Phase Detector output represents the phase difference between the two input signals. The phase of the VCO Divide-By-N.F. leads the phase of the reference when the loop is locked. The clock enable inputs at pins 6 and 11 of ECL Master-Slave Dual D flip-flop U1A and U1B are dc biased just below the ECL low threshold, <3.3V, by dividing the +5 Vdc. The +5 Vdc is divided by resistors R502 and R504 for U1A, and resistors R503 and R505 for U1B. The common clock input at pin 4 of U1A and pin 9 of U1B are both held low by internal pull-down resistors. With the common clock inputs low, U1A and U1B are clocked on the low to high transition of the clock enable inputs at pin 6 of U1A and pin 11 of U1B. The logic levels at each D input is clocked to the Q open emitter outputs. The Low Frequency Loop VCO's output frequency is divided to narrow pulses at a 100 kHz rate. Resistor R500 is an approximate 50 ohm termination for the VCO Divide-By-N.F. input pulses, and capacitor C500 ac couples the pulses to the clock enable input at pin 6 of U1A. U1A is clocked on the low to high transition, and when high resets U1B. The set input at pin 12 of U1B, and the reset input at pin 4 of U1A are held low by internal pull-down resistors. Resistor R501 is an approximate 50 ohm termination for the 100 kHz Reference input, and capacitor C501 ac couples the Reference to the clock enable input at pin 11. The Reference input clocks U1B on the low to high transition, and when high it sets U1A.

VCO Divide-By-N.F. Leads Reference

The VCO Divided-By-N.F. input pulses at a 100 kHz rate leads the 100 kHz Reference input in normal operation. When the Low Frequency Loop is locked and the VCO's frequency is 100 MHz, the 100 kHz pulses lead the Reference pulses by approximately 8 degrees, 0.22 μs. When the VCO's frequency is 60 MHz, the VCO Divide-By-N.F. pulses leads the Reference pulses by approximately 13 degrees, 0.37 μs.

When the VCO Divide-By-N.F. input leads the Reference input, normal operation, the VCO Divide-By-N.F. input at pin 6 clocks U1A on the low to high transition. When high, the VCO Divide-By-N.F. pulse resets U1B. When U1B is reset the output at pin 15 is low, and the output at pin 14 is high. The low D input at pin 7 of U1A is then clocked to the output at pin 2 and is applied to the D input at pin 10 of U1B. The Reference pulse at pin 11 of U1B clocks the low D input of U1B to the output at pin 15 and sets U1A. The output at pin 2 of U1A is set high and the output at pin 3 is set low. The next VCO Divide-By-N.F. input pulse clocks the low D input of U1A to the output at pin 2, and resets the output at pin 15 of U1B low. Therefore, the output at pin 15 of U1B is always low when the VCO Divide-By-N.F. input leads the Reference input. Refer to the Timing VCO Divide-By-N.F. Leads Reference, Figure 1.

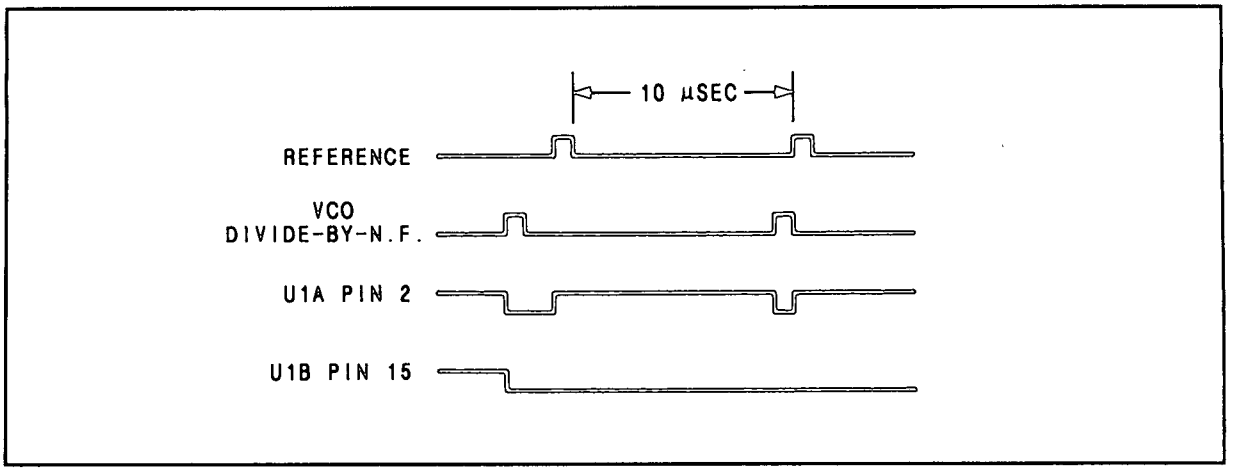


Figure 1. Timing VCO Divide-By-N.F. Leads Reference.

The low output at pin 15, and the high output at pin 14 of U1B is the bias voltage for differential switch transistors Q1 and Q2. The low output at pin 15 turns Q1 on, and the high output at pin 14 turns Q2 off. CR503 is turned on, and CR505 is turned off. The diodes remain in this condition unless the Reference input pulse leads the VCO Divide-By-N.F. pulse.

The VCO Divide-By-N.F. pulse clocks the low D input to the output at pin 2 of U1A, and the output at pin 3 of U1A high. The low output at pin 2, and the high output at pin 3 of U1A is the base voltage for differential switch Q12 and Q4. The low output at pin 12 turns Q12 on, and the high output at pin 3 turns Q4 off. With no current through Q4, the bias voltage on the base of Q5 is approximately −0.4V and the emitter voltage is then approximately −1.0V. The −1.0V turns CR502 off, and turns CR504 on. The anode voltage of CR504 is approximately 0.0V. When the Bias pulse and API pulses are inactive (refer to Service Sheet 12), the 5.4 mA's of API 1 current is directed from the node between diodes CR502 and CR504. With CR504 on, the Integrator supplies current for the API 1 current source. The Integrator's output voltage is ramped to a voltage dependent upon the phase error between the VCO Divide-By-N.F. input and the Reference input. The Reference pulse sets U1A's output at pin 2 high and the output at pin 3 low. Transistor Q12 is turned off, and Q4 is turned on. The current through Q4 biases the base of Q5 at approximately +1.6V, and the emitter voltage is approximately +1.0V. The +1.0V turns on CR502, and API 1 current is then supplied by Q5. When CR502 is turned on, CR504 can not be turned on. Refer to the Low Frequency Loop Timing Diagram, Figure 7.

Reference Leads VCO Divide-By-N.F.

The VCO Divided-By-N.F. input pulses at a 100 kHz rate leads the 100 kHz Reference input pulses in normal operation. If the Reference pulses leads the VCO Divide-By-N.F. pulses, the speed-up circuit of Q1 and Q2 will tune the VCO until the VCO Divide-By-N.F. input leads the Reference input. When the Reference input leads the VCO Divide-By-N.F. input, the Reference clocks U1B on the low to high transition and when high it sets U1A. The high D input at pin 10 of U1B is clocked to the output at pin 15, and the output at pin 2 of U1A is set high. The VCO Divide-By-N.F. input will clock the high D input of U1A to the output at pin 2, and will reset U1B. The output at pin 15 of U1B is then reset low. The next Reference input clocks the high D input of U1B to the output at pin 15, and set the output at pin 2 of U1A high. Therefore, the output at pin 2 of U1A remains high as long as the Reference input leads the VCO Divide-By-N.F. input. Refer to Figure 2.

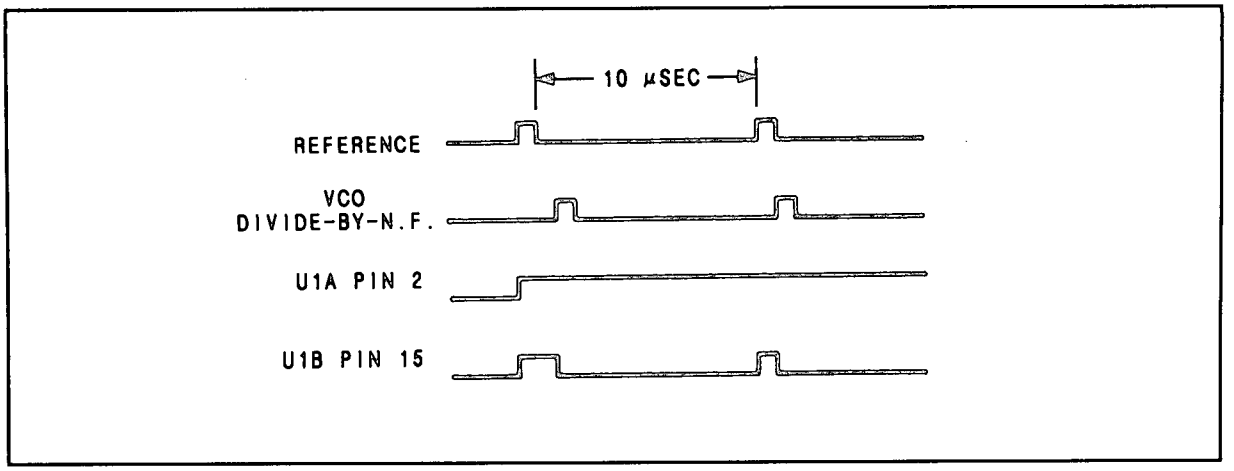


Figure 2. Timing Reference Leads VCO Divide-By-N.F.

The speed-up circuit consists of differential switch Q1 and Q2, and diodes CR503 and CR505. The speed-up circuit tunes the frequency of the VCO quickly until the VCO Divide-By-N.F. input to the Phase Comparator leads the Reference. The high output at pin 15, and low output at pin 14 of U1B is the base voltage for the differential switch. The Reference input clocks the output at pin 15 high, and the output at pin 14 low. The high output at pin 15 turns Q1 off, and the low output at pin 14 turns Q2 on. The collector voltage of Q2 rises above 0.0V. CR503 is turned off, and CR505 is turned on. Current is directed through CR505 to the Integrator and the VCO's frequency is increased. The VCO Divide-By-N.F. input resets the output at pin 15 of U1B low, and the output at pin 14 high. Q1 is turned on and Q2 is turned off. With no current through Q2, CR503 is turned on and CR505 is reverse biased at approximately 0.5V. The speed-up circuit is active (on) until the VCO Divide-By-N.F. input leads the Reference input.

The high output at pin 2, and low output at pin 3 of U1A is the base voltage for the differential switch, transistors Q12 and Q4. The output at pin 2 remains high, and Q12 is off and Q4 is on. The current through Q4 biases the base of Q5 at approximately +2.0V, and the emitter is biased at approximately +1.0V. The +1.0V turns CR502 on to supply current to the API 1 current source. When CR502 is turned on, CR504 can not be turned on. All current going to the Integrator is from the speed-up circuit.

This condition exists until the VCO Divide-By-N.F. input leads the Reference input, and lasts for a number of milliseconds. The number of milliseconds is dependent upon the amount the VCO frequency is changed.

Unlock Detection Comparators

The Low Frequency Loop Unlock Detection Comparators, U9A and U9B, detect when the loop is unlocked, light the unlock LED, and send an Out-Of-Lock (L) input to the Low Frequency Loop Microprocessor. The positive input at pin 4 of U9A is fixed at approximately −0.3 Vdc divided from −15 Vdc by resistors R525 and R527. The negative input at pin 10 of U9B is fixed at approximately +0.87 Vdc divided from +5 Vdc by resistors R524 and R526. Resistor R521 and capacitor C504 average the voltage at the collector of Q2 to detect an out-of-lock condition. Resistor R523 and capacitor C507 average the voltage at the emitter of Q5 to detect an out-of-lock condition. When the loop is unlocked, either the negative input at pin 5 of U9A can go positive or the positive input of U9B can go negative switching their output low, detecting an out-of-lock condition. The comparator's output that is switched low is dependent upon which input is leading. If the Reference input pulse is leading the VCO Divide-By-N.F. input pulse, comparator U9A is switched. If the VCO Divide-By-N.F. pulse is leading, the Reference pulse U9B is switched. The negative input of U9A is approximately −0.5V when the loop is locked and changes to approximately +0.6 when the loop is unlocked. The Reference leads the VCO Divide-By-N.F.. The positive input at pin 9 of U9B is approximately +1.0V when the loop is locked and changes to approximately −1.0V when the loop

is unlocked. The VCO Divide-By-N.F. leads the Reference. In either case, the LED is turned on, and the Out-Of-Lock (L) input to the Microprocessor is low.

Integrator

The Integrator is a wide bandwidth fast settling Operational Amplifier and consists of dual FET U32, transistors Q29, Q30, and Q31. The Integrator's output voltage is determined by parallel capacitors C508 and C509, and the input current. There are two current inputs to the Integrator, Bias Current and Phase Detector controlled API 1 Current. After the Integrator's output voltage has been sampled by the Sample and Hold Circuits, Bias Current ramps the Integrator's output voltage down to reset the Integrator. The Phase Detector's output pulse controls the length of time API 1 Current is supplied by the Integrator. The Integrator's output voltage is ramped up to a voltage dependent on the pulse width of the Phase Detector's output. The pulse width is determined by the phase difference between the VCO Divide-By-N.F. and the input pulses.

FET Q32, is a common source, unity gain, high input impedance Buffer Amplifier for the Differential Pair Q31C and Q31D. The gate at pin 3 of the dual FET Q32, is connected to ground, and the gate at pin 6 is fixed at approximately 0.0V by feedback around the operational amplifier. The sources at pins 4 and 1 are biased slightly above ground by approximately 1 mA of current through resistors R529, R540, and the FET's. The bias voltage for the dual FET sources is also the base voltage for the Differential Pair Q31C and Q31D, and sets their bias conditions. Current through Q31C and Q31D is approximately 4 mA each. The input at pin 6 of Q32 appears amplified and inverted at the collector of Q31C and drives the emitter of Q30 like a common base amplifier. The input also appears amplified but not inverted at the collector of Q31D, and drives the base of Q30 like a common emitter amplifier. Driving both the emitter and the base increases the dc gain of the stage. Bias for Q30 is set by the collector currents of Q31C and Q31D. Transistor Q29, is an active load and current source for Q30. Q29 has a high output impedance so the load that Q30 sees is primarily the input impedance of the Darlington dual emitter follower output stage Q31A and Q31B. Transistor Q30 supplies most of the voltage gain of the amplifier. At higher frequencies the gain is reduced by capacitor C513 shunting part of the signal to ground. Additional compensation is provided by capacitor C510 which shunts high frequency signals on the collector of Q31D (base of Q30) to ac ground. Although Q30 is driven as a common emitter and common base amplifier, at higher frequencies Q30 functions only as a common base amplifier with all of its input at the emitter. Emitter follower Q31A is biased by approximately 3 mA of current through resistor R559. Emitter follower Q31B is biased by approximately 6 mA of current 1 mA through resistor R556 and 5 mA to the Sample and Hold Circuit. The output impedance of an emitter follower can look inductive and cause ringing when driving capacitive loads. To correct for this condition, RC networks of R557, C516 and R565, C518, connected to the output of the emitter followers Q31A and Q31B, makes their output impedance look resistive at high frequencies.

Frequency Compensation RC Circuit of resistor R534 and capacitor C511 add Integrator gain at low frequencies and improves the stability of the phase lock loop.

Sample and Hold

The Sample and Hold Circuit is activated by the Sample and Hold pulse, active high for two Chip Clocks, from the Low Frequency Loop Fractional-N Controller. (Refer to Service Sheet 11, and the Timing Diagram Figure 7.) At the termination of the Phase Detector pulse, the Integrator's output voltage is representative of the phase difference between the VCO Divide-By-N.F., and the Reference input pulses to the Phase Detector. The first two Chip Clocks of each cycle, activates the Sample and Hold Circuit, and the Integrator's voltage is stored on the Sample and Hold capacitor C519. The VCO is then phase locked to the correct frequency.

The TTL high (>+2.0V) Sample and Hold Pulse from the Fractional N Controller, turns Q44 off. Its base voltage is changed from approximately −0.6V to approximately +1.5V. When transistor Q44 is turned off, transistors Q40 and Q41 are also turned off. When transistors Q40 and Q41 are off, the two FET switches Q34 and Q37 are closed (turned on). The Integrator's output voltage is then applied to capacitor C512 and to the Sample and Hold Capacitor C519. The capacitors then charge

to the output voltage of the Integrator. Transistor Q43 is turned on when transistor Q44 is turned off. Q43's base voltage changes from 0.0V to approximately +0.3V. When transistor Q43 is on, transistor Q39 and Q42 are also turned on.

When the Sample and Hold pulse is terminated, the base of transistor Q44 changes from approximately +1.5V to approximately −0.6V. Q44 is turned on. The base voltage of transistors Q40 and Q41 is less negative, and they are turned on. When Q40 and Q41 are turned on, the gate of FET switches Q34 and Q37 is 8V to 10V below their source voltage. The FET switches are opened (turned off). The Integrator's output voltage at this time is not sampled. Transistor Q43 is turned off when transistor Q44 is turned on. Q43's base voltage changes from approximately +0.3V to 0.0V. When transistor Q43 is off, transistors Q39 and Q42 are also turned off. One transistor of each differential pair, Q39 and Q40, Q41 and Q42, Q43 and Q44, is on while the other transistor is off. With one transistor of the differential pairs always on, there is a constant current through their emitter resistors R542, R560, R544, and a constant voltage on their emitters.

Capacitor C517 reduces a spur caused by the gate to drain capacitance of FET switch Q37. The gate to drain capacitance of Q37 provides an ac path to the Sample and Hold Capacitor C519 each time FET switch Q37 is closed.

The gate voltage is changed at the start of each Sample and Hold pulse, and FET switch Q37 is closed. Differential pair Q41 and Q42 are always in opposite states of on and off. Capacitor C517 provides an ac path to the Sample and Hold Capacitor and an equal but opposite polarity pulse is applied to C519. Resistor R562 is adjusted so that the pulses are equal, and since they are opposite in polarity the pulses cancel. The adjustment of R562 determines the voltage at the collector of Q42 and the amplitude of the pulse.

FET switches Q34 and Q37 must be biased when they are switched on during the Sample and Hold cycle. They are biased where Vgs is just below 0.0V. The output voltage of the Integrator is at the correct level to bias Q34, and the Sample and Hold voltage on C519 is at the correct level to bias Q37. When the Low Frequency Loop is locked, the two voltages are equal. The Integrator's voltage is connected to the gate of Q34 by resistor R541, and the Integrator's cycle is shown by the waveform at TP11. Figures 3 and 4 show the waveform at TP11 and TP12 with the Low Frequency Loop locked and a Signal Generator RF output frequency of 950 MHz. In Figures 5 and 6, the Signal Generator's RF output is 990 MHz. The voltage level shifts as the VCO's TUNE VOLTAGE is changed to tune its frequency 100 MHz to 60 MHz.

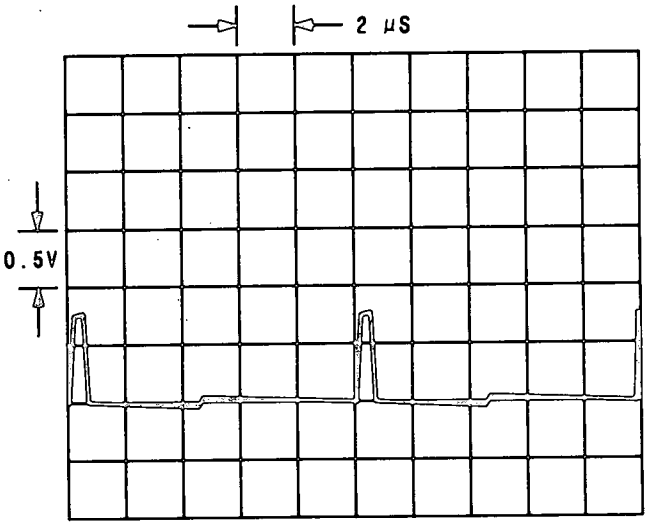


Figure 3. Oscilloscope Display of TP11 (dc coupled), W3 in W3A position, Low Frequency Loop locked, Signal Generator's frequency 950 MHz.

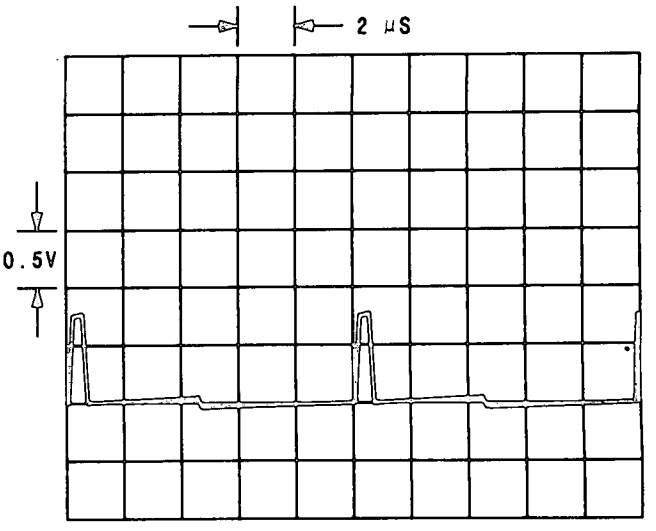


Figure 4. Oscilloscope Display of TP12 (decoupled) W3 in W3A position, Low Frequency Loop locked, Signal Generator's frequency 950 MHz.

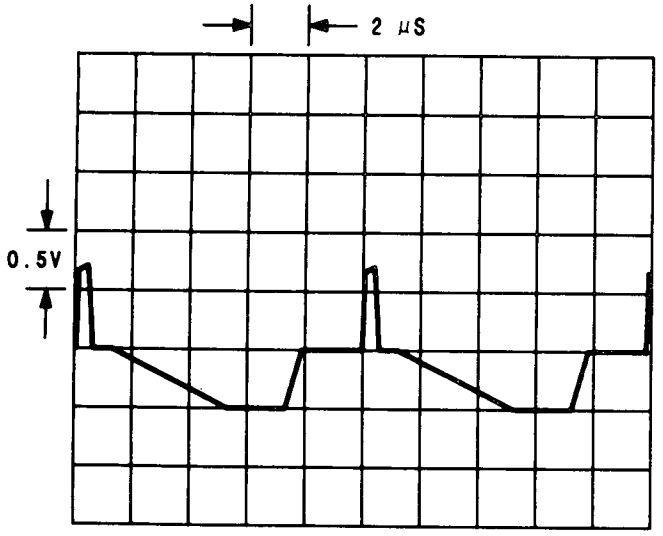


Figure 5. *Oscilloscope display of TP11 (dc coupled) W3 in W3A position, Low Frequency Loop locked, Signal Generator's frequency 990 MHz.*

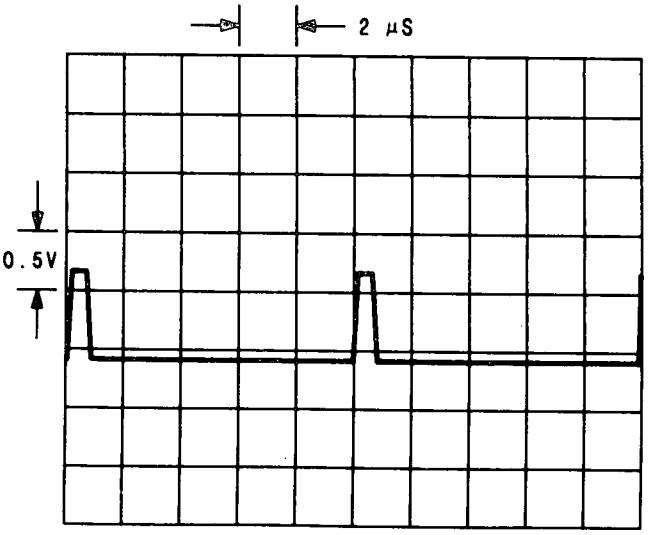


Figure 6. *Oscilloscope Display of TP12 W3 toW3A position, Low Frequency Loop locked, Signal Generator's frequency 990 MHz.*

To apply the Sample and Hold voltage to the gate of Q37 is more difficult. By connecting the source of Q37 to the collector resistors of Q41 and Q42 the Sample and Hold voltage would be connected to the gate of Q37. However, one transistor of the differential pair Q41 and Q42 is always on and the Sample and Hold Capacitor C519 would be quickly discharged through either Q41 or Q42. The voltage on the Sample and Hold Capacitor must be constant between samples so that the VCO frequency does not change. To prevent the voltage on C519 from changing, C519 is connected to a unity gain high input impedance Buffer Amplifier U21. The output of the Buffer Amplifier is connected through transistor Q38 back to the collector resistors of Q41 and Q42. The Sample and Hold voltage biases the gate of Q37 during the Sample and Hold pulse, and will not discharge the Sample and Hold Capacitor C519. Transistor Q38 reduces the amount of current U21 must supply. The output of U21 is also the TUNE VOLTAGE for the Low Frequency Loop VCO, and the Pedestal adjustment is adjusted for a continuous Sample and Hold voltage.

Two FET switches Q34 and Q37 are used to reduce feedthrough of the Integrator's voltage when the FET switches are off. With the FETs turned off there is still approximately 1 to 2 pF of source-to-drain capacitance. The FET's source-to-drain capacitance forms an ac voltage divider with capacitors C512 and C519 isolating the Integrator's changing voltage during the time of each cycle that the Sample and Hold operation is turned off. If the feedthrough was not reduced, there would be high 100 kHz and API spurs.

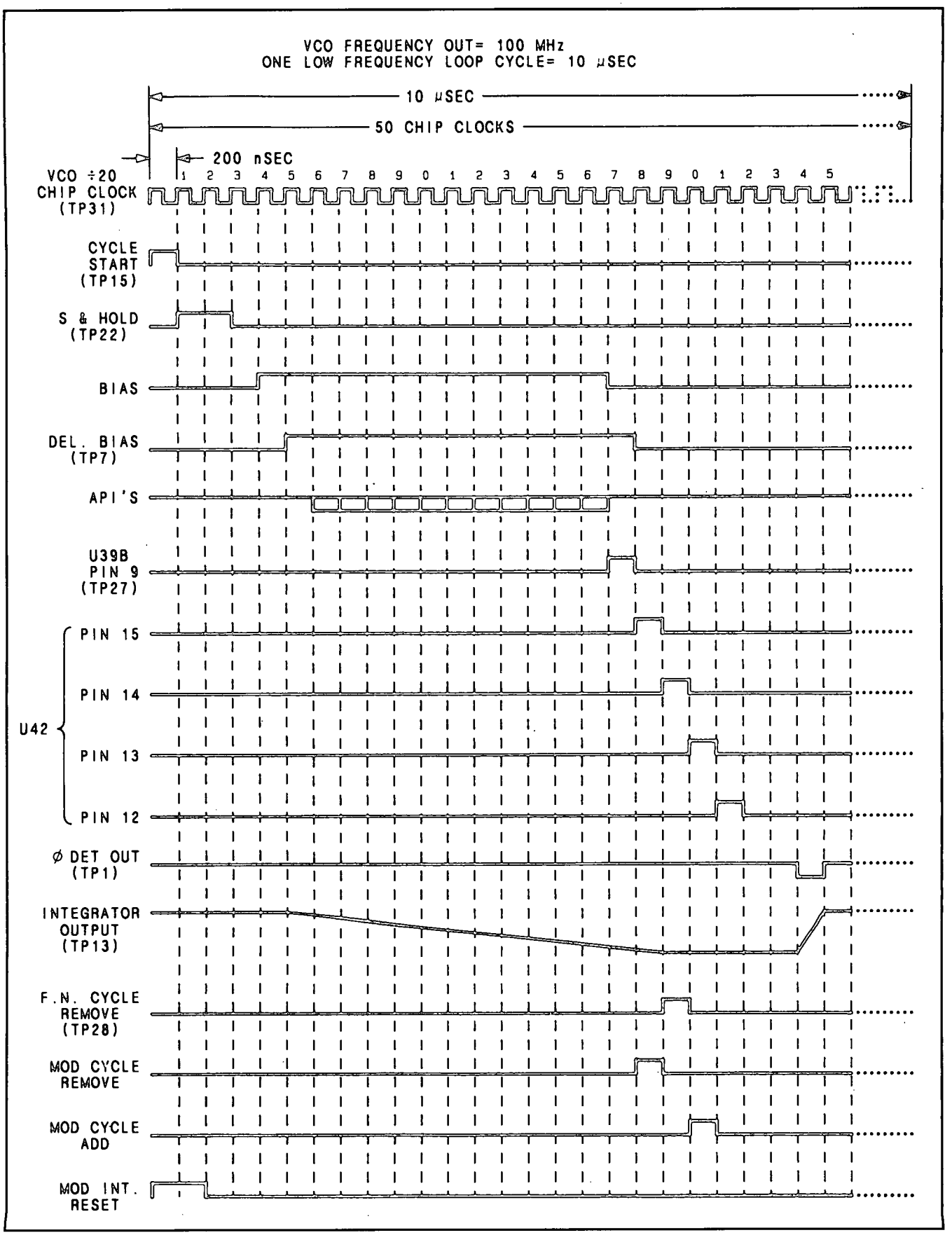


Figure 7. Low Frequency Loop Timing Diagram.

TROUBLESHOOTING

Procedures for checking part of the A3 Low Frequency Loop Assembly circuits are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, for example, ⟨✓1⟩. Transistor bias voltages are shown without tolerances.

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Digital Multimeter	HP 3466A
Oscilloscope	HP 54100A
Frequency Counter	HP 5328A
Audio Source	HP 8903B
Oscilloscope 1 Megohm Probe Pod Chan 2	HP 54003A
Oscilloscope Probe	HP 54003-61617

⟨✓1⟩ Phase Detector, Integrator, Sample and Hold

1. The Phase Detector, Integrator, and Sample and Hold circuits are checked for proper operation with the Low Frequency Loop unlocked.
2. Remove jumper A3W6 (refer to Service Sheet 14). The TUNE VOLTAGE input to the Low Frequency Loop VCO at feedthrough capacitor C100 goes to approximately 0.0V (refer to Service Sheet 9).
3. Set the RF output frequency of the Signal Generator to 990 MHz.
4. Set the Oscilloscope as follows:

Chan 1

Ch 1 Display	Off

Chan 2

Ch 2 Mode	Normal
Ch 2 Display	On
VOLTS/DIV	500 mV
OFFSET	3.0V

Timebase

SEC/DIV	20 ns
DELAY	0.0s
Delay Ref at	Center
Sweep	Trg'd

Trigger

Trigger Mode	Edge
Trig Src	Chan 2
TRIG LEVEL	3.5V
Slope	Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 400 ms
Split Screen ..... Off
Graticle ..... On

5. Check for the VCO Divide-By-N.F., and the 100 kHz Reference pulses at pin 6 and pin 11 of U1. The pulses are ECL logic, appear every 10 μs, and are narrow. They must be present for the Phase Detector to work.
6. Set the Signal Generator's frequency increment to 10 MHz.
7. Connect Chan 2 to W5. If the voltage displayed on the oscilloscope is +10V, increment the Signal Generator's frequency DOWN 10 MHz. The voltage on the oscilloscope should change to −10V. If the voltage displayed is −10V increment the frequency up and voltage should change to +10V.
8. The voltage on the oscilloscope should change from +10 to −10V as the frequency is incremented UP and DOWN 10 MHz. The Phase Detector, Integrator and Sample and Hold circuits are all working correctly. The +10V to −10V is the maximum swing of the Integrator.

⟨√2⟩ Phase Detector

1. With the Low Frequency Loop VCO and Signal Generator set-up the same as for steps 2 through 3 of ⟨√1⟩ the Phase Detector is checked.
2. Increment the frequency UP 10 MHz. The VCO Divide-By-N.F. input is leading the Reference input.
3. Set the Oscilloscope as follows:

Chan 1

Ch 1 Display ..... Off

Chan 2

Ch 2 Mode ..... Normal
Ch 2 Display ..... On
VOLTS/DIV ..... 500 mV
OFFSET 0V

Timebase

SEC/DIV ..... 10 μs
DELAY 0.0s
Delay Ref at ..... Left
Sweep ..... Auto

Trigger

Trigger Mode ..... Edge
Trig Src ..... Chan 2
TRIG LEVEL ..... 500 mV
Slope ..... Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 200 ms
Split Screen ..... Off
Graticle ..... On

4. Connect Chan 2 to TP1 (PHASE DET). The pulses at TP1 should be from +1V to −1V and are unstable since the loop is not locked.
5. If the pulses are not present at TP1, check that the output of U1A is changing between ECL high and low.
6. Check that the base of Q4, and Q12 is being pulsed from approximately +3V to approximately +4V. Check that the base of Q5 is being pulsed from approximately −0.6V to approximately +2V. Check that the base of Q6 is being pulsed from approximately −2V to approximately +0.6V.
7. Pin 9 of U9B is also pulsed, and the out-of-lock LED (DS500) is on.
8. Connect Chan 2 to TP2 (SPEEDUP). The pulses at TP2 should be approximately 0V to +5V and unstable since the loop is not locked.
9. If the pulses are not present at TP2, check that the output of U1B is changing between ECL high and low.
10. Check that the base of Q1 and Q2 is being pulsed from approximately +3V to approximately +4V.
11. Pin 5 of U9A is also pulsed and the out-of-lock LED (DS500) is on.
12. Reinstall jumper A3W6.

⟨3⟩ Integrator

1. Remove jumper A3W1 from position W1A and install A3W1 in position W1B. Remove A3W3 from the W3A position.
2. Connect a 1 kHz 0.1V signal from the audio source to A3W1.

Table 1. *Integrator Voltages with W1 in W1B Position.*

Transistor	Emitter (Vdc)	Base (Vdc)	Collector (Vdc)
Q31C	Pin 10, −0.75	Pin 9, −0.025	Pin 8, +12.5
Q31D	Pin 12, −0.75	Pin 13, −0.025	Pin 14, +12.0
Q30	— +12.5	— +11.9	— +1.3
Q29	— −13.2	— −12.5	— +1.3
Q31A	Pin 3, +0.5	Pin 2, +1.2	Pin 1, +14.0
Q31B	Pin 5, −0.007	Pin 6, +0.6	Pin 7, +14.0

3. Connect Chan 2 of the oscilloscope to TP13. The output at TP13 should be a 500 mVpp, 1 kHz signal.
4. Measure the transistor voltages according to Table 1.
5. Reinstall A3W1 to position W1A (normal operation).

⟨4⟩ Sample and Hold

1. Install A3W3 in the W3B position. +5V(F2) is thus connected to the input of the Sample and Hold circuit.
2. Connect Chan 2 of the oscilloscope to TP23. The output at TP23 should be +5V (+5V at W5).

3. If +5V is not present at TP23, check the Sample and Hold pulse at TP22 (SAMPLE). Verify that the waveform in Figure 8 is correct. (The VCO frequency with W6 removed and the Signal Generator's frequency will affect the time between pulses.)

4. Verify that the waveform in Figure 9 is correct.
5. Verify that the waveform in Figure 10 is correct.
6. Reinstall A3W3 in the W3A position.

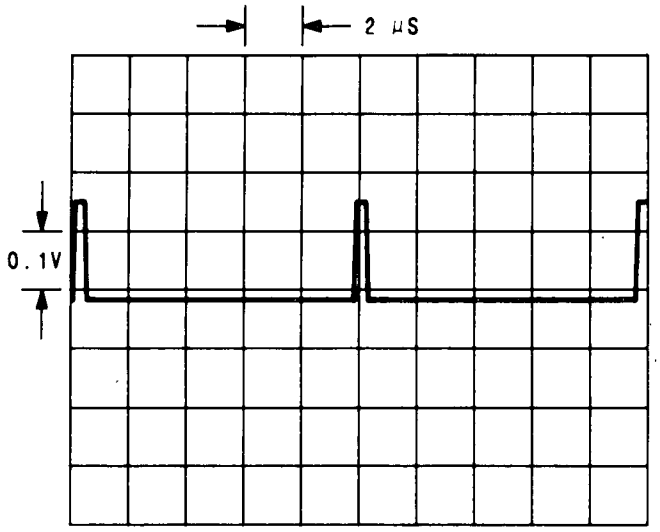


Figure 8. *Oscilloscope Display of TP22, Sample and Hold Pulse, W6 removed, Signal Generator's frequency is 960 MHz, Low Frequency Loop is unlocked.*

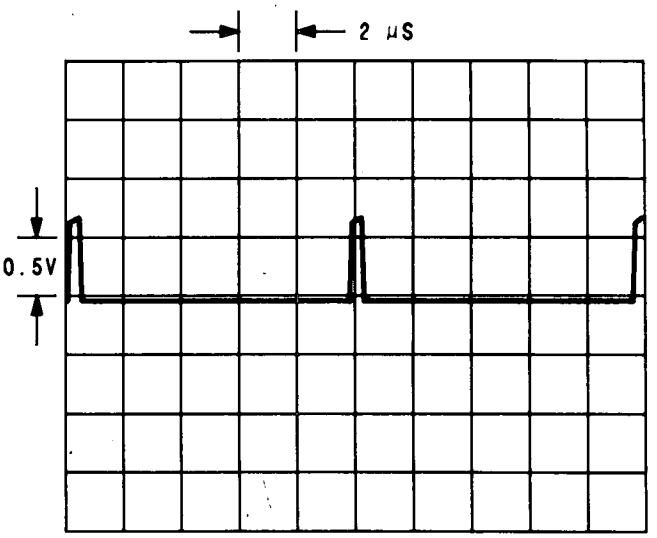


Figure 9. *Oscilloscope Display of TP11, W3 in position W3B (service position), Signal Generator's frequency 960 MHz.*

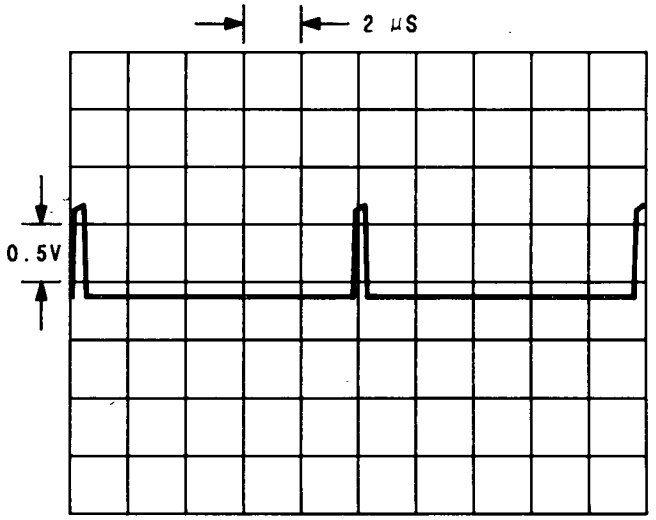


Figure 10. *Oscilloscope Display of TP12, W3 in position W3B (service position), Signal Generator's frequency 960 MHz.*

A3 Component Coordinates (1 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	E,1	C213	C,1	C513	A,4	CR1	D,2	FL1	E,2	Q10	D,4
C2	D,2	C300	D,2	C514	A,3	CR2	D,2	FL2	E,2	Q11	D,4
C3	E,2	C301	C,3	C515	A,4	CR3	D,2	FL3	D,2	Q12	A,4
C4	D,2	C302	C,3	C516	A,3	CR4	D,2	FL4	D,2	Q13	B,4
C5	D,1	C303	D,3	C517	A,3	CR5	E,1			Q14	B,4
C6	D,2	C304	D,3	C518	B,3	CR6	D,1	J1	E,4	Q15	B,4
C7	D,1	C305	D,3	C519	A,3	CR7	D,2	J2	A,4	Q16	C,4
C8	D,1	C306	C,2	C520	A,3	CR8	D,2	J3	A,4	Q17	C,4
C9	D,2	C307	C,3	C521	A,3	CR9	E,1	J4	C,2	Q18	C,4
C10	D,2	C308	C,3	C600	B,3	CR10	D,1	J5	C,1	Q19	D,4
C11	E,1	C309	C,3	C601	B,3	CR11	D,1	J6	D,1	Q20	D,4
C12	D,1	C310	C,2	C602	B,3	CR12	D,1	J7	E,1	Q21	D,4
C13	D,2	C311	C,1	C603	B,3	CR15	E,1	J8	E,2	Q22	B,4
C14	D,2	C312	C,1	C604	B,3	CR16	D,1			Q23	C,4
C15	D,1	C313	C,2	C605	B,3	CR17	E,2	L1	E,2	Q24	C,4
C16	D,2	C400	B,3	C606	B,3	CR18	D,2	L2	D,2	Q25	C,4
C17	D,1	C401	D,4	C607	B,3	CR200	C,1	L3	E,2	Q26	B,4
C18	E,1	C402	C,4	C608	B,3	CR201	C,1	L5	E,2	Q27	B,4
C19	E,2	C403	C,3	C609	B,3	CR400	B,4	L6	E,2	Q28	C,4
C20	E,2	C404	B,4	C610	C,3	CR401	C,4	L8	D,2	Q29	A,4
C21	E,1	C405	C,3	C611	C,4	CR402	C,4	L200	E,4	Q30	A,4
C22	E,2	C406	C,4	C612	C,3	CR403	C,4	L201	E,4	Q31	A,4
C23	E,1	C407	C,4	C613	B,3	CR404	C,4	L202	E,4	Q32	A,4
C24	E,2	C408	B,3	C614	B,3	CR405	B,4	L203	E,4	Q33	B,4
C25	E,1	C409	B,4	C615	B,2	CR406	B,4	L204	C,1	Q34	A,3
C26	E,2	C410	C,4	C616	B,3	CR500	B,4	L300	C,1	Q35	B,3
C27	D,1	C411	B,4	C617	B,2	CR501	B,4	L400	B,4	Q36	B,3
C28	E,2	C412	C,4	C618	B,3	CR502	A,4	L401	D,4	Q37	A,3
C29	D,1	C413	B,4	C619	B,3	CR503	A,4	L402	C,3	Q38	A,3
C30	E,1	C414	B,4	C620	B,2	CR504	B,4	L403	C,3	Q39	A,3
C100	A,3	C415	B,4	C621	B,2	CR505	B,4	L404	C,4	Q40	A,3
C101	A,2	C416	B,4	C700	E,3	CR506	B,4	L500	B,4	Q41	A,3
C200	E,4	C500	A,4	C701	E,3	CR600	B,3	L501	A,4	Q42	A,3
C201	E,4	C501	A,4	C702	E,3	CR602	B,3	L502	A,4	Q43	A,3
C202	E,4	C502	B,4	C703	E,2	CR700	D,4	L503	A,4	Q44	A,3
C203	E,4	C503	A,4	C704	E,3	CR701	D,4			Q46	A,2
C204	B,1	C504	A,3	C705	E,4	CR702	D,4	Q1	A,4	Q47	C,1
C205	C,2	C505	B,4	C706	E,4	CR703	D,4	Q2	A,4	Q48	C,2
C206	C,1	C506	B,4	C707	D,4	CR704	D,4	Q3	D,4	Q49	D,1
C207	C,1	C507	A,4	C708	D,4	CR705	D,4	Q4	A,4	Q50	E,1
C208	C,1	C508	B,3	C709	D,4	CR706	D,4	Q5	B,4	Q51	C,1
C209	C,1	C509	B,3	C710	D,4	CR707	D,4	Q6	B,4	Q52	D,1
C210	C,1	C510	A,4	C711	D,4			Q7	B,4	Q53	D,1
C211	C,1	C511	B,3	C712	D,4			Q8	C,4	Q54	E,1
C212	C,1	C512	A,3	C713	E,4	DS500	A,3	Q9	C,4	Q55	E,1

A3 Component Coordinates (2 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
Q56	C,1	R207	C,1	R431	B,4	R523	A,4	R568	A,3	R719	D,4
		R208	C,1	R432	C,3	R524	A,4	R569	B,3	R720	E,4
R1	D,2	R209	B,1	R433	D,4	R525	A,3	R570	A,3	R721	D,4
R2	D,2	R210	C,1	R434	C,4	R526	A,4	R600	B,3	R722	D,4
R3	D,2	R211	C,1	R435	C,3	R527	A,3	R601	B,3	R723	D,4
R4	E,2	R300	C,3	R436	B,4	R528	A,3	R602	B,3	R724	D,4
R5	D,2	R301	C,3	R437	B,4	R529	A,4	R603	B,3	R725	D,4
R6	D,1	R302	C,3	R438	D,4	R530	A,4	R604	B,3	R726	D,4
R7	D,2	R303	C,3	R439	C,3	R531	A,3	R605	B,3	R727	D,4
R8	D,1	R304	C,3	R440	C,4	R532	B,3	R606	B,3	R728	D,4
R9	E,1	R305	C,2	R441	B,4	R533	A,4	R607	B,3	R729	D,4
R10	D,2	R306	D,2	R442	C,4	R534	A,3	R608	A,3	R731	D,4
R11	D,2	R307	C,1	R443	B,4	R535	A,3	R609	B,3	R732	C,4
R12	D,2	R308	C,1	R444	B,4	R536	A,4	R610	B,3	R733	D,4
R13	D,1	R400	C,4	R445	B,4	R537	A,4	R611	B,3	R734	D,4
R14	D,2	R401	C,4	R446	B,4	R538	A,3	R612	C,3	R735	C,4
R15	E,1	R402	B,4	R447	B,4	R539	A,3	R613	B,3	R736	D,4
R16	D,1	R403	B,4	R448	B,4	R540	A,4	R614	B,3	R737	C,4
R17	D,1	R404	B,4	R449	B,4	R541	A,3	R615	B,3	R738	D,4
R18	E,1	R405	B,4	R450	B,4	R542	A,3	R616	C,3	R740	D,4
R19	D,1	R406	C,4	R451	C,4	R543	A,4	R617	B,3	R741	E,4
R20	D,1	R407	C,4	R452	C,4	R544	A,3	R618	B,3		
R21	D,1	R408	C,4	R500	A,4	R545	A,4	R619	B,3	TP1	B,4
R22	D,1	R409	B,4	R501	A,4	R546	A,3	R620	B,3	TP2	A,4
R23	E,1	R410	C,4	R502	A,4	R547	A,4	R621	B,2	TP3	D,4
R24	E,1	R411	C,4	R503	A,4	R548	A,3	R622	B,3	TP4	D,4
R25	E,2	R412	B,4	R504	A,4	R549	A,3	R700	E,4	TP5	D,4
R26	E,2	R413	C,4	R505	A,4	R550	A,3	R701	E,4	TP6	D,4
R27	E,2	R414	B,4	R506	A,4	R551	A,3	R702	E,4	TP7	C,4
R28	D,2	R415	C,4	R507	A,4	R552	A,4	R703	E,4	TP8	D,4
R29	D,1	R416	C,4	R508	A,4	R553	A,3	R704	D,4	TP9	D,4
R30	D,1	R417	C,4	R509	A,4	R554	A,3	R705	E,4	TP10	B,3
R31	D,1	R418	C,4	R510	A,4	R555	A,3	R706	D,4	TP11	A,3
R32	D,1	R419	B,4	R511	A,4	R556	A,3	R707	B,4	TP12	A,3
R33	D,2	R420	B,4	R512	A,4	R557	A,3	R708	E,4	TP13	B,3
R100	A,2	R421	C,4	R513	A,4	R558	A,3	R709	D,4	TP14	B,3
R101	A,2	R422	C,4	R514	A,4	R559	A,3	R710	D,4	TP15	C,3
R104	A,2	R423	C,4	R515	A,4	R560	A,3	R711	D,4	TP16	C,3
R200	B,2	R424	C,4	R516	A,4	R561	A,3	R712	B,4	TP17	C,3
R201	C,1	R425	C,4	R517	A,4	R562	A,3	R713	D,4	TP18	D,3
R202	C,2	R426	C,4	R518	B,4	R563	A,3	R714	D,4	TP19	D,3
R203	C,2	R427	C,4	R519	A,4	R564	A,3	R715	D,4	TP20	C,3
R204	C,1	R428	C,4	R520	A,4	R565	B,3	R716	C,4	TP21	C,3
R205	C,1	R429	B,4	R521	A,3	R566	A,3	R717	D,4	TP22	A,3
R206	C,1	R430	C,3	R522	B,4	R567	A,3	R718	E,4	TP23	A,3

A3 Component Coordinates (3 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
TP24	C,3	U35	C,2						
TP25	C,3	U36	D,2						
TP26	C,2	U37	E,2						
TP27	C,2	U38	C,2						
TP28	C,2	U39	C,2						
TP29	C,2	U40	D,2						
TP30	C,1	U41	C,2						
TP31	C,1	U42	C,2						
TP32	D,1	U43	C,2						
TP33	E,1	U44	C,2						
		U45	D,2						
U1	A,4	U46	C,1						
U2	B,4	U47	C,1						
U3	C,4	U48	D,1						
U4	D,4	U49	C,1						
U5	D,4	U50	C,1						
U6	C,4	U51	C,1						
U7	B,4	U52	D,1						
U8	C,4	U53	E,1						
U9	A,4	U54	C,1						
U10	D,4	U55	C,1						
U11	D,4								
U12	E,3	VR300	C,3						
U13	B,3	VR400	B,4						
U14	B,3	VR401	C,4						
U15	E,3	VR500	A,3						
U16	E,3	VR601	B,3						
U17	C,3								
U18	D,3	W1	B,3						
U19	E,3	W2	C,3						
U20	E,3	W3	A,3						
U21	A,3	W4	B,3						
U22	B,3	W5	A,3						
U23	D,3	W6	A,2						
U24	D,3	W7	D,1						
U25	E,3	W8	C,1						
U26	E,3	W9	C,4						
U27	B,3	W10	C,4						
U28	C,3	W11	B,4						
U29	D,3								
U30	D,3	Y1	E,2						
U31	E,3	Y300	C,2						
U32	E,3								
U33	B,3								
U34	B,3								

P/O A3 LOW FREQUENCY LOOP ASSEMBLY (08657-60110)

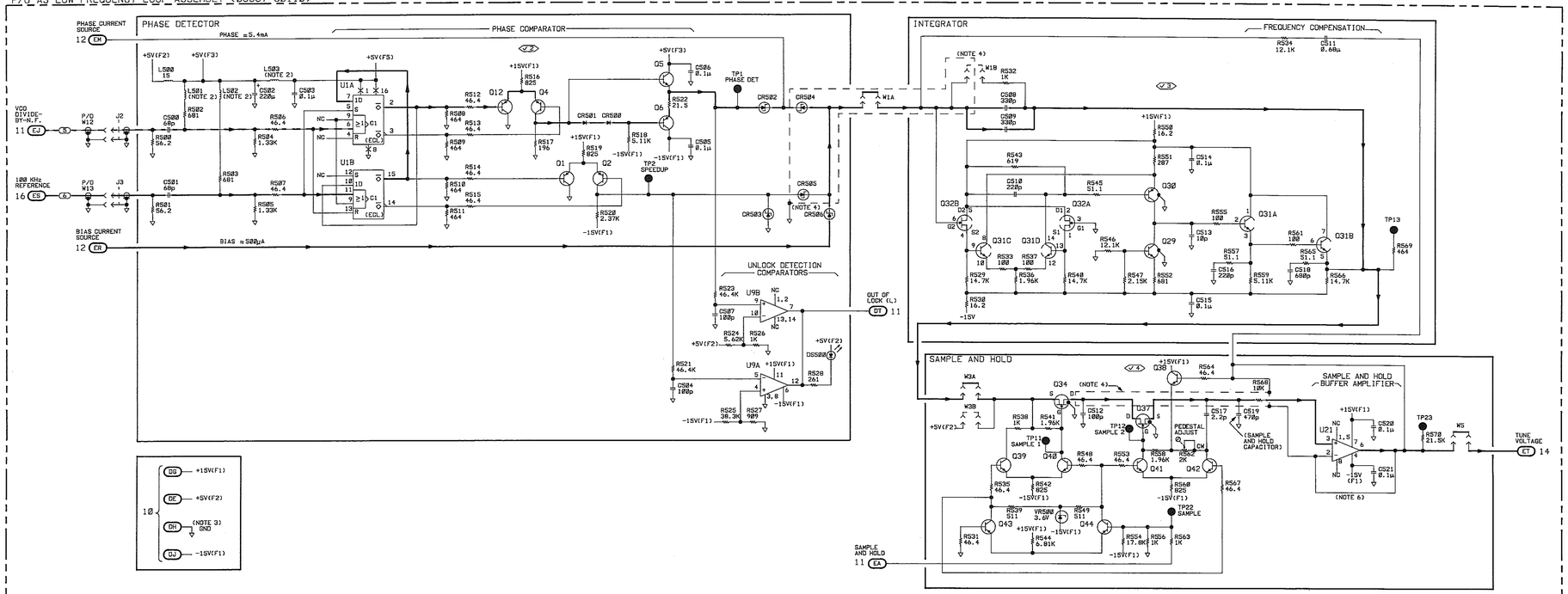


Figure 11
Service Sheet 13 17

SERIAL PREFIX: 2846J

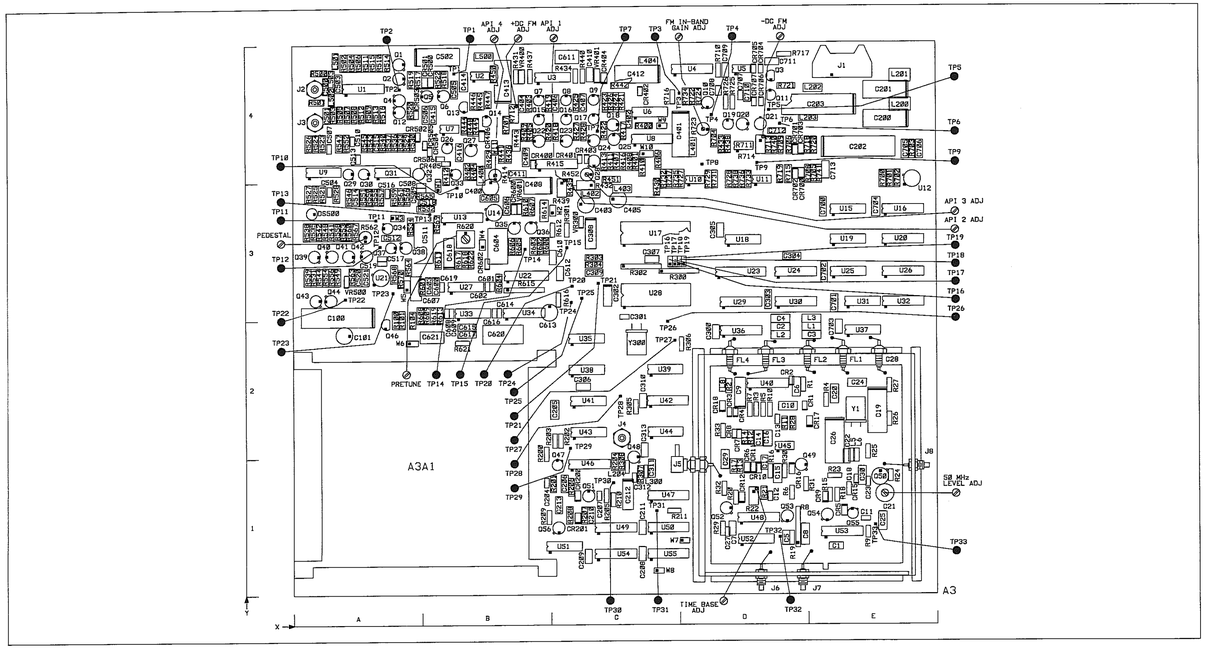


Figure Ø. Service Sheet 14 Information

Component Locator

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Chassis ground is achieved by mechanical contact through nuts holding PC board to cover and W4.
3. Isolation (guard) trace.
4. Reference designations on this service sheet C, CR, L, R and VR have numbers ranging from 600 to 699 only.

LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
	IS MORE NEG. THAN	
	IS MORE POS. THAN	
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

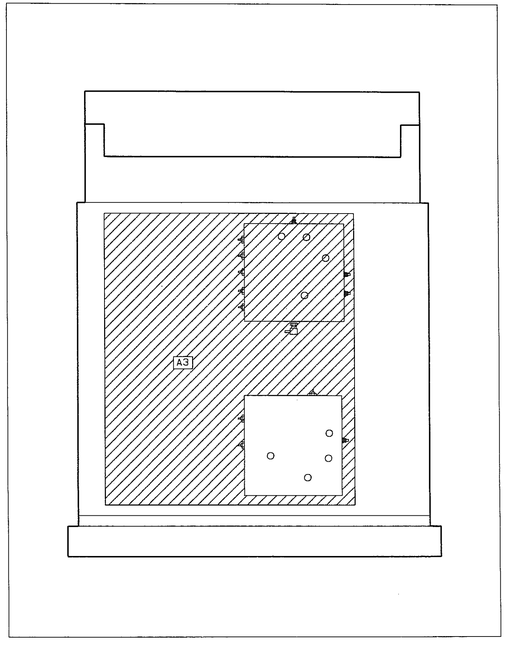
A3U14
TOP VIEW

A3Q35
TOP VIEW

P/O A3
SEE REVERSE SIDE

LOW FREQUENCY LOOP PHASE DETECTOR, INTEGRATOR, AND SAMPLE AND HOLD

SS13



Service Sheet 14

LOW FREQUENCY LOOP FREQUENCY MODULATION CALIBRATION

PRINCIPLES OF OPERATION

General

The voltage-to-frequency conversion of the Low Frequency Loop's VCO is dependent upon its output frequency. The purpose of FM Calibration is to make the VCO gain seen by the Low Frequency Loop appear constant. To guarantee calibrated frequency modulation at all frequencies, the loop must compensate for the VCO's nonlinear gain. The VCO Tune Voltage, and the Frequency Modulation signal are summed together at the FM Summing Amplifier U33A. The Low Frequency Loop adjusts the level of the inputs to the VCO by setting the bits of the FM Calibration DAC. The adjusted level at the output of the Current-To-Voltage Converter is the level required to lock the VCO at the correct frequency, and to have calibrated frequency modulation. An FM calibration is performed and the FM Calibration DAC is set each time the Low Frequency Loop VCO's frequency crosses a predetermined boundary, every 200 kHz.

When the Signal Generator's RF output frequency is changed, and the VCO's frequency crosses a 200 kHz boundary, the Low Frequency Loop data is latched into the Latches (refer to Service Sheet 11). The Low Frequency Loop's Microprocessor sets the Add Cycle input to the Prescaler high, divide-by-9. The loop adds two cycles and the frequency of the VCO is offset 200 kHz, F-200 kHz. The FM Calibration circuits store the Tune Voltage on capacitor C604. Immediately after the Tune Voltage is sampled, the Add Cycle input to the Prescaler is set low and the VCO returns to the frequency it was set to before the 200 kHz offset. The Tune Voltage difference between the 200 kHz offset, and the correct VCO frequency is detected by capacitor C604. The difference of the two tune voltages is input to the Analog-To-Digital Converter U22. The analog input voltage and the internal reference voltage determines the digital data, and stores the data in its DAC. The digital output sets the gain of the FM Calibration DAC U34 from 0.46 to 0.97.

The Offset Current circuits sums in an offset voltage at the output of the FM Calibration DAC U34. The Offset Voltage reduces the voltage required at the input of the DAC to tune the Low Frequency Loop VCO over its frequency range of 60 MHz to 110 MHz.

FM Summing, D to A Conversion

The Low Frequency Loop VCO's Tune Voltage is filtered by the 5 kHz Low Pass Filter, R608 and C607, and is connected through input resistor R609 to the input of the FM Summing Amplifier U33A at pin 1. The 5 kHz Low Pass Filter filters digital noise. The frequency modulation signal is summed at the input of U33A with the VCO's dc Tune Voltage. When frequency modulation is selected at the front-panel or over the HP-IB, the two inputs are summed together. When FM is not selected, the FM Enable input from the microprocessor is set high and switches U13A and U13D are both off. When Frequency Modulation is selected the FM Enable input at pin 1 of U13A and pin 16 of U13D is low. The two switches are closed and the frequency modulation input is summed with the VCO Tune Voltage. Tune Voltage gain of the FM Summing Amplifier is approximately 1.5, and FM signal gain is approximately 0.68. The VCO Tune Voltage is applied to the Vref input at pin 15 of the FM Calibration DAC U34. The bits of the DAC are set during the FM Calibration cycle. The Tune Voltage input is attenuated by the DAC and is dependent on the DAC bits set. The output current of the DAC at pin 1 is converted to a voltage by the Current-To-Voltage Converter U33B. The Tune Voltage output of U33B at pin 10 is applied to the Lag-Lead circuit of R619, R621, C620 and C621 to attenuate the DAC and amplifier noise by 33 dB. The output tunes the Low Frequency Loop VCO to the correct frequency, corrects for phase errors, and frequency modulates the VCO when FM is enabled. The VCO Tune Voltage is also applied to Inverting Amplifier U27B for FM Calibration.

FM Calibration

FM Calibration compensates for the non-linearity of the VCO's varactor diode. The varactor diode changes the frequency of the VCO a different amount for a fixed change in tune voltage as the VCO is tuned over its frequency range. The FM Calibration cycle sets the VCO's gain by setting the bits of the FM Calibration DAC. The VCO gain seen by the Low Frequency Loop appears constant over its frequency range of 60 MHz to 110 MHz. The FM Calibration Cycle is initiated each time the frequency of the Low Frequency Loop VCO crosses a predetermined boundary of 200 kHz.

During the FM Calibration cycle, the following sequence of events occur controlled by the Low Frequency Loop Microprocessor. Figure 1 shows the timing diagram of the FM Calibration cycle.

At time T1, the Low Frequency Loop Microprocessor U28 (shown on Service Sheet 11), sets the DCFM bit high. DCFM is enabled.

At time T2, the FM Enable bit is set high. If frequency modulation was enabled, it is disabled. The output of the Current-To-Voltage Converter U33B is always connected through resistor R601 to the input of of the Inverting Amplifier U27B at pin 7. The FM Calibration bit from the Microprocessor sets the add cycle bit high. The Low Frequency Loop VCO's frequency is offset by 200 kHz. The S(L)/H1 is set low and the base voltage of Q36 is changed to approximately −0.7V divided from the −15 Vdc supply voltage to the low input by resistors R602 and R603. Q36 is biased on and FET switch Q35's gate voltage is approximately 0.0V turning Q35 on. The offset VCO Tune Voltage is stored on capacitor C604. The B+C(L) bit is set high. The high input at pin 11 of the Analog-To-Digital Converter blanks and opens its outputs, and readies U22 for the next analog to digital conversion. With the digital output of U22 tri-stated (open), the data input to the FM Calibration DAC is determined by the pull up resistors of R615 to +5 Vdc and pull down resistor R616 to ground. The FM Calibration DAC bits 0 through 6 and 8 are high and bit 7 is low. The FM Calibration DAC U34 is set at 0.75 of its maximum value of 1.0 or 191/256.

By time T3, the frequency of the Low Frequency Loop's VCO has settled to a frequency of F-200 kHz. The 200 kHz offset is the result of the active Add Cycle high input to the Prescaler to divide its input by nine. The S(L)/H1 bit is set high by the Low Frequency Loop Microprocessor and the voltage at the base of Q36 changes to approximately +1.4V. Q36 is biased off and the gate voltage of FET switch Q35 changes to approximately −12.0 Vdc divided from −15 Vdc to ground by resistors R605 and R606. Q35 is turned off, opened. The tune voltage for the VCO frequency of F-200 kHz is stored on capacitor C604.

At time T4, the FM Calibration add cycle bit is reset low, and the Prescaler divides-by-10. The frequency of the VCO moves to and settles at frequency F. The VCO Tune Voltage has changed by the amount that was required to offset the VCO's frequency by 200 kHz. The change in the Tune Voltage is detected by capacitor C604 and applied through the Tune Voltage Step Amplifier U14 to the analog input at pin 13 of Analog-To-Digital Converter U22. With the FET switch Q35 open, the output of capacitor C604 is connected to a high impedance, and any change at the input is a change at the output. The voltage across the capacitor must remain constant. There is not a current path for C604 with Q35 open.

At time T5, the voltage at the output of capacitor C604 is amplified by the Tune Voltage Step Amplifier U14 and applied to the analog input at pin 13 of the Analog-To-Digital Converter.

Diode CR600 and Zener Diode VR601 prevent the analog input at pin 13 of the Analog-To-Digital Converter from going below approximately +3V. If the input was allowed to go to 0V, the bits to the the FM Calibration DAC could all be set to 0. The DAC would be set for maximum attenuation and the loop would not lock.

At time T6, the B+C(L) bit is reset low. On the high to low transition, the Analog-To-Digital Converter U22 starts a new conversion. The Analog-To-Digital Converter is an 8-bit successive approximation A/D Converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register, and output buffers. The Analog-To-Digital Converter's internal reference voltage is compared to the analog input voltage by the internal successive approximation register to set the bits of the internal DAC. The bits latched in the internal DAC are the inputs for the FM

Calibration DAC. The output is dependent upon the analog input. With the offset control input at pin 15 of U22 connected to ground, U22 is operating in the unipolar mode. The A/D's input voltage range is 0.0 Vdc to +10.0 Vdc. The time required for an A to D conversion by U22 is 40 μs.

At time T7, the FM Enable bit is returned to the state it was at before the FM Calibration cycle was initiated. As shown in the FM Calibration Timing Diagram Figure 1, the FM Enable bit is set low. Frequency modulation is enabled.

At time T8, the DCFM bit is returned to the state it was at before the FM Calibration cycle was initiated. As shown in the FM Calibration Timing Diagram Figure 1, the DCFM bit is set low. DCFM is disabled. The FM Calibration cycle is complete.

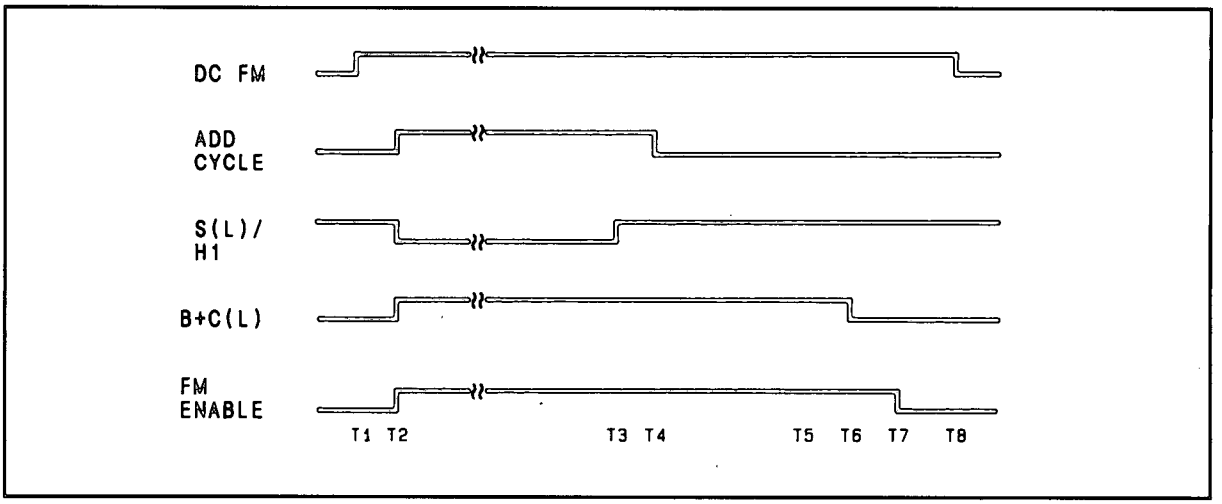


Figure 1. FM Calibration Timing Diagram.

Offset Current

The Low Frequency Loop VCO has the maximum Hz/Volt tuning sensitivity at 60 MHz. This requires that the FM Calibration DAC setting be 0.5 of its range. The VCO tuning voltage for 60 MHz is approximately +9.0V. With the DAC set at 0.5, the voltage input to the DAC would have to be +18.0V. The +18.0V is greater than the possible output voltage swing of the circuit's operational amplifier. The Offset Current circuit compensate for this problem by summing in an offset voltage proportional to the VCO's frequency at the input of the Current-To-Voltage Converter U33B. The D1 bit from the 10 MHz counter's latch is used to determine if 6V is summed at the input of U33B. The bit determines if diode CR602 is turned on or off. When the diode is off, D1 data bit at pin 9 of U13C is low and the switch is closed. The +5 Vdc at pin 10 of U13C is switched through the switch to bias diode CR602 off. When the D1 data bit is high, the diode is on and an offset voltage is summed into the input of U33B. Data bit D1 controls CR602 and when D1 is high, CR602 is biased on and current through R622 sums 6V offset into the input of U33B. When the VCO frequency is 60 MHz, the D1 data bit is high. Diode CR602 is biased on and a 6V offset is summed into the input of U33B. The 6V offset voltage is summed with the output of the FM Calibration DAC. The VCO Tune Voltage for a VCO output frequency of 60 MHz is approximately +9V. The gain of the DAC is set at 0.46, and the DAC input voltage is −8.0 V. The DAC gain and input voltage will vary because of the Low Frequency Loop FM calibration. The offset voltage summed into the input of U33B varies from +6V to 0V as the VCO is tuned across its frequency range. The offset voltage is 6V for VCO frequencies from 60 MHz to 84 MHz, and 0V for 84 MHz to 110 MHz.

TROUBLESHOOTING

Procedures for checking part of the A3 Low Frequency Loop Assembly circuits are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, for example, ⟨✓3⟩

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Digital Multimeter	HP 3466A
Oscilloscope	HP 54100A
Oscilloscope 1 Megohm Probe Pod Chan 2	HP 54003A
Oscilloscope Probe	HP 54003-61617
Audio Source	HP 8903B

⟨✓1⟩FM Summing

1. Remove jumper W3 from the W3A position, and install it in the W3B position (refer to Service Sheet 13). Remove jumper W6 from the A3 Assembly. +5 Vdc is connected to the input of the Sample and Hold circuits by W3. When the Sample and Hold circuits are working correctly, +5 Vdc is input to the FM Summing Amplifier.
2. Set the Oscilloscope as follows:

Chan 1

Ch 1 Display	Off

Chan 2

Ch 2 Mode	Normal
Ch 2 Display	On
VOLTS/DIV	5.0V
OFFSET	0V

Timebase

SEC/DIV	500 ns
DELAY	0.0s
Delay Ref at	Left
Sweep	Auto

Trigger

Trigger Mode	Edge
Trig Src	Chan 2
TRIG LEVEL	0.0V
Slope	Pos

Display

Display Mode	Normal
DISPLAY TIME	200 ms
Split Screen	Off
Graticle	Grid

3. Connect Chan 2 to pin 12 of U33A. If the amplifier is operating correctly, the output voltage of U33A is approximately −6.8V.
4. Set the Signal Generator as follows:
   Frequency ..... Any Frequency
   Amplitude ..... Any Amplitude
   Modulation ..... FM 50 kHz
   Source ..... 1 kHz (Int.)
5. Set the oscilloscope's Chan 2 OFFSET to −5.0 V.
6. Connect Chan 2 to pin 12 of U33A. Check the oscilloscope for a 1 kHz signal of approximately 0.2 Vpp.
7. If a modulation signal is not present, check the Out-Of-Band FM Input switches by inserting a 1 kHz, 10 mV signal at hard-wired jumper W11.

⟨J2⟩ D to A Conversion

1. With jumper W3 in the W3B position as for ⟨J1⟩ remove jumper W2 the B+C(L) input to U22, and remove jumper W4 the offset input to U33B. With the outputs of U22 open, the input to the FM Calibration DAC U34 is determined by resistors R615 and R616.
2. Set the digital multimeter function to dc and Range to Auto.
3. Connect the digital multimeter to jumper W6 at the output of U33B.
4. Ground the inputs of the FM Calibration DAC at pins 4, 6, 7, 8, 9, 10 and 11, and connect pin 5 to +5 Vdc one at a time. The dc voltage level on the digital multimeter will changes as each pin 4, 6, 7, 8, 9, 10 and 11 are connected to ground, and as pin 5 is connected to +5 Vdc.

NOTE

When the least significant bits are grounded, the voltage change is only a few millivolts.

5. Reinstall the jumpers W2, W3, and W4 (put W3 in the W3A position).

⟨J3⟩ FM Calibration

1. The FM Calibration circuits are checked by placing the Low Frequency Loop in the repeatable FM Cal mode. An FM Calibration is performed every 100 ms.
2. With the instrument ON, connect TP26 to ground (refer to Service Sheet 11). Increment the Signal Generator's frequency by 10 MHz. The Signal Generator will then be in the repeatable FM Cal mode.
3. Remove jumper W6 and connect a 100 Hz, 200 mV peak signal to the input of U27B at pin 7. This connection can be made at the socket of jumper W6, VCO Tune input.
4. The 100 Hz input causes the input to the Analog-To-Digital Converter to change, and the output bits to change.

5. Set the oscilloscope as follows:

Chan 1

Ch 1 Mode ..... Normal
Ch 1 Display ..... Off
VOLTS/DIV 2.0V
OFFSET 0.0V

Chan 2

Ch 2 Mode ..... Normal
Ch 2 Display ..... On
VOLTS/DIV 2.0V
OFFSET 0.0V

Timebase

SEC/DIV ..... 50 ms
DELAY 0.0s
Delay Ref at ..... Left
Sweep ..... Trg'd

Trigger

Trigger Mode ..... Edge
Trig Src ..... Chan 2
TRIG LEVEL 1.0V
Slope ..... Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 200 ms
Split Screen ..... Off
Graticle ..... Grid

6. Check the S(L)/H1 and B+C(L) inputs. Pulses are TTL level and at every 100 ms.
7. Check that Q36 is pulsed on and off and that the Gate voltage of Q35 is switched from approximately 0V to approximately −15V. Q35 is gated on and off.
8. Connect Chan 2 to W2, B+C(L), input. Set Chan 1 Display On and connect it to TP14. The signal at TP14 is randomly pulsed high when the B+C(L) input is low.
9. Connect Chan 2 to the output of the Analog-To-Digital Converter (U22) at pins 2 through 9. The output bits randomly change when the B+C(L) input is low. The Analog-To-Digital Converter does a conversion.
10. Remove the ground from TP26. Re-install W6, and turn the Signal Generator to STBY, and back to ON to exit the FM Cal mode.

◇4◇ Offset Current

1. Remove jumper W1 from the W1A position, and install W1 in the W1B position (refer to Service Sheet 13).
2. Jumper W4 must be installed.
3. The voltage input to the FM Calibration DAC at pin 15 is 0.0V. The output of the Current-To-Voltage Converter is the offset voltage from the Offset Current as the Signal Generator's frequency is changed.
4. Set the Signal Generator as follows:
   a. Frequency to 45 MHz
5. If the offset voltages shown in Table 1 for W6 (pin 1), at the input of U33B, are correct the voltages for U13 are correct. Change the Signal Generator's frequency as indicated in Table 1 and measure the voltage levels as indicated.

Table 1. Input and Output Voltage of Offset Circuits.

Signal Generator Frequency (MHz)	U13 and W6 with W4 Installed		
	Pin 9	Pin 11	W6 Pin 1
45	0	+5	0
70	+5	0	+6

A3 Component Coordinates (1 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	E,1	C213	C,1	C513	A,4	CR1	D,2	FL1	E,2	Q10	D,4
C2	D,2	C300	D,2	C514	A,3	CR2	D,2	FL2	E,2	Q11	D,4
C3	E,2	C301	C,3	C515	A,4	CR3	D,2	FL3	D,2	Q12	A,4
C4	D,2	C302	C,3	C516	A,3	CR4	D,2	FL4	D,2	Q13	B,4
C5	D,1	C303	D,3	C517	A,3	CR5	E,1			Q14	B,4
C6	D,2	C304	D,3	C518	B,3	CR6	D,1	J1	E,4	Q15	B,4
C7	D,1	C305	D,3	C519	A,3	CR7	D,2	J2	A,4	Q16	C,4
C8	D,1	C306	C,2	C520	A,3	CR8	D,2	J3	A,4	Q17	C,4
C9	D,2	C307	C,3	C521	A,3	CR9	E,1	J4	C,2	Q18	C,4
C10	D,2	C308	C,3	C600	B,3	CR10	D,1	J5	C,1	Q19	D,4
C11	E,1	C309	C,3	C601	B,3	CR11	D,1	J6	D,1	Q20	D,4
C12	D,1	C310	C,2	C602	B,3	CR12	D,1	J7	E,1	Q21	D,4
C13	D,2	C311	C,1	C603	B,3	CR15	E,1	J8	E,2	Q22	B,4
C14	D,2	C312	C,1	C604	B,3	CR16	D,1			Q23	C,4
C15	D,1	C313	C,2	C605	B,3	CR17	E,2	L1	E,2	Q24	C,4
C16	D,2	C400	B,3	C606	B,3	CR18	D,2	L2	D,2	Q25	C,4
C17	D,1	C401	D,4	C607	B,3	CR200	C,1	L3	E,2	Q26	B,4
C18	E,1	C402	C,4	C608	B,3	CR201	C,1	L5	E,2	Q27	B,4
C19	E,2	C403	C,3	C609	B,3	CR400	B,4	L6	E,2	Q28	C,4
C20	E,2	C404	B,4	C610	C,3	CR401	C,4	L8	D,2	Q29	A,4
C21	E,1	C405	C,3	C611	C,4	CR402	C,4	L200	E,4	Q30	A,4
C22	E,2	C406	C,4	C612	C,3	CR403	C,4	L201	E,4	Q31	A,4
C23	E,1	C407	C,4	C613	B,3	CR404	C,4	L202	E,4	Q32	A,4
C24	E,2	C408	B,3	C614	B,3	CR405	B,4	L203	E,4	Q33	B,4
C25	E,1	C409	B,4	C615	B,2	CR406	B,4	L204	C,1	Q34	A,3
C26	E,2	C410	C,4	C616	B,3	CR500	B,4	L300	C,1	Q35	B,3
C27	D,1	C411	B,4	C617	B,2	CR501	B,4	L400	B,4	Q36	B,3
C28	E,2	C412	C,4	C618	B,3	CR502	A,4	L401	D,4	Q37	A,3
C29	D,1	C413	B,4	C619	B,3	CR503	A,4	L402	C,3	Q38	A,3
C30	E,1	C414	B,4	C620	B,2	CR504	B,4	L403	C,3	Q39	A,3
C100	A,3	C415	B,4	C621	B,2	CR505	B,4	L404	C,4	Q40	A,3
C101	A,2	C416	B,4	C700	E,3	CR506	B,4	L500	B,4	Q41	A,3
C200	E,4	C500	A,4	C701	E,3	CR600	B,3	L501	A,4	Q42	A,3
C201	E,4	C501	A,4	C702	E,3	CR602	B,3	L502	A,4	Q43	A,3
C202	E,4	C502	B,4	C703	E,2	CR700	D,4	L503	A,4	Q44	A,3
C203	E,4	C503	A,4	C704	E,3	CR701	D,4			Q46	A,2
C204	B,1	C504	A,3	C705	E,4	CR702	D,4	Q1	A,4	Q47	C,1
C205	C,2	C505	B,4	C706	E,4	CR703	D,4	Q2	A,4	Q48	C,2
C206	C,1	C506	B,4	C707	D,4	CR704	D,4	Q3	D,4	Q49	D,1
C207	C,1	C507	A,4	C708	D,4	CR705	D,4	Q4	A,4	Q50	E,1
C208	C,1	C508	B,3	C709	D,4	CR706	D,4	Q5	B,4	Q51	C,1
C209	C,1	C509	B,3	C710	D,4	CR707	D,4	Q6	B,4	Q52	D,1
C210	C,1	C510	A,4	C711	D,4			Q7	B,4	Q53	D,1
C211	C,1	C511	B,3	C712	D,4			Q8	C,4	Q54	E,1
C212	C,1	C512	A,3	C713	E,4	DS500	A,3	Q9	C,4	Q55	E,1

A3 Component Coordinates (2 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
Q56	C,1	R207	C,1	R431	B,4	R523	A,4	R568	A,3	R719	D,4
		R208	C,1	R432	C,3	R524	A,4	R569	B,3	R720	E,4
R1	D,2	R209	B,1	R433	D,4	R525	A,3	R570	A,3	R721	D,4
R2	D,2	R210	C,1	R434	C,4	R526	A,4	R600	B,3	R722	D,4
R3	D,2	R211	C,1	R435	C,3	R527	A,3	R601	B,3	R723	D,4
R4	E,2	R300	C,3	R436	B,4	R528	A,3	R602	B,3	R724	D,4
R5	D,2	R301	C,3	R437	B,4	R529	A,4	R603	B,3	R725	D,4
R6	D,1	R302	C,3	R438	D,4	R530	A,4	R604	B,3	R726	D,4
R7	D,2	R303	C,3	R439	C,3	R531	A,3	R605	B,3	R727	D,4
R8	D,1	R304	C,3	R440	C,4	R532	B,3	R606	B,3	R728	D,4
R9	E,1	R305	C,2	R441	B,4	R533	A,4	R607	B,3	R729	D,4
R10	D,2	R306	D,2	R442	C,4	R534	A,3	R608	A,3	R731	D,4
R11	D,2	R307	C,1	R443	B,4	R535	A,3	R609	B,3	R732	C,4
R12	D,2	R308	C,1	R444	B,4	R536	A,4	R610	B,3	R733	D,4
R13	D,1	R400	C,4	R445	B,4	R537	A,4	R611	B,3	R734	D,4
R14	D,2	R401	C,4	R446	B,4	R538	A,3	R612	C,3	R735	C,4
R15	E,1	R402	B,4	R447	B,4	R539	A,3	R613	B,3	R736	D,4
R16	D,1	R403	B,4	R448	B,4	R540	A,4	R614	B,3	R737	C,4
R17	D,1	R404	B,4	R449	B,4	R541	A,3	R615	B,3	R738	D,4
R18	E,1	R405	B,4	R450	B,4	R542	A,3	R616	C,3	R740	D,4
R19	D,1	R406	C,4	R451	C,4	R543	A,4	R617	B,3	R741	E,4
R20	D,1	R407	C,4	R452	C,4	R544	A,3	R618	B,3		
R21	D,1	R408	C,4	R500	A,4	R545	A,4	R619	B,3	TP1	B,4
R22	D,1	R409	B,4	R501	A,4	R546	A,3	R620	B,3	TP2	A,4
R23	E,1	R410	C,4	R502	A,4	R547	A,4	R621	B,2	TP3	D,4
R24	E,1	R411	C,4	R503	A,4	R548	A,3	R622	B,3	TP4	D,4
R25	E,2	R412	B,4	R504	A,4	R549	A,3	R700	E,4	TP5	D,4
R26	E,2	R413	C,4	R505	A,4	R550	A,3	R701	E,4	TP6	D,4
R27	E,2	R414	B,4	R506	A,4	R551	A,3	R702	E,4	TP7	C,4
R28	D,2	R415	C,4	R507	A,4	R552	A,4	R703	E,4	TP8	D,4
R29	D,1	R416	C,4	R508	A,4	R553	A,3	R704	D,4	TP9	D,4
R30	D,1	R417	C,4	R509	A,4	R554	A,3	R705	E,4	TP10	B,3
R31	D,1	R418	C,4	R510	A,4	R555	A,3	R706	D,4	TP11	A,3
R32	D,1	R419	B,4	R511	A,4	R556	A,3	R707	B,4	TP12	A,3
R33	D,2	R420	B,4	R512	A,4	R557	A,3	R708	E,4	TP13	B,3
R100	A,2	R421	C,4	R513	A,4	R558	A,3	R709	D,4	TP14	B,3
R101	A,2	R422	C,4	R514	A,4	R559	A,3	R710	D,4	TP15	C,3
R104	A,2	R423	C,4	R515	A,4	R560	A,3	R711	D,4	TP16	C,3
R200	B,2	R424	C,4	R516	A,4	R561	A,3	R712	B,4	TP17	C,3
R201	C,1	R425	C,4	R517	A,4	R562	A,3	R713	D,4	TP18	D,3
R202	C,2	R426	C,4	R518	B,4	R563	A,3	R714	D,4	TP19	D,3
R203	C,2	R427	C,4	R519	A,4	R564	A,3	R715	D,4	TP20	C,3
R204	C,1	R428	C,4	R520	A,4	R565	B,3	R716	C,4	TP21	C,3
R205	C,1	R429	B,4	R521	A,3	R566	A,3	R717	D,4	TP22	A,3
R206	C,1	R430	C,3	R522	B,4	R567	A,3	R718	E,4	TP23	A,3

A3 Component Coordinates (3 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
TP24	C,3	U35	C,2						
TP25	C,3	U36	D,2						
TP26	C,2	U37	E,2						
TP27	C,2	U38	C,2						
TP28	C,2	U39	C,2						
TP29	C,2	U40	D,2						
TP30	C,1	U41	C,2						
TP31	C,1	U42	C,2						
TP32	D,1	U43	C,2						
TP33	E,1	U44	C,2						
		U45	D,2						
U1	A,4	U46	C,1						
U2	B,4	U47	C,1						
U3	C,4	U48	D,1						
U4	D,4	U49	C,1						
U5	D,4	U50	C,1						
U6	C,4	U51	C,1						
U7	B,4	U52	D,1						
U8	C,4	U53	E,1						
U9	A,4	U54	C,1						
U10	D,4	U55	C,1						
U11	D,4								
U12	E,3	VR300	C,3						
U13	B,3	VR400	B,4						
U14	B,3	VR401	C,4						
U15	E,3	VR500	A,3						
U16	E,3	VR601	B,3						
U17	C,3								
U18	D,3	W1	B,3						
U19	E,3	W2	C,3						
U20	E,3	W3	A,3						
U21	A,3	W4	B,3						
U22	B,3	W5	A,3						
U23	D,3	W6	A,2						
U24	D,3	W7	D,1						
U25	E,3	W8	C,1						
U26	E,3	W9	C,4						
U27	B,3	W10	C,4						
U28	C,3	W11	B,4						
U29	D,3								
U30	D,3	Y1	E,2						
U31	E,3	Y300	C,2						
U32	E,3								
U33	B,3								
U34	B,3								

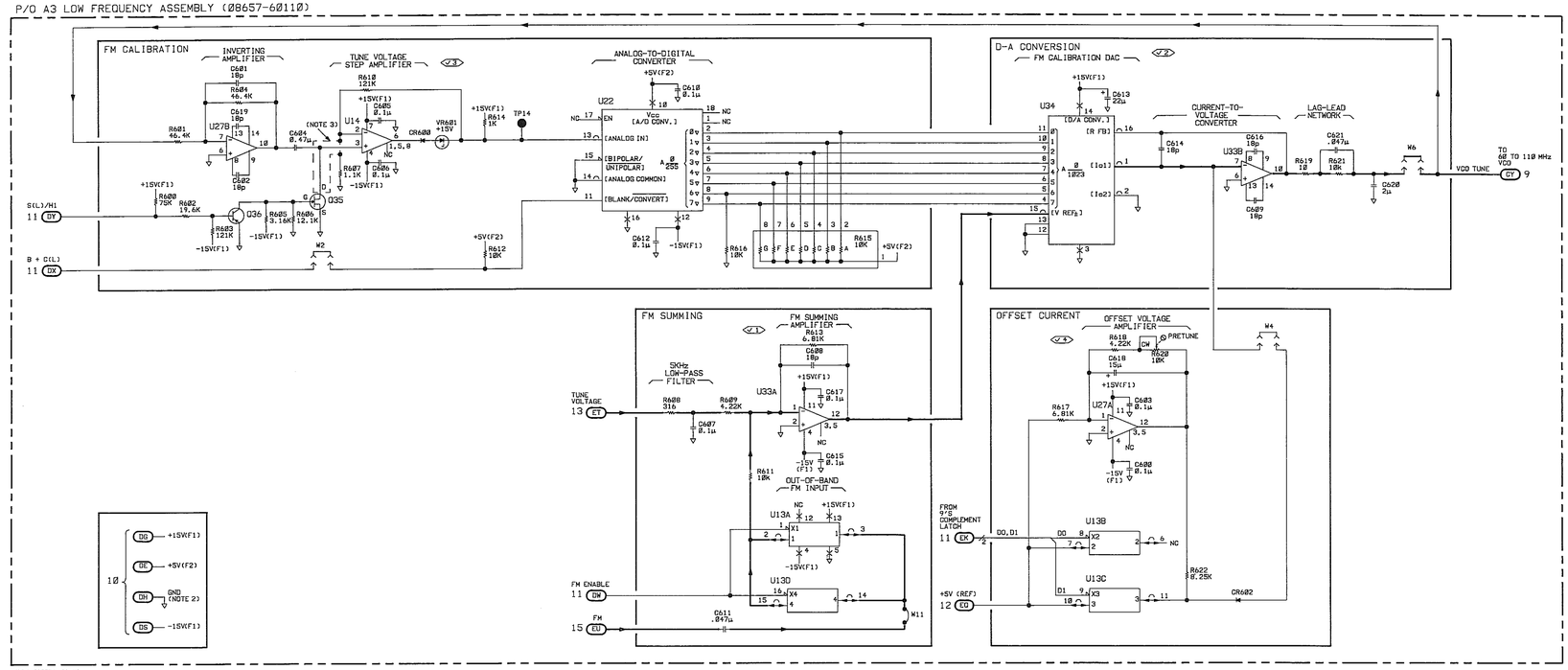


Figure 2
Service Sheet 14 13

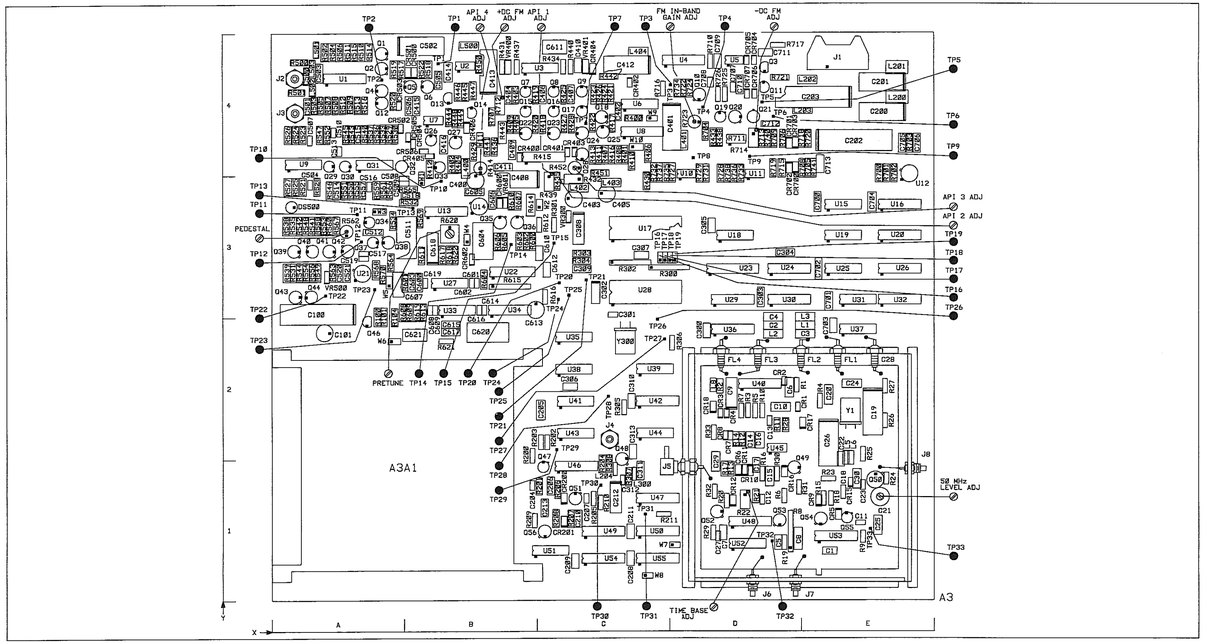


Figure Ø. Service Sheet 15 Information

Component Locator

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Isolation (guard) trace.
3. Chassis ground is achieved by mechanical contact through nuts holding PC board to cover and W4.
4. Reference designations on this service sheet C, CR, Q, R and U have numbers ranging from 7ØØ to 799 only.

LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
	IS MORE NEG. THAN	
	IS MORE POS. THAN	
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

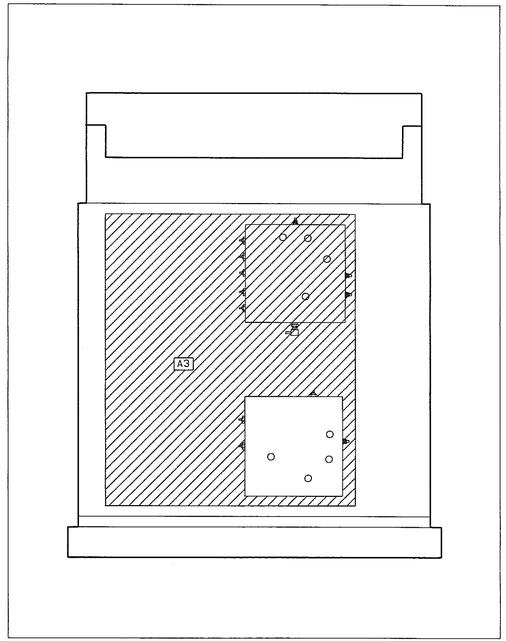
A3021 TOP VIEW

A3U5, 10-12 TOP VIEW

P/O A3 LOW FREQUENCY LOOP FREQUENCY MODUALTION CALIBRATION

SEE REVERSE SIDE

SS14



Service Sheet 15

LOW FREQUENCY LOOP IN-BAND FREQUENCY MODULATION

PRINCIPLES OF OPERATION

General

Phase detector range, integrator range, and phase lock loop bandwidth are limitations of frequency modulation in a phase lock loop. These limitations are overcome with the addition of circuits to add a cycle and remove a cycle of the Low Frequency Loop's VCO frequency at the Prescaler, and to precisely reset the Integrator (refer to Service Sheet 13). The FM input is applied to Integrator U5. When the output of Integrator U5 crosses the high threshold, +1V, the High Threshold Comparator is set and a Remove Cycle control pulse is generated. The Remove Cycle control pulse is gated to the Prescaler, and a cycle is removed from the VCO Divided-By-N.F. signal. When the output of the integrator crosses the low threshold, −4V, the Low Threshold Comparator is set and an Add Cycle control pulse is generated. The Add Cycle control pulse is gated to the Prescaler, and a cycle is added to the VCO Divided-By-N.F. signal. When a cycle is removed or added, a precise current is directed to the FM Integrator U5. Just enough charge is added to or removed from the Integrator to offset the 360 degrees of phase caused by adding or removing a cycle by the Prescaler.

The FM section operates in a sampled mode. At the time each sample is taken the effects of the Remove Cycle or Add Cycle and the resetting of the integrator have settled. When DC FM is selected and a dc voltage is applied to the MOD INPUT/OUTPUT connector, the dc voltage offsets the VCO frequency a proportional amount. The drift of Integrator U5, without feedback, offsets the VCO center frequency when a dc voltage is not present at the MOD INPUT/OUTPUT connector. With ac FM, it is desirable to frequency modulate the VCO and keep the center frequency locked to a stable reference.

To prevent integrator U5's offset currents from being translated into a frequency shift during ac FM, a feedback voltage to the integrator proportional to the phase offset of the Low Frequency Loop VCO is needed. The Up/Down Counters and DAC reconstruct a staircase voltage approximation of the total VCO phase offset caused by the frequency modulation Remove Cycle and Add Cycle control inputs to the Prescaler. This voltage is fed-back to the integrator. The resistor network of R722, R726, and R734 provides feedback to fill in the spaces between the steps.

The FM Reset Timing and Current Switches reset the Integrator. The Up/Down Counters, Phase Deviation DAC, and Current-To-Voltage Converter keep track of the number of times and the direction which Integrator U5 is reset. The High and Low Threshold Comparators determine when the Integrator is reset and when a frequency modulation remove or Add Cycle control pulse is generated. Figure 1 shows the timing diagram for square wave in-band frequency modulation.

FM Control Gates and Switches

The FM OFF instruction from the Microprocessor U28 at pin 27 (refer to Service Sheet 11), is high when FM is off. With FM selected the FM OFF input at pin 2 of NOR gate U15A is low and the output at pin 1 is high. The load input at pin 11 of the Up/Down Counters, U20, U26, and U32, is high and data at the inputs is not loaded into the Counters. The high output of U15A is also the input of U15B at pin 5 and sets the Buffered FM OFF output at pin 4 low. The low Buffered FM OFF to switch U4B at pin 8 closes the switch to connect the output of the Integrator U5 at pin 6 to the base of Q10.

The DC FM instruction from the Microprocessor U28 at pin 26 is high when DC FM is selected. When the DC FM instruction is high Up/Down Counter U20 is disabled and switch U4A is opened. When the DC FM instruction is low and DC FM is not selected, the Up/Down Counters are enabled, and switch U4A is closed.

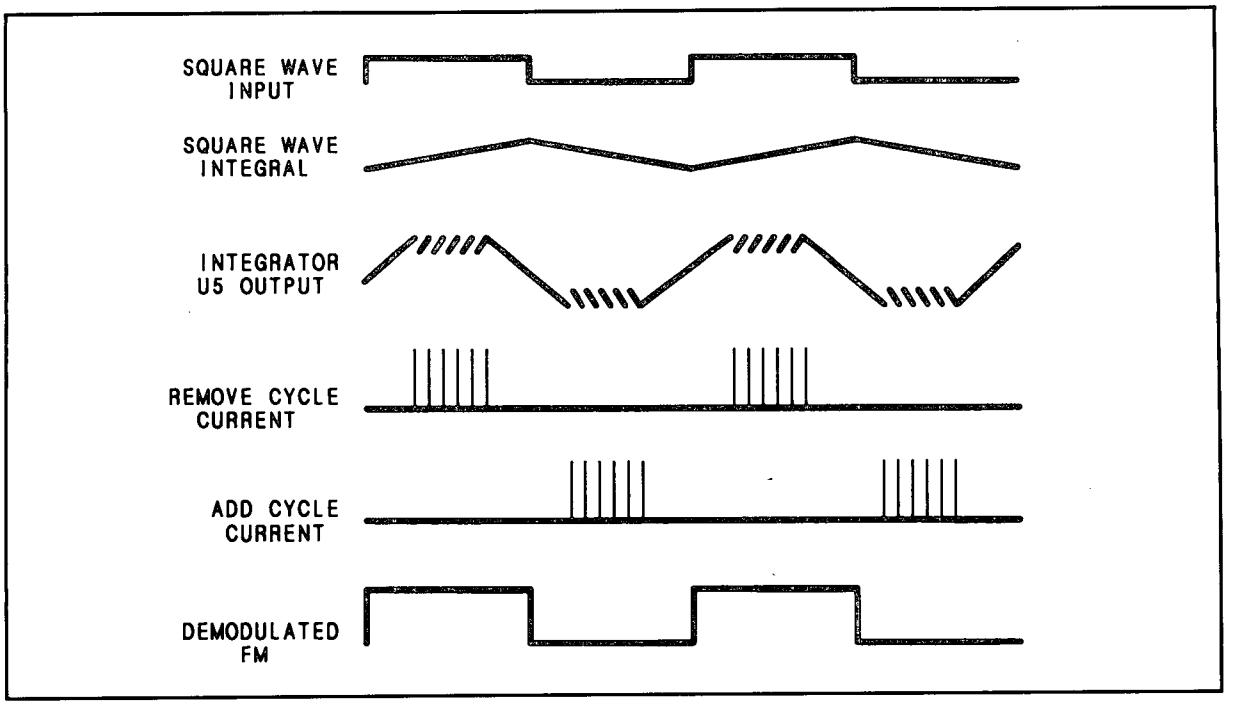


Figure 1. 10 Hz Square Wave In-Band Modulation.

Threshold Comparators

The output of Integrator U5 is applied to the input of the High and Low Threshold Comparators U10 and U11. When the integrated voltage is approximately +1V the High Threshold Comparator's output is switched from low to high. The high output is latched into the Remove Cycle flip-flop U38B (refer to Service Sheet 11). The output of U38B is gated at the correct time in each Low Frequency Loop cycle for the Prescaler to remove a cycle and to clock D flip-flop U25A on the low to high transition. When the integrated voltage is approximately −4V, the Low Threshold Comparator's output is switched from low to high. The high output is latched into the Add Cycle flip-flop U38A (refer to Service Sheet 11). The output of U38A is gated at the correct time in each Low Frequency Loop cycle for the Prescaler to add a cycle and to clock D flip-flop U25B on the low to high transition.

FM Reset Timing

The FM Reset Timing D flip-flops U31 and U37 are clocked at pins 3 and 11 by the 5 MHz Reference input, divided from the 50 MHz Reference (refer to Service Sheet 9). The 5 MHz Reference input is directed to the FM Reset Timing flip-flop's when frequency modulation is selected. The low to high transition of Remove Cycle flip-flop U38B's output at pin 9, clocks the high D input at pin 2 of U25A to the output at pin 5. The output at pin 5 is the D input for U31A, and is clocked to the output at pin 5 by the 5 MHz Reference. The output at pin 5 of U31A is the D input at pin 12 of U31B, and the high input is clocked to the output at pin 9 on the next low to high transition of the 5 MHz Reference. The output at pin 8 of U31B is clocked low, and U25A is reset (the output at pin 5 is low and output at pin 6 is high). The low output at pin 5 of U25A is clocked through U31A and U31B. The output at pin 9 of U31B was set high, and after two cycles of the 5 MHz Reference it is set low. The high output pulse width of U31B at pin 9 is 400 ns, two cycles of the 5 MHz Reference clock. U25A, U31A and U31B generate a 400 ns pulse each time a Remove Cycle control pulse is generated by the High Threshold Comparator U10. During the 400 ns pulse a precise positive current (from the API 2 current source and current mirror) resets Integrator U5. The 400 ns pulse from U31B is also one input to NOR gate U15C, and when high the output of U15C at pin 10 is low. At the termination of the 400 ns pulse, the output of U15C goes high and clocks the Up/Down

Counter U20 up one count on the low to high transition. The output of U25A at pin 6 had set the output at pin 8 of U19B low, and enabled the Up/Down Counters to count up when clocked.

The low to high transition from the output of U38A at pin 5 (refer to Service Sheet 11) clocks the high D input at pin 12 of U25B to the output at pin 9. U25B, U37A and U37B generate a precise 400 ns pulse each time an Add Cycle control pulse is generated by the Low Threshold Comparator U11. They function the same as U25A, U31A, and U31B, described above, to generate a 400 ns pulse. During the 400 ns pulse a precise negative current from the API 3 current source resets Integrator U5. The 400 ns pulse from U37B is also one input to NOR gate U15C, and when high the output of U15C at pin 10 is low. At the termination of the 400 ns pulse, the output of U15C goes high and will clock the Up/Down Counter U20 down one count on the low to high transition of the pulse. The output of U25B at pin 8 had reset the output at pin 8 of U19B high, and enabled the Up/Down Counter to count down when clocked.

Up/Down Control

The Up/Down Control, U19B, for the Up/Down Counters of U20, U26, and U32 is controlled by U25A and U25B. When U19B's output at pin 8 is set low by U25A, the Counters are enabled to count up. When U19B's output at pin 8 is reset high by U25B the Counters are enabled to count down. The D flip-flop U25A is clocked each time the High Threshold Comparator's output at pin 7 of U10 is switched high, and the Prescaler removes a cycle. U25A is clocked by the output of U38B. U19B is set and the Up/Down Counters are enabled to count up. The D flip-flop U25B is clocked each time the Low Threshold Comparator's output at pin 7 of U11 is switched high, and the Prescaler adds a cycle. U25B is clocked by the output of U38A. U19B is reset, and the Up/Down Counters are enabled to count down.

√1

Up/Down Counters

The Up/Down Counters counts up each time an FM Remove Cycle control pulse is generated, and counts down each time an FM Add Cycle control pulse is generated. The Up/Down Counters are enabled to count when the DC FM instruction from the microprocessor U28 at pin 26 is low. FM is selected but DC FM is not selected. The enable input at pin 4 of U20 enables the counter to count on each clock from U15C.

The data inputs of the Up/Down Counters are connected to +5 Vdc except bit 10 at pin 1 of U32, and it is connected to ground. The input data is loaded into Up/Down Counters each time Frequency Modulation is selected. The DAC is set to 512, one-half of its maximum value of 1024. The FM OFF instruction from the Low Frequency Loop Microprocessor U28 at pin 27 is low when FM is selected. The low FM OFF instruction is one input to NOR gate U15A at pin 2. Its other input is connected to ground and the output goes high. The input data to the counter is loaded on the low to high transition of U15A's output.

FM Deviation DAC and Current-to-Voltage Converter

Ten output bits of the Up/Down Counters set the bits of the Phase Deviation DAC U16 to 512. The input to the DAC increases when the Counters are counted up for an FM Remove Cycle, and decreases when the Counters are counted down for an FM Add Cycle. The output current of the DAC changes as the bits are changed by the Counters. The output current of the DAC controls the output voltage of the Current-To-Voltage Converter U12 from −5V to +5V. When the Counters are loaded, the DAC is set at one half of its maximum value and the output voltage is approximately 0.0V. The Current-To-Voltage Converter's voltage output is input to Integrator U5 through the resistor network of R704, R726, and R734 as a current. The current input to the Integrator represents the net number of FM Remove Cycles and Add Cycles or the amount the phase of the Low Frequency Loop VCO has been shifted for Frequency Modulation. Each time a cycle is removed or added, 360 degrees of phase, one cycle, of the VCO's frequency divided-by-2 is removed or added by the Prescaler. The Up/Down Counters keeps track of the number of cycles that have been removed or added. The output of the DAC reconstructs the remove or add voltage step to the loop Integrator of Service Sheet 13.

Current Switches

For the duration of the 400 ns pulse, initiated by a Remove Cycle control pulse from the High Threshold Comparator U10 through the Remove Cycle D flip-flop U38B and generated by U25A and U31A/B, a precise positive current is applied to the Integrator U5 to reset its output voltage. The positive 400 ns pulse biases the base of Q11 at approximately +0.3V and the emitter is then approximately +1.0V. Diode CR706 is turned off and diode CR707 is turned on. The positive current from the Current Mirror, transistors Q20 and Q21, is directed through the Integrator. The Current Mirror changes the negative API 3 current to a positive current. When the 400 ns FM Reset Pulse is not active, the bias on the base of Q11 is approximately −1.3V and the emitter is approximately −0.6V. Diode CR706 is turned on and diode CR707 is turned off. The Current is directed through transistor Q11.

For the duration of the 400 ns pulse, initiated by a Add Cycle control pulse from the Low Threshold Comparator U11 through the Add Cycle D flip-flop U38A and generated by U25B and U37A/B, a precise negative current is applied to Integrator U5 to reset its output voltage. The negative 400 ns pulse biases the base of Q3 at approximately −0.3V, and the emitter is approximately −1.0V. Diode CR704 is turned off, and diode CR705 is turned on.

Negative API 2 current is directed through the Integrator. When the 400 ns FM reset pulse is not active, the bias on the base of Q3 is approximately +1.3V and the emitter voltage is Approximately +0.6V. Diode CR704 is turned on and diode CR705 is turned off. API 2 current is directed through transistor Q3.

Integrator

When AC FM or DC FM is selected, switches U4C and D are closed. The frequency modulation signal is applied to the FM Summing Amplifier U33A (Service Sheet 14), and to Integrator U5. In a phase lock loop, frequency modulation within the loop bandwidth is canceled and phase modulation within the loop bandwidth is passed. Both properties are used in the Low Frequency Loop for flat frequency modulation by Integrator U5 converting the frequency modulation signal to phase modulation. The phase output of the Integrator is summed at the virtual +5V node of the Current Summing Amplifier U7 (refer to Service Sheet 12). Each Low Frequency Loop cycle, AC FM or DC FM selected and within the bandwidth of the Low Frequency Loop, the output of the Integrator is summed with the Bias Current and API Current to offset the VCO tune voltage phase modulating the VCO. All components of the modulation signal within the loop bandwidth phase modulate the VCO and all components outside the loop bandwidth frequency modulate the VCO. The result is continuous modulation.

The 400 ns pulses from the current switches directs a positive or negative current to reset the Integrator. The Integrator is reset during frequency modulation when its output voltage reaches the high or low threshold voltage. During the same Low Frequency Loop cycle the Integrator is reset, a cycle is removed or added by the Prescaler dependent upon the output voltage of the Integrator being at the high or low threshold. The Prescaler removes or adds a cycle, and the 400 ns of current resets the Integrator's output voltage to remove or add 2 cycles, 720 degrees, from the Low Frequency Loop VCO (one cycle, 360 degrees, of the VCO Divide-By-2 frequency added or removed at the Prescaler). The output of Integrator U5 is summed with the Bias and API currents at the virtual +5V node of the Current Summing Amplifier in-band modulation. The Low Frequency Loop Integrator (refer to Service Sheet 13), is offset by the current from U5 to compensate for the 2 cycles removed or added. The phase of the Low Frequency Loop VCO is continuous when cycles are removed or added for frequency modulation.

The Up/Down Counters and Phase Deviation DAC, U16 with resistors R704, R726 and R734 provide dc current feedback to Integrator U5. When DC FM is selected, the feedback circuits are disabled. The high DC FM input disables the Up/Down Counter U20 and opens switch U4A. The Integrator, Threshold Comparator's, Reset Timing, and current switches are still active. With the feedback resistors disabled, the Integrator has dc offset in the DC FM mode of operation.

TROUBLESHOOTING

Procedures for checking part of the A3 Low Frequency Loop Assembly circuits are shown below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-f2. Post-Repair Adjustments

Test Equipment

Oscilloscope	HP 54100A
Oscilloscope Active Probe, Chan 1	HP 54001A
Oscilloscope 1 Megohm Probe Pod, Chan 2	HP 54003A
Oscilloscope Probe Pod, Chan 3	HP 54002A
Oscilloscope Probe	HP 54003-61617A
Function Generator	HP 3312A

⟨✓1⟩FM Digital Circuits, In-Band Analog

The FM Integrator and In-Band Analog circuits are checked for proper operation with the Low Frequency Loop locked.

1. Set the Signal Generator as follows:

Frequency	950 MHz
Amplitude	Any
Modulation	AC FM, 3 kHz
Source	EXT

2. Set the Oscilloscope as follows:

Chan 1

Ch 1 Display	Off

Chan 2

Ch 2 Mode	Normal
Ch 2 Display	On
VOLTS/DIV	1.0V
OFFSET	0.0V

Timebase

SEC/DIV	2 ms
DELAY	0.0s
Delay Ref at	Left
Sweep	Trg'd

Trigger

Trigger Mode ..... Edge
Trig Src ..... Chan 3
TRIG LEVEL ..... 50 mV
Slope ..... Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 200 ms
Split Screen ..... Off
Graticle ..... Grid

3. Set the Function Generator as follows:
   a. Function to Square Wave
   b. Frequency to 100 Hz
   c. Output Level to 1 Vpk (HI and LO EXT LED's out)
   d. Connect to Oscilloscope Chan 3, 54002A, input and MOD INPUT/OUTPUT.
4. Connect Chan 2 to TP3 (ΦM INPUT). Verify that the oscilloscope display shown in Figure 2 is correct. If the waveform is not correct continue with ⟨✓2⟩

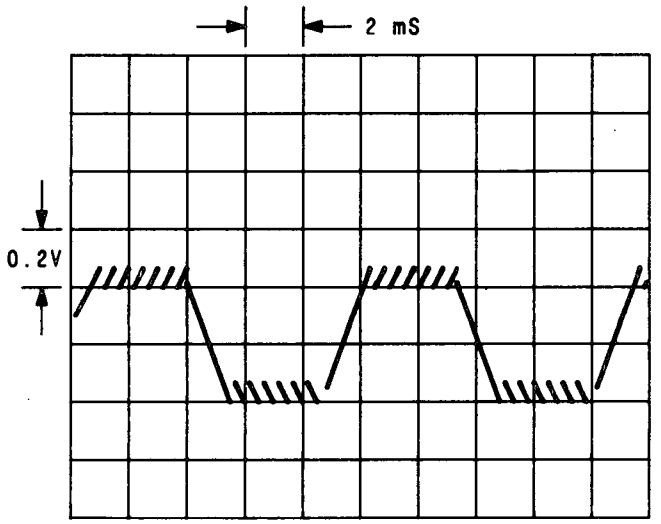


Figure 2. *Oscilloscope display of TP3 (dc coupled), Signal Generator's frequency 950 MHz, modulation EXT FM 3 kHz deviation (100 Hz square wave).*

⟨✓2⟩ FM Control Gates and Switches

1. Set up the Signal Generator, oscilloscope, and function generator as shown in ⟨✓1⟩
2. Check that the DC FM inputs at pin 4 of U20 and at pin 1 of U4A are low, and that switch U4A is closed.
3. Check that the FM OFF input at pin 2 of U15A is low, that the output at pin 1 of U15A is high, and that the output at pin 4 of U15B is low. Check that switch U4B is closed.
4. Check that the FM Enable inputs at pin 9 of U4C and pin 16 of U4D are low, and that switches U4C and U4D are closed.

√3 FM Reset Timing

1. Set up the Signal Generator, oscilloscope, and function generator as shown in √1
2. Check for the 5 MHz Reference input at pin 3 of U31A, the Remove Cycle input at pin 3 of U25A, and the Add Cycle input at pin 11 of U25B.
3. Change the oscilloscope Sec/Div to 0.2 μs. Check for the positive 400 ns Remove Cycle pulse at pin 9 of U31B, and the negative 400 ns Add Cycle pulse at pin 8 of U37B.
4. Check that the Set (pin 10), and Reset (pin 13) inputs to Up/Down Control U19B are gated low for 200 ns, and that the output at pin 8 is gated.
5. Check that the output of NOR gate U15C is gating to count the Counter U20 up or down.

√4 Up/Down Counters, Phase Deviation DAC, Current-To-Voltage Converter

1. Set-up the Signal Generator, oscilloscope, and function generator as shown in √1
2. Change Chan 2 VOLTS/DIV setting to 100 mV.
3. Set the modulation on the Signal Generator to OFF.
4. Check the input to the Phase Deviation DAC U16. The input at pin 4 is low, and the inputs at pins 5 through 13 are high.
5. Check that the voltage at TP4 (OFFSET ZERO) is approximately 0.0V.
6. Set the Signal Generator as follows:
   a. Modulation to FM, 99 kHz
   b. Source to EXT
7. Verify that the oscilloscope displays the same waveform as shown in Figure 3.

√5 Current Switches

1. Set-up the Signal Generator and function generator as shown in √1
2. Set the Oscilloscope as follows:

Chan 1

Ch 1 Display ..... Off

Chan 2

Ch 2 Mode ..... Normal
Ch 2 Display ..... On
VOLTS/DIV ..... 500 mV
OFFSET 0.0V

Timebase

SEC/DIV ..... 200 ns
DELAY 0.0s
Delay Ref at ..... Left
Sweep ..... Trg'd

Trigger

Trigger Mode ..... Edge
Trig Src ..... Chan 2
TRIG LEVEL ..... 50 mV
Slope ..... Pos

Display

Display Mode ..... Normal
DISPLAY TIME ..... 200 ms
Split Screen ..... Off
Graticle ..... Grid

3. Connect Chan 2 to TP5 (POSITIVE CURRENT), select oscilloscope AUTO SCALE, and check for a 400 ns pulse from −1.5V to +0.3V.
4. Set the oscilloscope to trigger on negative slope. Connect Chan 2 to TP6 (NEGATIVE CURRENT), select oscilloscope AUTO SCALE, and check for a 400 ns pulse from +1.5V to −0.3V.
5. Connect Chan 2 between diodes CR706 and CR707. Verify that the oscilloscope displays the same waveform as shown in Figure 4.
6. Set the oscilloscope to trigger on negative slope. Connect Chan 2 between diodes CR704 and CR705. Verify that the oscilloscope displays the same waveform as shown in Figure 5.

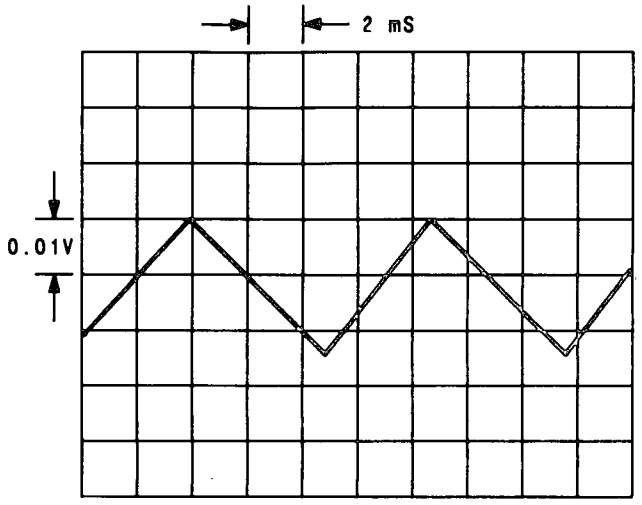


Figure 3. *Oscilloscope display of TP4 (dc coupled), Signal Generator's frequency 950 MHz, modulation EXT FM 99 kHz (100 Hz square wave).*

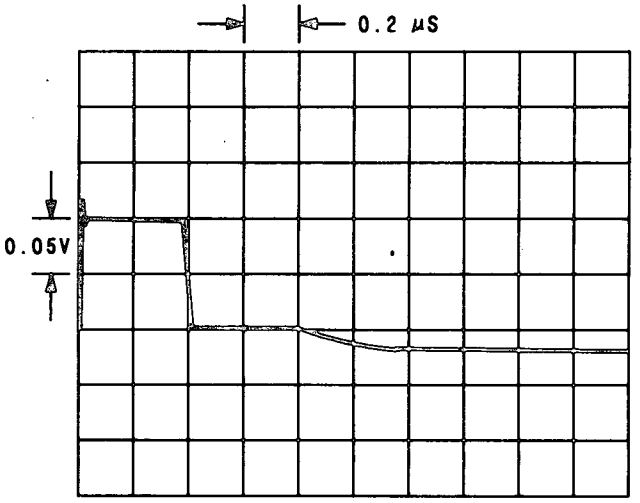


Figure 4. *Oscilloscope Display between diodes CR706 and CR707 (dc coupled), Signal Generator's frequency is 950 MHz, modulation EXT FM 99 kHz deviation (100 Hz square wave).*

✓6 Integrator, High and Low Threshold Comparators

1. Set-up the Signal Generator, oscilloscope, and function generator as shown in ✓1
2. Connect Chan 2 to TP3 (ΦM INPUT), and verify that the waveform shown in Figure 6 is correct. Set Trig Src to Chan 3.

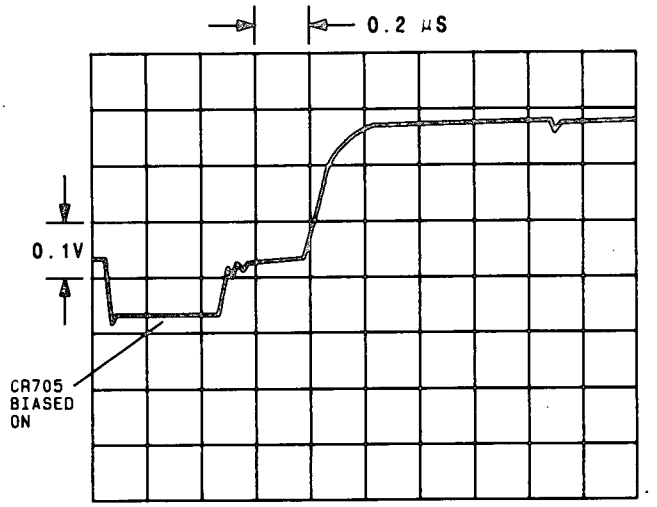


Figure 5. *Oscilloscope Display between diodes CR704 and CR705 (dc coupled), Signal Generator's frequency is 950 kHz, modulation EXT FM 99 kHz (100 Hz square wave).*

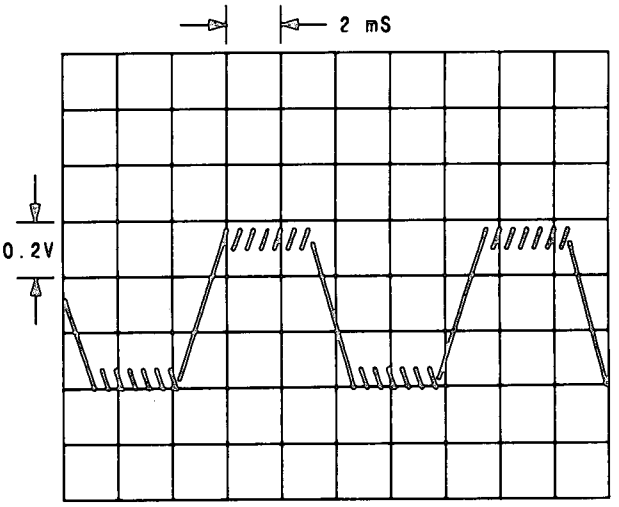


Figure 6. *Oscilloscope Display of TP3 (dc coupled), Signal Generator's frequency is 950 MHz, modulation EXT FM 3 kHz deviation (100 Hz square wave).*

3. Connect Chan 2 to TP8 (HIGH THRESHOLD). Sets of pulses from approximately 0.0V to approximately +4.5V should be displayed. Pulses are narrow.
4. Connect Chan 2 to TP9 (LOW THRESHOLD). Sets of pulses from approximately 0.0V to approximately +4.5V should be displayed.
5. Connect Chan 2 to TP3, and Chan 1 to pin 3 of U25A. Set the Chan 1 DISPLAY to On, its OFFSET to 4.0V, and its VOLTS/DIV to 2.0V.

   There should be a Remove Cycle pulse for every high threshold reset of the Integrator.
6. Connect Chan 2 to TP3, and Chan 1 to pin 11 of U25B. There should be an Add cycle pulse for every low threshold reset of the Integrator.

NOTE

When using the digital oscilloscope, the narrow pulses appear not to be present on every sweep due to the sample rate.

A3 Component Coordinates (1 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	E,1	C213	C,1	C513	A,4	CR1	D,2	FL1	E,2	Q10	D,4
C2	D,2	C300	D,2	C514	A,3	CR2	D,2	FL2	E,2	Q11	D,4
C3	E,2	C301	C,3	C515	A,4	CR3	D,2	FL3	D,2	Q12	A,4
C4	D,2	C302	C,3	C516	A,3	CR4	D,2	FL4	D,2	Q13	B,4
C5	D,1	C303	D,3	C517	A,3	CR5	E,1			Q14	B,4
C6	D,2	C304	D,3	C518	B,3	CR6	D,1	J1	E,4	Q15	B,4
C7	D,1	C305	D,3	C519	A,3	CR7	D,2	J2	A,4	Q16	C,4
C8	D,1	C306	C,2	C520	A,3	CR8	D,2	J3	A,4	Q17	C,4
C9	D,2	C307	C,3	C521	A,3	CR9	E,1	J4	C,2	Q18	C,4
C10	D,2	C308	C,3	C600	B,3	CR10	D,1	J5	C,1	Q19	D,4
C11	E,1	C309	C,3	C601	B,3	CR11	D,1	J6	D,1	Q20	D,4
C12	D,1	C310	C,2	C602	B,3	CR12	D,1	J7	E,1	Q21	D,4
C13	D,2	C311	C,1	C603	B,3	CR15	E,1	J8	E,2	Q22	B,4
C14	D,2	C312	C,1	C604	B,3	CR16	D,1			Q23	C,4
C15	D,1	C313	C,2	C605	B,3	CR17	E,2	L1	E,2	Q24	C,4
C16	D,2	C400	B,3	C606	B,3	CR18	D,2	L2	D,2	Q25	C,4
C17	D,1	C401	D,4	C607	B,3	CR200	C,1	L3	E,2	Q26	B,4
C18	E,1	C402	C,4	C608	B,3	CR201	C,1	L5	E,2	Q27	B,4
C19	E,2	C403	C,3	C609	B,3	CR400	B,4	L6	E,2	Q28	C,4
C20	E,2	C404	B,4	C610	C,3	CR401	C,4	L8	D,2	Q29	A,4
C21	E,1	C405	C,3	C611	C,4	CR402	C,4	L200	E,4	Q30	A,4
C22	E,2	C406	C,4	C612	C,3	CR403	C,4	L201	E,4	Q31	A,4
C23	E,1	C407	C,4	C613	B,3	CR404	C,4	L202	E,4	Q32	A,4
C24	E,2	C408	B,3	C614	B,3	CR405	B,4	L203	E,4	Q33	B,4
C25	E,1	C409	B,4	C615	B,2	CR406	B,4	L204	C,1	Q34	A,3
C26	E,2	C410	C,4	C616	B,3	CR500	B,4	L300	C,1	Q35	B,3
C27	D,1	C411	B,4	C617	B,2	CR501	B,4	L400	B,4	Q36	B,3
C28	E,2	C412	C,4	C618	B,3	CR502	A,4	L401	D,4	Q37	A,3
C29	D,1	C413	B,4	C619	B,3	CR503	A,4	L402	C,3	Q38	A,3
C30	E,1	C414	B,4	C620	B,2	CR504	B,4	L403	C,3	Q39	A,3
C100	A,3	C415	B,4	C621	B,2	CR505	B,4	L404	C,4	Q40	A,3
C101	A,2	C416	B,4	C700	E,3	CR506	B,4	L500	B,4	Q41	A,3
C200	E,4	C500	A,4	C701	E,3	CR600	B,3	L501	A,4	Q42	A,3
C201	E,4	C501	A,4	C702	E,3	CR602	B,3	L502	A,4	Q43	A,3
C202	E,4	C502	B,4	C703	E,2	CR700	D,4	L503	A,4	Q44	A,3
C203	E,4	C503	A,4	C704	E,3	CR701	D,4			Q46	A,2
C204	B,1	C504	A,3	C705	E,4	CR702	D,4	Q1	A,4	Q47	C,1
C205	C,2	C505	B,4	C706	E,4	CR703	D,4	Q2	A,4	Q48	C,2
C206	C,1	C506	B,4	C707	D,4	CR704	D,4	Q3	D,4	Q49	D,1
C207	C,1	C507	A,4	C708	D,4	CR705	D,4	Q4	A,4	Q50	E,1
C208	C,1	C508	B,3	C709	D,4	CR706	D,4	Q5	B,4	Q51	C,1
C209	C,1	C509	B,3	C710	D,4	CR707	D,4	Q6	B,4	Q52	D,1
C210	C,1	C510	A,4	C711	D,4			Q7	B,4	Q53	D,1
C211	C,1	C511	B,3	C712	D,4			Q8	C,4	Q54	E,1
C212	C,1	C512	A,3	C713	E,4	DS500	A,3	Q9	C,4	Q55	E,1

A3 Component Coordinates (2 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
Q56	C,1	R207	C,1	R431	B,4	R523	A,4	R568	A,3	R719	D,4
		R208	C,1	R432	C,3	R524	A,4	R569	B,3	R720	E,4
R1	D,2	R209	B,1	R433	D,4	R525	A,3	R570	A,3	R721	D,4
R2	D,2	R210	C,1	R434	C,4	R526	A,4	R600	B,3	R722	D,4
R3	D,2	R211	C,1	R435	C,3	R527	A,3	R601	B,3	R723	D,4
R4	E,2	R300	C,3	R436	B,4	R528	A,3	R602	B,3	R724	D,4
R5	D,2	R301	C,3	R437	B,4	R529	A,4	R603	B,3	R725	D,4
R6	D,1	R302	C,3	R438	D,4	R530	A,4	R604	B,3	R726	D,4
R7	D,2	R303	C,3	R439	C,3	R531	A,3	R605	B,3	R727	D,4
R8	D,1	R304	C,3	R440	C,4	R532	B,3	R606	B,3	R728	D,4
R9	E,1	R305	C,2	R441	B,4	R533	A,4	R607	B,3	R729	D,4
R10	D,2	R306	D,2	R442	C,4	R534	A,3	R608	A,3	R731	D,4
R11	D,2	R307	C,1	R443	B,4	R535	A,3	R609	B,3	R732	C,4
R12	D,2	R308	C,1	R444	B,4	R536	A,4	R610	B,3	R733	D,4
R13	D,1	R400	C,4	R445	B,4	R537	A,4	R611	B,3	R734	D,4
R14	D,2	R401	C,4	R446	B,4	R538	A,3	R612	C,3	R735	C,4
R15	E,1	R402	B,4	R447	B,4	R539	A,3	R613	B,3	R736	D,4
R16	D,1	R403	B,4	R448	B,4	R540	A,4	R614	B,3	R737	C,4
R17	D,1	R404	B,4	R449	B,4	R541	A,3	R615	B,3	R738	D,4
R18	E,1	R405	B,4	R450	B,4	R542	A,3	R616	C,3	R740	D,4
R19	D,1	R406	C,4	R451	C,4	R543	A,4	R617	B,3	R741	E,4
R20	D,1	R407	C,4	R452	C,4	R544	A,3	R618	B,3		
R21	D,1	R408	C,4	R500	A,4	R545	A,4	R619	B,3	TP1	B,4
R22	D,1	R409	B,4	R501	A,4	R546	A,3	R620	B,3	TP2	A,4
R23	E,1	R410	C,4	R502	A,4	R547	A,4	R621	B,2	TP3	D,4
R24	E,1	R411	C,4	R503	A,4	R548	A,3	R622	B,3	TP4	D,4
R25	E,2	R412	B,4	R504	A,4	R549	A,3	R700	E,4	TP5	D,4
R26	E,2	R413	C,4	R505	A,4	R550	A,3	R701	E,4	TP6	D,4
R27	E,2	R414	B,4	R506	A,4	R551	A,3	R702	E,4	TP7	C,4
R28	D,2	R415	C,4	R507	A,4	R552	A,4	R703	E,4	TP8	D,4
R29	D,1	R416	C,4	R508	A,4	R553	A,3	R704	D,4	TP9	D,4
R30	D,1	R417	C,4	R509	A,4	R554	A,3	R705	E,4	TP10	B,3
R31	D,1	R418	C,4	R510	A,4	R555	A,3	R706	D,4	TP11	A,3
R32	D,1	R419	B,4	R511	A,4	R556	A,3	R707	B,4	TP12	A,3
R33	D,2	R420	B,4	R512	A,4	R557	A,3	R708	E,4	TP13	B,3
R100	A,2	R421	C,4	R513	A,4	R558	A,3	R709	D,4	TP14	B,3
R101	A,2	R422	C,4	R514	A,4	R559	A,3	R710	D,4	TP15	C,3
R104	A,2	R423	C,4	R515	A,4	R560	A,3	R711	D,4	TP16	C,3
R200	B,2	R424	C,4	R516	A,4	R561	A,3	R712	B,4	TP17	C,3
R201	C,1	R425	C,4	R517	A,4	R562	A,3	R713	D,4	TP18	D,3
R202	C,2	R426	C,4	R518	B,4	R563	A,3	R714	D,4	TP19	D,3
R203	C,2	R427	C,4	R519	A,4	R564	A,3	R715	D,4	TP20	C,3
R204	C,1	R428	C,4	R520	A,4	R565	B,3	R716	C,4	TP21	C,3
R205	C,1	R429	B,4	R521	A,3	R566	A,3	R717	D,4	TP22	A,3
R206	C,1	R430	C,3	R522	B,4	R567	A,3	R718	E,4	TP23	A,3

A3 Component Coordinates (3 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
TP24	C,3	U35	C,2						
TP25	C,3	U36	D,2						
TP26	C,2	U37	E,2						
TP27	C,2	U38	C,2						
TP28	C,2	U39	C,2						
TP29	C,2	U40	D,2						
TP30	C,1	U41	C,2						
TP31	C,1	U42	C,2						
TP32	D,1	U43	C,2						
TP33	E,1	U44	C,2						
		U45	D,2						
U1	A,4	U46	C,1						
U2	B,4	U47	C,1						
U3	C,4	U48	D,1						
U4	D,4	U49	C,1						
U5	D,4	U50	C,1						
U6	C,4	U51	C,1						
U7	B,4	U52	D,1						
U8	C,4	U53	E,1						
U9	A,4	U54	C,1						
U10	D,4	U55	C,1						
U11	D,4								
U12	E,3	VR300	C,3						
U13	B,3	VR400	B,4						
U14	B,3	VR401	C,4						
U15	E,3	VR500	A,3						
U16	E,3	VR601	B,3						
U17	C,3								
U18	D,3	W1	B,3						
U19	E,3	W2	C,3						
U20	E,3	W3	A,3						
U21	A,3	W4	B,3						
U22	B,3	W5	A,3						
U23	D,3	W6	A,2						
U24	D,3	W7	D,1						
U25	E,3	W8	C,1						
U26	E,3	W9	C,4						
U27	B,3	W10	C,4						
U28	C,3	W11	B,4						
U29	D,3								
U30	D,3	Y1	E,2						
U31	E,3	Y300	C,2						
U32	E,3								
U33	B,3								
U34	B,3								

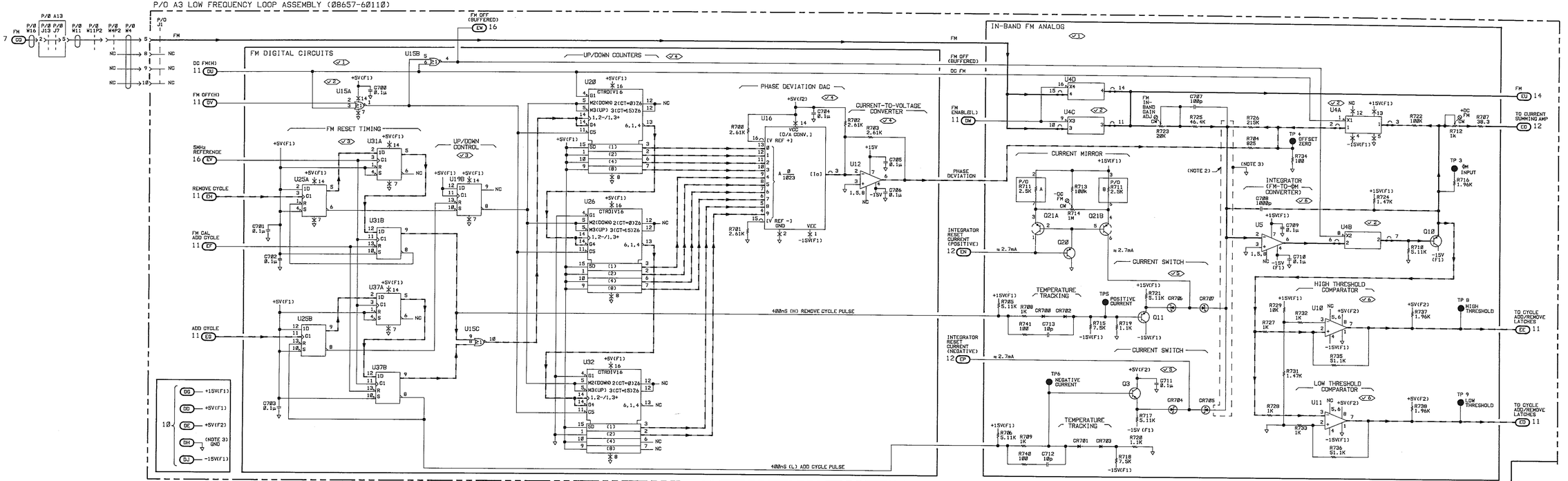


Figure 7
Service Sheet 15 15

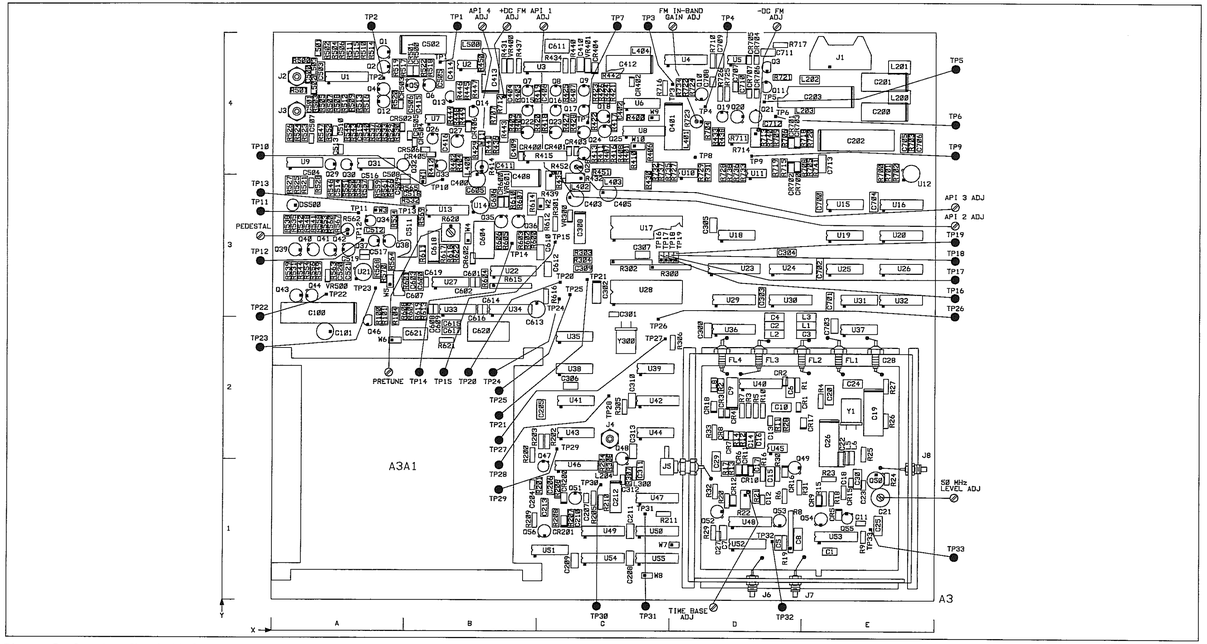


Figure Ø. Service Sheet 16 Information

Component Locator

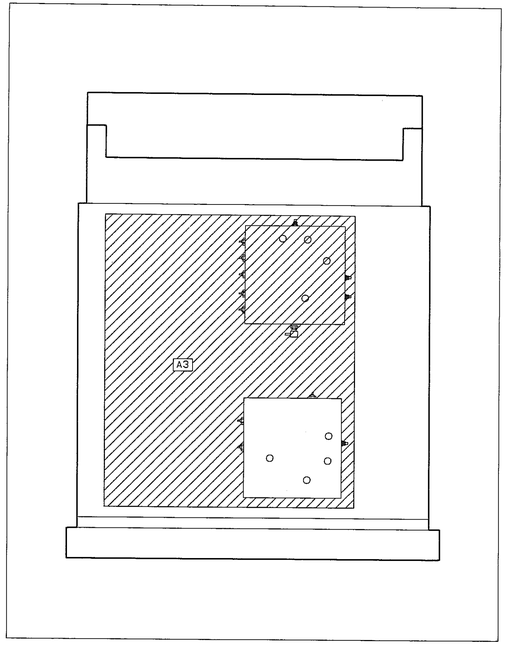
NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Chassis ground is achieved by J3 and J4 connection and mechanical contact through nuts holding PC board to cover and W4.
3. Printed circuit trace inductor.
4. PC board shipped with resistive jumper installed in the 10 MHz position.
5. Reference designations on this service sheet C, CR, FL, L and R have numbers ranging from 1 to 99 only.

LOGIC LEVELS

	TTL	ECL
HIGH	2V	+4.2V
LOW	0.8V	+3.3V
IS MORE NEG. THAN		
IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

P/O A3 — LOW FREQUENCY LOOP IN-BAND FREQUENCY MODULATION — SEE REVERSE SIDE — SS15



Service Sheet 16

LOW FREQUENCY LOOP 50 MHZ REFERENCE OSCILLATOR, PHASE LOCK LOOP

PRINCIPLES OF OPERATION

50 MHz Reference Oscillator

The 50 MHz Reference Oscillator, Q50, is a common-base crystal controlled oscillator. The amount of positive feedback is predetermined by the taps on inductor L7. Inductor L7 is a spiral printed circuit board trace.

The base of Q50 is biased by resistor R24 at approximately 0 Vdc. The emitter is biased by resistors R25 and R26. Resistor R26 is connected to the −15 Vdc supply which biases on diodes CR13 and CR14. This closes the dc current path for the emitter current of Q50 and also closes the tank circuit. The tank circuit consists of the crystal Y1, varactor diode CR15, printed circuit board inductor L7, and capacitors C21 and C23. The output frequency can be adjusted by R22 (TIME BASE ADJ) which controls the voltage across the varactor diode CR15 thereby changing the capacitance of the tank circuit. This tune voltage is applied through resistors R21, R23 and RF chokes L5 and L6. The output level is peaked by capacitor C21 (50 MHZ LEVEL ADJ). Capacitors C18, C19, C20, C24, C25 and C26 are bypass capacitors.

Time Base Divider

The output of the 50 MHz Reference Oscillator is ac coupled by C30 to the Frequency Multiplier Assembly shown on Service Sheet 3. The output is also ac coupled by capacitor C11 to common-base Time Base Buffer Q55. The output of Q55 clocks the Divide-by-10 circuit U53 at pin 7. This divider is made up of a Divide-by-5 and a Divide-by-2 circuit. Note that the set inputs are all tied low. The output, 10 MHz at pin 4, is the 50 MHz Divide-by-5. The 10 MHz output at pin 4 clocks the Divide-by-2 circuit at pin 12, and its output is 5 MHz.

The 5 MHz outputs, at pins 14 and 15 of U53, clocks the ECL-To-TTL Converter transistors Q54 and Q53. Q54 converts the ECL logic levels to TTL logic levels and Q53 provides the current drive. The TTL output of Q53 clocks the Divide-By-5 circuit U48A and its output is 1 MHz at pin 6.

The 1 MHz output of U48A clocks the Divide-by-2 section of U48B and its 500 kHz output at pin 13 clocks the Divide-by-5 section. The output of U48B at pin 9 is 100 kHz.

One of the three divided output frequencies, 10, 5, or 1 MHz may be selected to phase lock the reference oscillator to an internal (Option 001) or external time base. The resistor jumper is shipped in the 10 MHz position and must be moved to the 5 or 1 MHz position depending upon the frequency of the external time base. The Time Base Output follows the frequency selected by the jumper.

The Time Base output is applied to pin 11 of exclusive-or gate U40C. Its other input is tied to +5 Vdc. The output from pin 14 is the input phase shifted 180 degrees. The signal is then detected by diode CR18 and ac coupled to the Time Base Output J4.

100 kHz Reference

The 100 kHz Reference output of U48B clocks the Synchronization D flip-flop U52A, and its output is synchronized with the 5 MHz output of Q53 by U52B. The Pulser circuit, capacitor C27 and transistor Q52, change the output of U52B to a narrow pulse.

5 MHz Switch

The 5 MHz switch transistor Q49 is controlled by the FM OFF input (refer to Service Sheet 15). When frequency modulation is not selected, the FM OFF input is high and Q49 is biased off. When frequency modulation is selected, the FM OFF input is low and Q49 is biased on and off by the 5 MHz input from Q53. The 5 MHz output at the emitter of Q49 clocks the FM Reset Timing D flip-flops (refer to Service Sheet 15).

Reference Phase Lock Circuit

The Time Base Input signal is ac coupled by C6 to resistor R1, and the positive and negative peak limiting diodes of CR1 and CR2. The input is then ac coupled by capacitor C10 to pin 7 of exclusive-or gate buffer U40B. The input goes to ac ground by resistors R2 and R3 and capacitor C9. The output is connected through the resistor R7 to the resistor P/O R8 and diode CR3. CR3 detects the Time Base Input signal, and applies the voltage to the positive input of External Reference Detector U45B. The positive input is increased so it is more positive than the negative input, and the output of U45B switches to +15 Vdc, detecting the presence of a Time Base Input. When the output of U45B switches to +15 Vdc the phase lock operational amplifier U45A is activated by turning off diode CR6 and turning on diode CR11. The inputs of comparator U45B are connected to U40B pin 3, the exclusive-or gate output. Diode CR4 temperature compensates CR3.

The Time Base Input signal from U40B pin 3 is connected to U40A pin 4. The other input, pin 5, is the divided output of the 50 MHz Reference Oscillator. The signal is divided to 10, 5 or 1 MHz depending on the Time Base Input frequency and the subsequent jumper placement. This exclusive-or gate serves as a phase detector with its change in output voltage being proportional to the phase difference of the two inputs. The output is coupled to the 50 MHz Reference Oscillator which serves to phase lock the oscillator to the Time Base Input signal. The correction voltage to U45A is amplified and applied to the oscillator tank circuit through diode CR10. CR10 is turned on when comparator U45B turns CR6 off, and the negative input of U45B changes to approximately +3V. The positive input is fixed and the output goes from +15 Vdc to approximately −7V. CR10 is turned on as are diodes CR7 and CR8 when the phase difference is large enough. Resistor R14 is bypassed which moves the reference oscillator to the correct frequency.

TROUBLESHOOTING

Procedures for checking part of the A3 Low Frequency Loop Assembly circuits are given below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. Fixed voltages are shown on the schematic inside a hexagon, for example, ⟨2V ±0.2V⟩. Transistor bias voltages are shown without tolerances.

Troubleshooting Help

Block Diagram 3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Digital Multimeter ..... HP 3466A
Oscilloscope ..... HP 54100A
Oscilloscope Active Probe, Chan 1 ..... HP 54001A

⟨✓1⟩ Reference Phase Lock Circuit

Measure the voltage shown in Table 1. With an external reference oscillator connected to the Time Base Input or with the internal reference oscillator installed, the 50 MHz oscillator should be phase locked.

Table 1. Crystal Phase Lock Circuit Voltages.

Operating Mode		Voltages (dc and ac) on									
		U40-Pin				U45B-Pin			U45A-Pin		
		7	5	2	3	5	6	7	3	2	1
Phase Locked	Vdc	+3.8	+3.8	+3.8	+4.0	+4.0	+3.7	+13	+4	+4	−10
	Vpk	0.4	0.4	0.4	0.4	0.01	0.01	0.01	0.08	0	0.02
Not Phase Locked	Vdc	+3.8	+3.8	+3.8	+3.8	+3.5	+3.7	−13	+4	+3	+14
	Vpk	0.02	0.4	0.2	0.05	0.01	0.01	0.005	0.02	0	0.008

⟨✓2⟩ 50 MHz Reference Oscillator

1. Verify that Q50's bias voltages are correct.
2. Measure the oscillator output at TP33 (50 MHz).

⟨✓3⟩ Time Base Dividers

1. Measure the TIME BASE OUTPUT signals at J7.
2. Measure the 5 MHz signal at pin 15 of U53.
3. Measure the 5 MHz signal at pin 14 of U53 and at TP32.
4. Measure the 1 MHz signal at pin 6 of U48A.
5. Measure the 500 kHz signal at pin 13 of U48B.
6. Measure the 100 kHz signal at pin 9 of U48B.

⟨4⟩ 100 kHz Reference

1. Check the 100 kHz signal at pin 5 of U52A, and at pin 9 of U52B.
2. Check the 100 kHz output pulse of Q52 at J5. The pulse is narrow and approximately 1.5 Vpk.

⟨5⟩ 5 MHz Switch

1. Select Frequency Modulation at the Signal Generator's front-panel and check for a low FM OFF input to FL4.
2. Check that transistor Q49 is biased on.
3. Measure for a 5 MHz signal at feedthrough capacitor C28.

NOTE

A residual FM problem at the RF output may be due to residual FM from the 50 MHz Reference Oscillator. Measuring residual FM of the Reference Oscillator using the test setup found in Section 4 may be inconclusive. The residual FM of the measuring instrument (HP 8902A Measuring Receiver) is normally greater than that of a Reference Oscillator that is operating properly. All connectors to the 50 MHz Oscillator must be tight to prevent noise on the 50 MHz signal.

A3 Component Coordinates (1 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	E,1	C213	C,1	C513	A,4	CR1	D,2	FL1	E,2	Q10	D,4
C2	D,2	C300	D,2	C514	A,3	CR2	D,2	FL2	E,2	Q11	D,4
C3	E,2	C301	C,3	C515	A,4	CR3	D,2	FL3	D,2	Q12	A,4
C4	D,2	C302	C,3	C516	A,3	CR4	D,2	FL4	D,2	Q13	B,4
C5	D,1	C303	D,3	C517	A,3	CR5	E,1			Q14	B,4
C6	D,2	C304	D,3	C518	B,3	CR6	D,1	J1	E,4	Q15	B,4
C7	D,1	C305	D,3	C519	A,3	CR7	D,2	J2	A,4	Q16	C,4
C8	D,1	C306	C,2	C520	A,3	CR8	D,2	J3	A,4	Q17	C,4
C9	D,2	C307	C,3	C521	A,3	CR9	E,1	J4	C,2	Q18	C,4
C10	D,2	C308	C,3	C600	B,3	CR10	D,1	J5	C,1	Q19	D,4
C11	E,1	C309	C,3	C601	B,3	CR11	D,1	J6	D,1	Q20	D,4
C12	D,1	C310	C,2	C602	B,3	CR12	D,1	J7	E,1	Q21	D,4
C13	D,2	C311	C,1	C603	B,3	CR15	E,1	J8	E,2	Q22	B,4
C14	D,2	C312	C,1	C604	B,3	CR16	D,1			Q23	C,4
C15	D,1	C313	C,2	C605	B,3	CR17	E,2	L1	E,2	Q24	C,4
C16	D,2	C400	B,3	C606	B,3	CR18	D,2	L2	D,2	Q25	C,4
C17	D,1	C401	D,4	C607	B,3	CR200	C,1	L3	E,2	Q26	B,4
C18	E,1	C402	C,4	C608	B,3	CR201	C,1	L5	E,2	Q27	B,4
C19	E,2	C403	C,3	C609	B,3	CR400	B,4	L6	E,2	Q28	C,4
C20	E,2	C404	B,4	C610	C,3	CR401	C,4	L8	D,2	Q29	A,4
C21	E,1	C405	C,3	C611	C,4	CR402	C,4	L200	E,4	Q30	A,4
C22	E,2	C406	C,4	C612	C,3	CR403	C,4	L201	E,4	Q31	A,4
C23	E,1	C407	C,4	C613	B,3	CR404	C,4	L202	E,4	Q32	A,4
C24	E,2	C408	B,3	C614	B,3	CR405	B,4	L203	E,4	Q33	B,4
C25	E,1	C409	B,4	C615	B,2	CR406	B,4	L204	C,1	Q34	A,3
C26	E,2	C410	C,4	C616	B,3	CR500	B,4	L300	C,1	Q35	B,3
C27	D,1	C411	B,4	C617	B,2	CR501	B,4	L400	B,4	Q36	B,3
C28	E,2	C412	C,4	C618	B,3	CR502	A,4	L401	D,4	Q37	A,3
C29	D,1	C413	B,4	C619	B,3	CR503	A,4	L402	C,3	Q38	A,3
C30	E,1	C414	B,4	C620	B,2	CR504	B,4	L403	C,3	Q39	A,3
C100	A,3	C415	B,4	C621	B,2	CR505	B,4	L404	C,4	Q40	A,3
C101	A,2	C416	B,4	C700	E,3	CR506	B,4	L500	B,4	Q41	A,3
C200	E,4	C500	A,4	C701	E,3	CR600	B,3	L501	A,4	Q42	A,3
C201	E,4	C501	A,4	C702	E,3	CR602	B,3	L502	A,4	Q43	A,3
C202	E,4	C502	B,4	C703	E,2	CR700	D,4	L503	A,4	Q44	A,3
C203	E,4	C503	A,4	C704	E,3	CR701	D,4			Q46	A,2
C204	B,1	C504	A,3	C705	E,4	CR702	D,4	Q1	A,4	Q47	C,1
C205	C,2	C505	B,4	C706	E,4	CR703	D,4	Q2	A,4	Q48	C,2
C206	C,1	C506	B,4	C707	D,4	CR704	D,4	Q3	D,4	Q49	D,1
C207	C,1	C507	A,4	C708	D,4	CR705	D,4	Q4	A,4	Q50	E,1
C208	C,1	C508	B,3	C709	D,4	CR706	D,4	Q5	B,4	Q51	C,1
C209	C,1	C509	B,3	C710	D,4	CR707	D,4	Q6	B,4	Q52	D,1
C210	C,1	C510	A,4	C711	D,4			Q7	B,4	Q53	D,1
C211	C,1	C511	B,3	C712	D,4			Q8	C,4	Q54	E,1
C212	C,1	C512	A,3	C713	E,4	DS500	A,3	Q9	C,4	Q55	E,1

A3 Component Coordinates (2 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
Q56	C,1	R207	C,1	R431	B,4	R523	A,4	R568	A,3	R719	D,4
		R208	C,1	R432	C,3	R524	A,4	R569	B,3	R720	E,4
R1	D,2	R209	B,1	R433	D,4	R525	A,3	R570	A,3	R721	D,4
R2	D,2	R210	C,1	R434	C,4	R526	A,4	R600	B,3	R722	D,4
R3	D,2	R211	C,1	R435	C,3	R527	A,3	R601	B,3	R723	D,4
R4	E,2	R300	C,3	R436	B,4	R528	A,3	R602	B,3	R724	D,4
R5	D,2	R301	C,3	R437	B,4	R529	A,4	R603	B,3	R725	D,4
R6	D,1	R302	C,3	R438	D,4	R530	A,4	R604	B,3	R726	D,4
R7	D,2	R303	C,3	R439	C,3	R531	A,3	R605	B,3	R727	D,4
R8	D,1	R304	C,3	R440	C,4	R532	B,3	R606	B,3	R728	D,4
R9	E,1	R305	C,2	R441	B,4	R533	A,4	R607	B,3	R729	D,4
R10	D,2	R306	D,2	R442	C,4	R534	A,3	R608	A,3	R731	D,4
R11	D,2	R307	C,1	R443	B,4	R535	A,3	R609	B,3	R732	C,4
R12	D,2	R308	C,1	R444	B,4	R536	A,4	R610	B,3	R733	D,4
R13	D,1	R400	C,4	R445	B,4	R537	A,4	R611	B,3	R734	D,4
R14	D,2	R401	C,4	R446	B,4	R538	A,3	R612	C,3	R735	C,4
R15	E,1	R402	B,4	R447	B,4	R539	A,3	R613	B,3	R736	D,4
R16	D,1	R403	B,4	R448	B,4	R540	A,4	R614	B,3	R737	C,4
R17	D,1	R404	B,4	R449	B,4	R541	A,3	R615	B,3	R738	D,4
R18	E,1	R405	B,4	R450	B,4	R542	A,3	R616	C,3	R740	D,4
R19	D,1	R406	C,4	R451	C,4	R543	A,4	R617	B,3	R741	E,4
R20	D,1	R407	C,4	R452	C,4	R544	A,3	R618	B,3		
R21	D,1	R408	C,4	R500	A,4	R545	A,4	R619	B,3	TP1	B,4
R22	D,1	R409	B,4	R501	A,4	R546	A,3	R620	B,3	TP2	A,4
R23	E,1	R410	C,4	R502	A,4	R547	A,4	R621	B,2	TP3	D,4
R24	E,1	R411	C,4	R503	A,4	R548	A,3	R622	B,3	TP4	D,4
R25	E,2	R412	B,4	R504	A,4	R549	A,3	R700	E,4	TP5	D,4
R26	E,2	R413	C,4	R505	A,4	R550	A,3	R701	E,4	TP6	D,4
R27	E,2	R414	B,4	R506	A,4	R551	A,3	R702	E,4	TP7	C,4
R28	D,2	R415	C,4	R507	A,4	R552	A,4	R703	E,4	TP8	D,4
R29	D,1	R416	C,4	R508	A,4	R553	A,3	R704	D,4	TP9	D,4
R30	D,1	R417	C,4	R509	A,4	R554	A,3	R705	E,4	TP10	B,3
R31	D,1	R418	C,4	R510	A,4	R555	A,3	R706	D,4	TP11	A,3
R32	D,1	R419	B,4	R511	A,4	R556	A,3	R707	B,4	TP12	A,3
R33	D,2	R420	B,4	R512	A,4	R557	A,3	R708	E,4	TP13	B,3
R100	A,2	R421	C,4	R513	A,4	R558	A,3	R709	D,4	TP14	B,3
R101	A,2	R422	C,4	R514	A,4	R559	A,3	R710	D,4	TP15	C,3
R104	A,2	R423	C,4	R515	A,4	R560	A,3	R711	D,4	TP16	C,3
R200	B,2	R424	C,4	R516	A,4	R561	A,3	R712	B,4	TP17	C,3
R201	C,1	R425	C,4	R517	A,4	R562	A,3	R713	D,4	TP18	D,3
R202	C,2	R426	C,4	R518	B,4	R563	A,3	R714	D,4	TP19	D,3
R203	C,2	R427	C,4	R519	A,4	R564	A,3	R715	D,4	TP20	C,3
R204	C,1	R428	C,4	R520	A,4	R565	B,3	R716	C,4	TP21	C,3
R205	C,1	R429	B,4	R521	A,3	R566	A,3	R717	D,4	TP22	A,3
R206	C,1	R430	C,3	R522	B,4	R567	A,3	R718	E,4	TP23	A,3

A3 Component Coordinates (3 of 3)

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
TP24	C,3	U35	C,2						
TP25	C,3	U36	D,2						
TP26	C,2	U37	E,2						
TP27	C,2	U38	C,2						
TP28	C,2	U39	C,2						
TP29	C,2	U40	D,2						
TP30	C,1	U41	C,2						
TP31	C,1	U42	C,2						
TP32	D,1	U43	C,2						
TP33	E,1	U44	C,2						
		U45	D,2						
U1	A,4	U46	C,1						
U2	B,4	U47	C,1						
U3	C,4	U48	D,1						
U4	D,4	U49	C,1						
U5	D,4	U50	C,1						
U6	C,4	U51	C,1						
U7	B,4	U52	D,1						
U8	C,4	U53	E,1						
U9	A,4	U54	C,1						
U10	D,4	U55	C,1						
U11	D,4								
U12	E,3	VR300	C,3						
U13	B,3	VR400	B,4						
U14	B,3	VR401	C,4						
U15	E,3	VR500	A,3						
U16	E,3	VR601	B,3						
U17	C,3								
U18	D,3	W1	B,3						
U19	E,3	W2	C,3						
U20	E,3	W3	A,3						
U21	A,3	W4	B,3						
U22	B,3	W5	A,3						
U23	D,3	W6	A,2						
U24	D,3	W7	D,1						
U25	E,3	W8	C,1						
U26	E,3	W9	C,4						
U27	B,3	W10	C,4						
U28	C,3	W11	B,4						
U29	D,3								
U30	D,3	Y1	E,2						
U31	E,3	Y300	C,2						
U32	E,3								
U33	B,3								
U34	B,3								

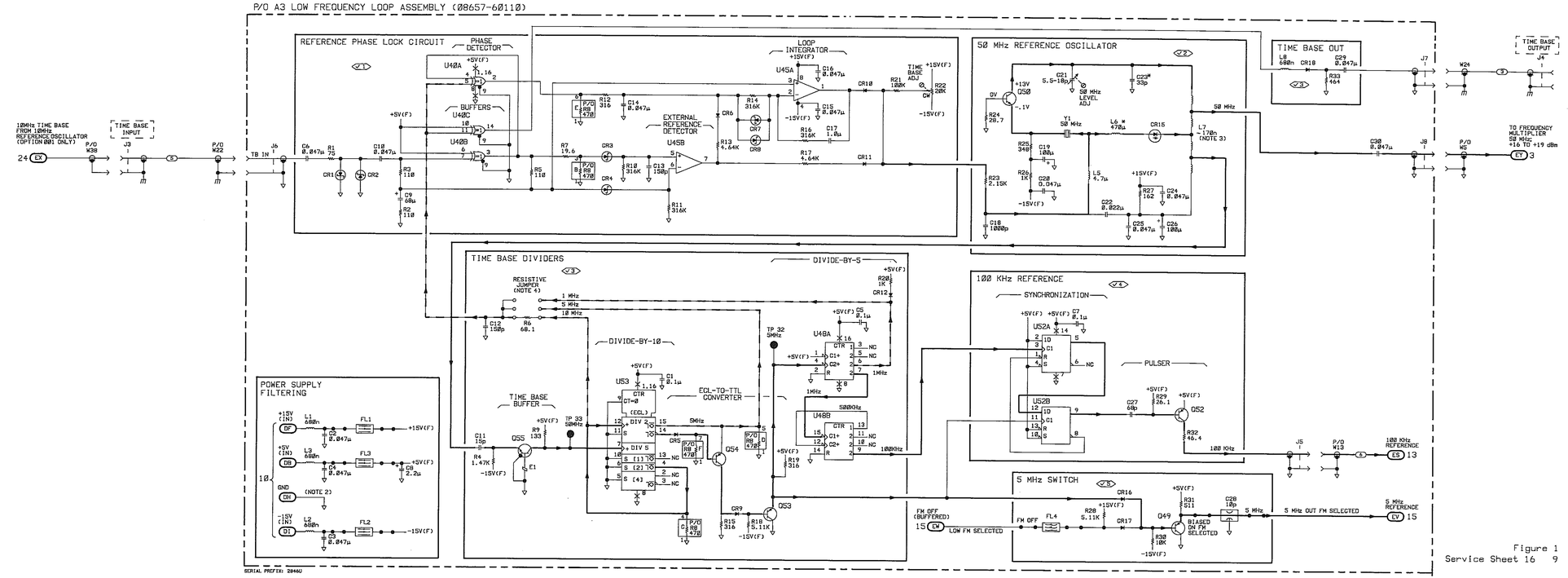


Figure 1
Service Sheet 16 9

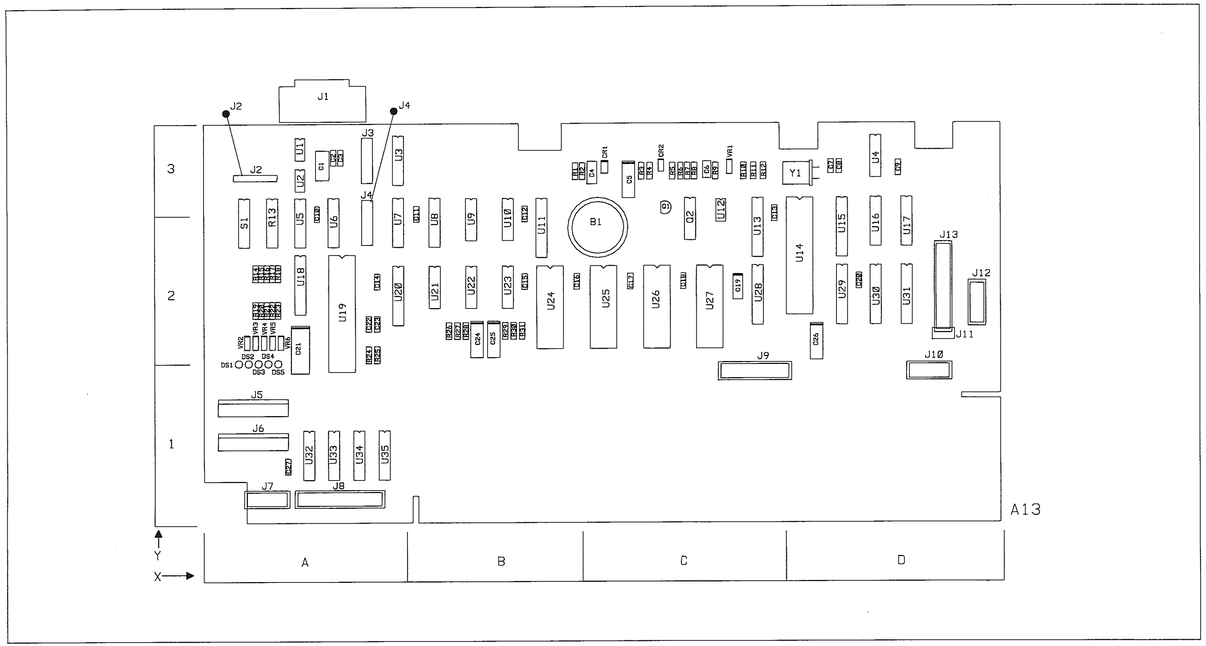


Figure Ø. Service Sheet 17 Information.

Component Locator

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Chassis ground is represented by, ⏚
3. Address data is transferred positive true from the microprocessor on the uni-directional address bus.
4. Data is transferred positive true to and from the microprocessor on the bi-directional data bus.

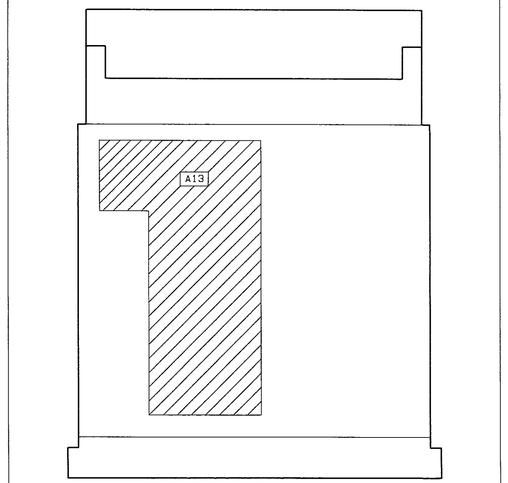
LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
IS MORE NEG. THAN IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A3
P/O A16
SEE REVERSE SIDE

LOW FREQUENCY LOOP
5ØMHz REFERENCE
OSCILLATOR AND
PHASE LOCK LOOP

SS16



Service Sheet 17

MICROPROCESSOR INTERRUPT PROCESSING, AND RESTART

PRINCIPLES OF OPERATION

Microprocessor

Instrument functions are controlled by the Microprocessor U14 as it executes the program instructions stored in ROM (read only memory). The function of the Microprocessor's data bus, address bus, and each of its input/output lines is discussed in the following paragraphs:

Data Bus

The data bus (D0 through D7) consists of 8 bi-directional data lines which transfer 8-bit, positive-true data bytes to and from the Microprocessor (U14 pins 26 through 33). The 3-state lines can be high, low, or at the high impedance state depending on the individual data bit or its buffering conditions. The Microprocessor reads data from memory, the keyboard, the HP-IB interface, etc., via the data bus under the control of its monitor program. Data is written onto the data bus for the displays, RF and modulation circuitry, etc. Information on the data bus is buffered as it enters or exits the Microprocessor. For additional information, refer to the discussion on Data Bus Buffering that follows.

Read/Write Control

The Read/Write signal from the Microprocessor (R(H)/W(L) at pin 34 of U14) controls the direction of data transfer on the data bus. When the Microprocessor is halted or available to accept data, this signal is high (indicating that the Microprocessor is in the "read" When data is being transferred out onto the data bus, this signal is low (indicating that the Microprocessor is in the "write" state). This signal is buffered by one of the Microprocessor Control Line Buffers in U15A. The buffered Read/Write signal controls the direction of data transfer: through the Data Bus Buffers in U29, to or from RAM memory (refer to Service Sheet 19), and to or from the HP-IB Interface Buffers in U20 (refer to Service Sheet 20).

Address Bus

The address bus (A0 through A15) consists of 16 unidirectional lines which transfer a 16-bit, positive-true address from the Microprocessor (pins 9 through 20 and 22 through 25). After exiting the Microprocessor, information on the address bus is buffered and decoded to produce control strobes for level, modulation, attenuation, and serial I/O data (refer to Service Sheet 18). These buffered address bits are also decoded to select RAM, or ROM memory locations (refer to Service Sheet 19) or one of the HP-IB General Purpose Interface Adapter U19 ports (refer to Service Sheet 20).

Valid Memory Address

The Microprocessor's Valid Memory Address signal (VMA at pin 5) indicates that data on the address lines is valid. Data is valid when VMA is active (high). VMA is buffered by U15A to enable the decoding and selection of ROM and RAM memory locations (refer to Service Sheet 19).

System Clock

An external 4 MHz crystal A13 Y1 is directly connected to the Microprocessor (U14 pins 38 and 39). The Microprocessor's internal divide-by-4 circuit develops the 1 MHz system clock E (U14 pin 37). Capacitors C7 and C8 are used to keep the clock frequency stable.

Memory Ready

The Microprocessor's Memory Ready input (MR at U14 pin 3) is tied to +5 V to enable the 1 MHz system-clock rate.

RAM Enable

The Microprocessor's RAM Enable input (RE at U14 pin 36) is tied to ground, to disable the internal RAM.

Halt

The Microprocessor's Halt input (HALT at U14 pin 2) is tied to +5 V to disable the input.

Reset

The Microprocessor's Reset input (RESET at U14 pin 40) starts the Microprocessor from a power-down condition. This condition exists during initial start-up of the instrument, after a power failure or power supply glitch has occurred, and when the RESET Test Point J2 pin 8 is momentarily connected to ground. When RESET is active (low), the Microprocessor becomes inactive. When RESET is inactive (high), the internal program directs program execution to the power-up subroutine. For additional information on the control of this input, refer to the discussion on Restart Circuitry that follows.

Non-Maskable Interrupt

The Microprocessor's Non-Maskable Interrupt input (NMI at U14 pin 6) interrupts program execution. When NMI is active (low), the Microprocessor finishes executing its current instruction, and saves its current status. Then the Microprocessor's internal program directs program execution to the non-maskable interrupt subroutine. For this Signal Generator, the non-maskable interrupt is used to invoke the Signal Generator's signature analysis subroutine. For additional information on the control of this input, refer to the discussion on Interrupt Processing that follows.

Maskable Interrupt Request

The Microprocessor's Maskable Interrupt Request input (IRQ at U14 pin 4) will also interrupt program execution. When IRQ is active (low), and the interrupt mask bit of the internal condition code register is not set, the Microprocessor finishes executing its current instruction. Then its internal program directs program execution to the maskable-interrupt subroutine. For additional information on the control of this input (refer to the discussion on Interrupt Processing that follows).

Data Bus Buffering

Data is transferred (positive-true) to and from the Microprocessor on the bidirectional, 8-bit data bus. Information on the data bus is buffered after it exits or before it enters the Microprocessor. The 3-state, bidirectional Data Bus Buffers in U29 provide asynchronous, 2-way communication between the data bus and the Microprocessor. During normal operation, rocker switch S1C is set to NRM causing the enable input of U29 (pin 19) to be pulled low through the inverter U21C. The enable input of the 3-state buffer U9C is also pulled low through U21C (refer to the discussion on Interrupt Processing that follows).

The direction of data transfer through U29 is controlled by the state of the buffered Read/Write line from the Microprocessor. When the direction-controlling input of U29 (pin 1) is high, information is transferred from the data bus to the Microprocessor (a "read" operation). When this input is low, information is transferred from the Microprocessor to the data bus (a "write" operation).

When U30 is enabled (refer to Service Sheet 18), data bus information is written to the Modulation Control Latches/Mode Selects on the Audio Assembly A11 (refer to Service Sheet 6). When U30 is disabled, the data bus information is not written to the Audio Assembly.

Sixteen bits of serial keyboard data are transferred from the storage registers on the Display Assembly A2 to the Microprocessor via bit 0 of the data bus (refer to Service Sheet 21). During the keyboard read subroutine, the Keyboard Serial Data Bus Buffer U4A is enabled to couple the serial, keyboard data to the bit 0 input of U29.

Hard-wired NOP

The hard-wired NOP (no operation) instruction is a service feature of this instrument. This 8-bit instruction steps the Microprocessor through its addresses during ROM testing or troubleshooting. When the Microprocessor receives a NOP instruction, its program counter advances once for every two clock cycles without affecting any other operations. The 8 inputs to the 3-state buffer U31 are configured and hard-wired to provide the NOP instruction (00000001) to the Microprocessor. During normal operation, rocker switch S1C is set to NRM, (high input at U31 pin 1) disabling the outputs of U31. During ROM testing, S1C is set to ROM to enable the outputs of U31, which places the hard-wired NOP instruction on the data bus. U29 is disabled as a result of U21C inverting the low set up by S1C, which pulls U29 pin 19 high. Disabling U29 inhibits the NOP instruction from being transferred to any circuitry but the Microprocessor.

Restart Circuitry

The Signal Generator employs an internal battery backup to save the contents of RAM, refer to Service Sheet 19, whenever the instrument is in standby or is unplugged. The restart circuitry disables the RAM and directs the Microprocessor to begin it's power-up routine when the +5 V supply reaches a nominal voltage after a reset. Reset of the Signal Generator occurs:

1. During power-up initialization.
2. During service by briefly connecting TP (RESET) (J2 pin 8) to ground.

When the Signal Generator is unplugged or in standby, 2.8 V from battery B1 is applied to the RAM's Vcc input through R2 and CR2. CR1 is biased off to isolate the battery from the +5 V supply. Battery voltage is also applied to the RAM SELECT through R3, disabling the RAM. Reset occurs whenever the Signal Generator is turned ON or after test point J2 pin 8 is momentarily connected to ground. The +5 volt supply is connected through R9 to the RESIN input of U12 at pin 2. When the voltage at U12 pin 2 comes up to 3.0 V, the $\overline{\text{RESET}}$ output of U12 at pin 5 goes low for 195 ms. External timing capacitor C5 determines the time $\overline{\text{RESET}}$ stays low. Capacitor C6 at U12 pin 1 (REF) prevents fast power supply transients from causing resets. The low $\overline{\text{RESET}}$ turns off Q1 and Q2C. The collector of Q2C is set to 0 V through R7, setting the RESET input to the Microprocessor low and turning off Q2B and Q2A. The RESET input to the Microprocessor must stay low for at least 100 ms for a valid reset. The $\overline{\text{RESET}}$ output of U12 is open collector. After 195 ms $\overline{\text{RESET}}$ goes high and is set to +0.8 V by VR1, R1, and R12, turning on Q1 and Q2C. The collector of Q2C goes to +5 V, setting the RESET input to the Microprocessor high, turning on Q2B and setting the base of Q2A to +5 V. With Q2B on, Q2D is turned on, and the +5 V supply is applied to the RAM's Vcc input. The cathode of CR2 becomes more positive than its anode and CR2 is turned off, isolating B1 from the +5 V supply. The high RESET input to the Microprocessor starts its power-up routine. Address Decoder U48A (refer to Service Sheet 18) sets RAM SELECT ENABLE low. Q2A is turned on and its collector goes to 0 V. RAM SELECT is low and the RAM U24 (refer to Service Sheet 19) is enabled.

Interrupt Processing

Two methods are employed to interrupt normal program execution, namely maskable and nonmaskable interrupts. When either type of interrupt is detected, the Microprocessor finishes executing its current instruction before program execution is directed to the respective interrupt subroutine.

Maskable interrupts occur whenever a key on the keyboard is pressed, a reverse-power condition is detected, or an active-low switch closure is applied through the rear-panel sequence connector JX. Whenever one of these conditions is detected and latched, the Microprocessor's Interrupt Request input line (IRQ at U14 pin 4) is forced active (low). The Microprocessor then examines (via the data bus) the contents of the Service Request Register U11. The Microprocessor can then determine which one of the three maskable interrupts has occurred. U11 functions as a 3-state buffer. During program execution of the maskable interrupt subroutine, the Microprocessor first checks for a reverse-power interrupt (D7 active low), then a sequence interrupt (D1 and D2 active low), and finally a keyboard interrupt (D2 active low). The methods used to detect and latch the three maskable interrupts are discussed in the following paragraphs.

Keyboard Interrupt

Whenever one of the keys on the Keyboard Assembly A1 is pressed, a keyboard interrupt KIN(L) is issued to the Microprocessor Assembly A13 (refer to Service Sheet 21). This active-low interrupt is applied to connector J12 pin 8 and then gated through U23A and U23B to a direct-set flip-flop U22A causing the output at U22 pin 6 to go low. This flip-flop debounces the leading edge of KIN and latches the occurrence of the keyboard interrupt. The latched keyboard interrupt is gated through U23C and the enabled, 3-state buffer U9C to generate an interrupt request IRQ(L). U9C is enabled at U9C pin 10 through the inverting driver U21C as long as rocker switch S1C is set to NRM.

When the key is released, KIN is high and U23A pin 1 is pulled high by resistor R28. After an approximate 33 ms delay produced by the RC network of R31 and C2, capacitor C2 charges to pull U23A pin 2 high. This delay debounces the trailing edge of KIN. Once the keyboard interrupt is processed, the Microprocessor issues and decodes hexadecimal address 01FB to clock U22A clear by the KIC input. Clearing U22A clears the keyboard interrupt.

Reverse-Power Interrupt

A reverse-power interrupt RPI(L) occurs when a reverse power condition is detected and latched by the reverse-power-sense circuitry on the Output Assembly A6 (refer to Service Sheet 8). This active-low interrupt is applied through the feedthrough capacitor C16 to connector A13J9 pin 12. Normally, with no interrupt present, U23C pin 9 is pulled high through resistor R27. When a reverse-power interrupt occurs, it is gated through U23C and the enabled 3-state buffer U9C to generate an interrupt request IRQ(L). U9C is enabled at U9C pin 10 through the inverting driver U21C as long as rocker switch S1C is set to NRM.

Sequence Interrupt

A sequence interrupt SQI(L) occurs when an active-low switch closure is applied through the rear-panel connector J5 to connector A13 J5 pin 7. This interrupt is handled in much the same manner as the keyboard interrupt. Normally, with no interrupt present, U21A pin 1 is pulled high through resistor R5. A 33 ms delay is produced by the RC network of R29 and C24 to debounce the leading edge of SQI. When a sequence interrupt occurs, it is gated through U23B pin 5 to direct-set flip-flop U22A causing the output at U22A pin 6 to go low. This flip-flop latches the occurrence of the sequence interrupt. The latched-sequence interrupt is gated through U23C and the enabled 3-state buffer U9C to generate an interrupt request IRQ(L). U9C is enabled at U9C pin 10 through the inverting driver U21C as long as rocker switch S1C is set to NRM.

When the switch closure is removed, U21A pin 1 is pulled high as soon as capacitor C24 charges. The delay produced by the RC network of R29 and C24 debounces the trailing edge of SQI. Once

the sequence interrupt is processed, the Microprocessor clears. Clearing U22A clears the sequence interrupt.

The Microprocessor's Non-Maskable Interrupt input line (NMI at U14 pin 6) is normally pulled high through resistor R13. During signature analysis troubleshooting, this edge-triggered line is momentarily grounded to abort normal program execution and to direct program execution to the non-maskable, interrupt subroutine.

In addition to buffering the three maskable interrupts, the Service Request Register U11 also buffers four status lines which monitor various instrument conditions. These conditions include the state of the LF Loop Out-Of-Lock LFR(H) line (refer to Service Sheet 11), the state of the HI(H) and LO(H) lines from the Over and Under Modulation Comparators (refer to Service Sheet 7), the state of the HP-IB Interrupt Request IBI(L) line (refer to Service Sheet 20), and the state of the Doubler Interrupt X2I(L). During normal program execution, the Microprocessor strobes the contents of U11 onto the data bus. If one of these four conditions is active when the Microprocessor strobes U11, it executes the necessary instructions to service the interrupt condition.

Doubler Detector Sample And Hold

The Doubler's ALC Loop detector voltage is sampled and stored prior to pulse modulation being turned on when the output frequency is in the doubled band 1030 MHz to 2060 MHz. When pulse modulation turns off RF Output, the Doubler's ALC Loop would go into saturation. A power spike would be output when the RF Output was turned back on. The Output power spike is prevented by sampling the ALC Loop detector voltage. Open the ALC Loop and set the Doubler's level DAC until the detector voltage (RF Output Level) is at the closed loop voltage before Pulse Modulation is turned before Pulse Modulation is turned on.

The ALC Loop's detector voltage X2ANBUS (Doubler Analog Bus) is input on J1 Pin 10 to sampler U2. The input voltage is sampled when the control input X2 SAM (doubler Sample) is set low. See Service Sheet 18. The sampled voltage is stored on Sample/Hold capacitor C1. Next the Doubler's ALC Loop is opened, serial data is sent to the Doubler's level DAC to adjust the Output. The output level is adjusted until the Loop's detector voltage is equal to the voltage sampled and stored on capacitor C1. After each write to the Doubler's level DAC, the sampled voltage stored on C1 is compared with the current detector voltage X2ANBUS by comparator U1. The comparison result is placed on Data Bus Line D0 when control input X2DETIE (Doubler Detector Input enable) is set low turning U9G on. The process is repeated until the detector's open-loop voltage equals the detector's closed loop voltage stored on C1.

A13 Component Coordinates

COMP	X	Y	COMP	X	Y	COMP	X	Y
B1	C	2	J12	D	2	U11	B	2
			J13	D	2	U12	C	3
C1	A	3				U13	C	2
C2	A	3	Q1	C	3	U14	D	2
C3	A	3	Q2	C	2	U15	D	2
C4	C	3				U16	D	2
C5	C	3	R1	B	3	U17	D	2
C6	C	3	R2	B	3	U18	A	2
C7	D	3	R3	C	3	U19	A	2
C8	D	3	R4	C	3	U20	A	2
C9	D	3	R5	C	3	U21	B	2
C10	A	3	R6	C	3	U22	B	2
C11	B	3	R7	C	3	U23	B	2
C12	B	3	R8	C	3	U24	B	2
C13	C	3	R9	C	3	U25	C	2
C14	A	2	R10	C	3	U26	C	2
C15	B	2	R11	C	3	U27	C	2
C16	B	2	R12	C	3	U28	C	2
C17	C	2	R13	A	2	U29	D	2
C18	C	2	R14	A	2	U30	D	2
C19	C	2	R15	A	2	U31	D	2
C20	D	2	R16	A	2	U32	A	1
C21	A	2	R17	A	2	U33	A	1
C22	A	2	R18	A	2	U34	A	1
C23	A	2	R19	A	2	U35	A	1
C24	B	2	R20	A	2			
C25	B	2	R21	A	2	VR1	C	3
C26	D	2	R22	A	2	VR2	A	2
C27	A	1	R23	A	2	VR3	A	2
			R24	A	2	VR4	A	2
CR1	C	3	R25	A	2	VR5	A	2
CR2	C	3	R26	B	2	VR6	A	2
			R27	B	2			
DS1	A	2	R28	B	2	Y1	D	3
DS2	A	2	R29	B	2			
DS3	A	2	R30	B	2			
DS4	A	2	R31	B	2			
DS5	A	2						
			S1	A	2			
J1	A	3						
J2	A	3	U1	A	3			
J3	A	3	U2	A	3			
J4	A	3	U3	A	3			
J5	A	1	U4	D	3			
J6	A	1	U5	A	2			
J7	A	1	U6	A	2			
J8	A	1	U7	A	2			
J9	C	1	U8	B	2			
J10	D	1	U9	B	2			
J11	D	2	U10	B	2			

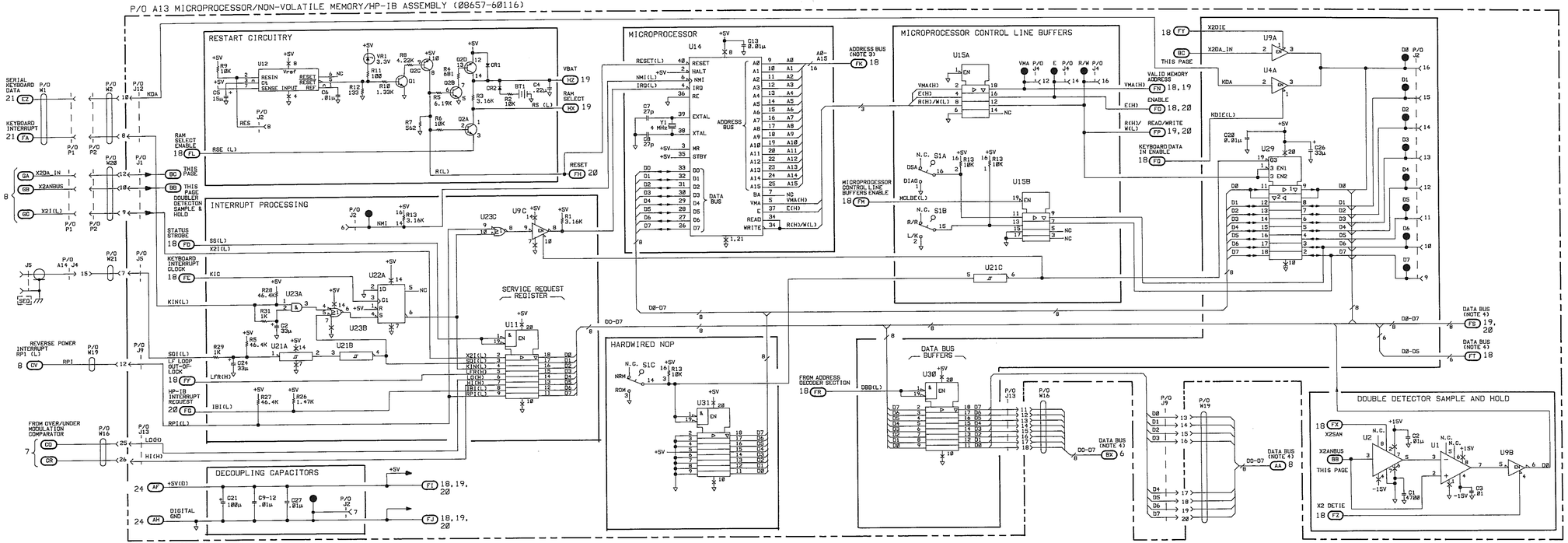


Figure 1
Service Sheet 17 7

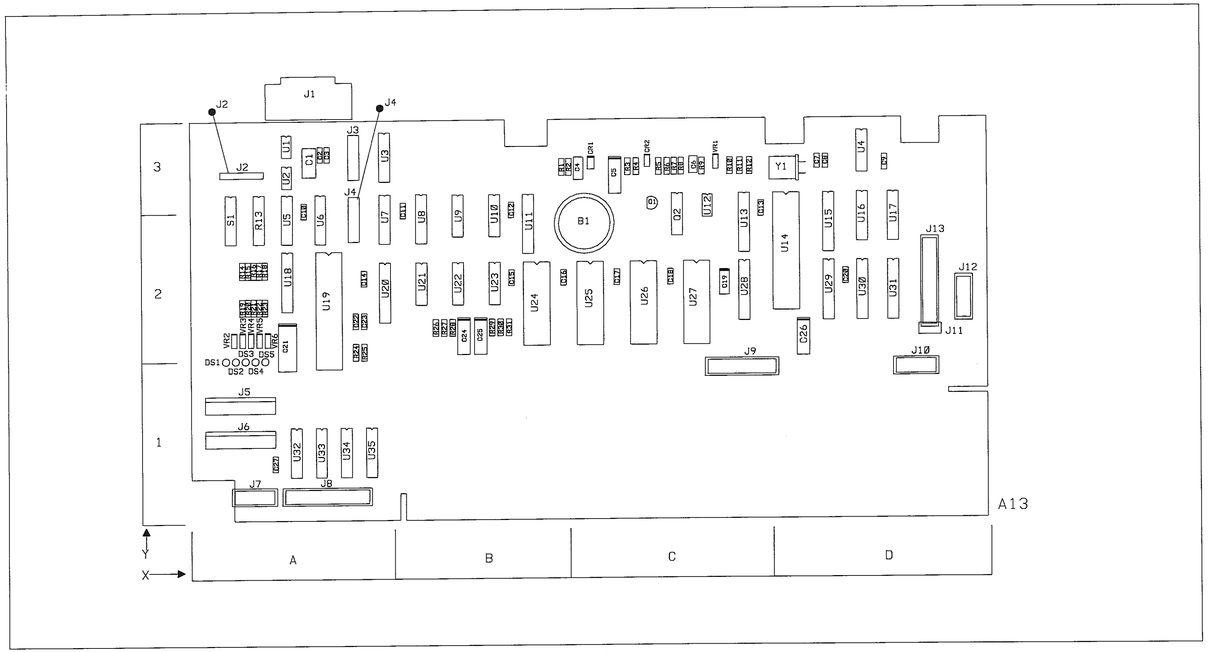


Figure Ø. Service Sheet 18 Information.

Component Locator

NOTES

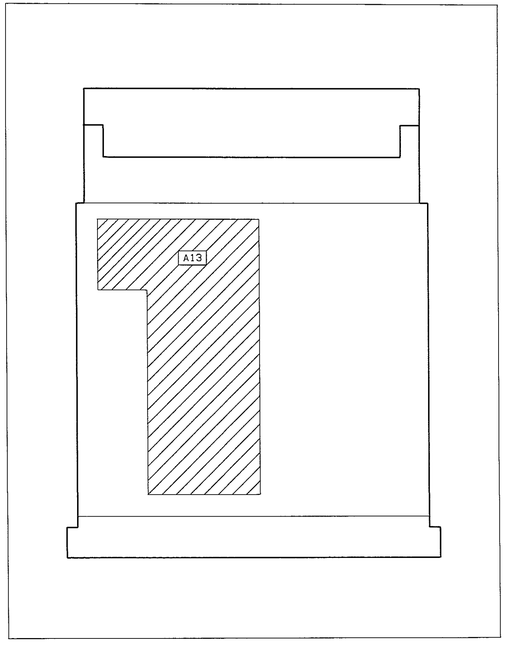
1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" In Section 8.
2. Address data is transferred positive true from the microprocessor on the unidirectional buffered address bus.

LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
IS MORE NEG. THAN IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A13 — MICROPROCESSOR, INTERRUPT PROCESSING AND RESTART — SS17

SEE REVERSE SIDE



Service Sheet 18

ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL

PRINCIPLES OF OPERATION

General

The circuits of Service Sheet 18 control the major functions of the Signal Generator. This circuitry has direct control on almost all of the analog functions of the instrument; such as frequency, amplitude, and modulation. Address data from the Microprocessor is decoded; the accompanying data from the data bus (either series or parallel) is manipulated to set various output modes, levels, and frequencies. In addition, many functions that are strictly digital (such as control of keyboard, display, and data bus) are decoded by the Address Decoders.

Address Decoders

There are three De-multiplexers, (U5, U6, U17), used to decode the address lines A0, A1, and A2. Address lines A3 and A4 are decoded by U8B to activate any of the three de-multiplexers. The ouput at U8B pin 10 controls de-mux U5, U5 will turn on when U5-6 is active high and U5-4 and 5 are active low. The output at U8B pin 11 controls de-mux U6, U6 will turn on when U6-6 is active high and U6-4 and 5 are active low. The output of U8B pin 9 controls de-mux U17, U17 will turn on when U17-6 is active high and U17-4 and 5 are active low.

Address lines A0, A1, and A2 are decoded into control lines. U5 decodes the address lines to activate other control functions in the A13 Microprocessor. U6 decodes the lines to control modulation, attenuation and other various functions.

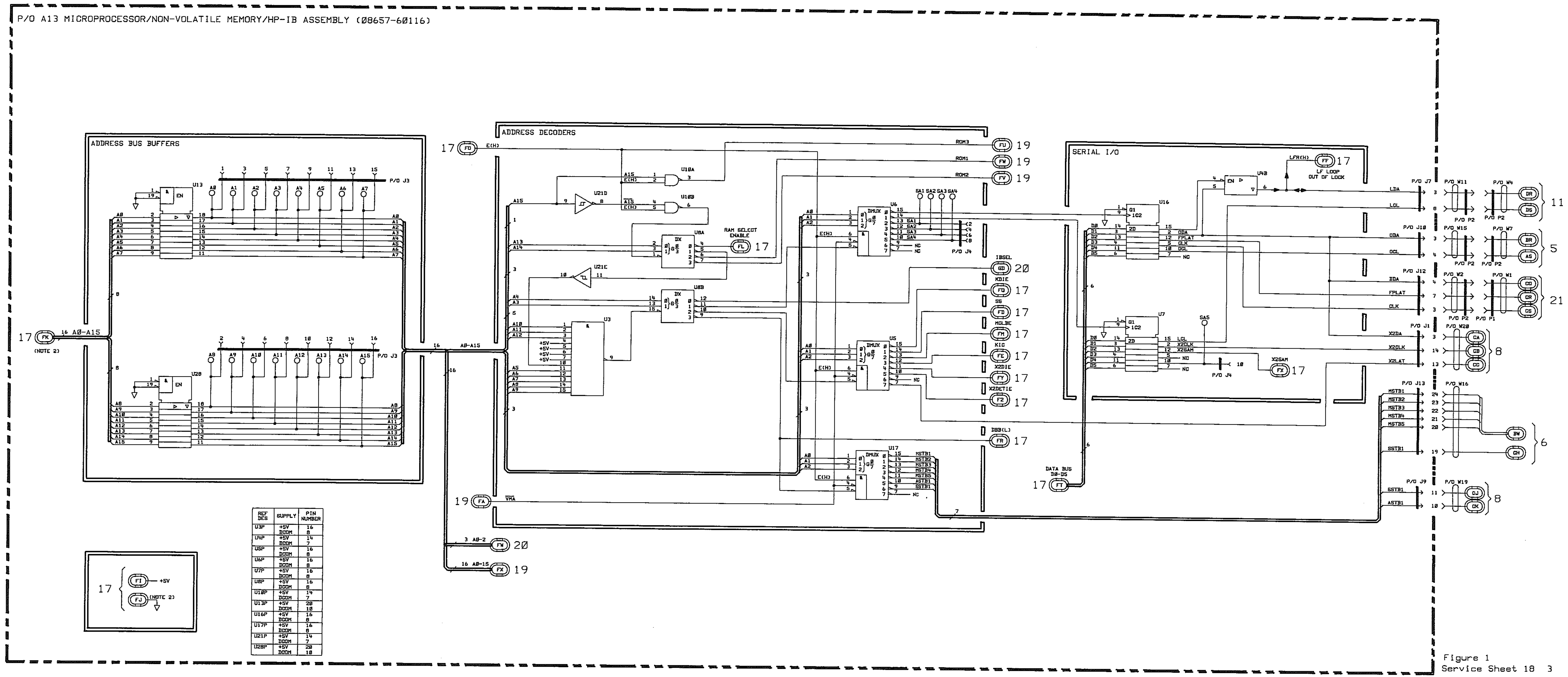
Serial I/O Control

Serial I/O is composed of two control registers, U7 and U16. Control registers U7 and U16 are activated by controls lines from De-multiplexer U6 pins 14 and 15.

Control registers U7 and U16 translate serial data bus information from data bus lines D0 through D5 into instrument control functions. The control functions are used for the output section, doubler module and fractional N control.

A13 Component Coordinates

COMP	X	Y	COMP	X	Y	COMP	X	Y
B1	C	2	J12	D	2	U11	B	2
			J13	D	2	U12	C	3
C1	A	3				U13	C	2
C2	A	3	Q1	C	3	U14	D	2
C3	A	3	Q2	C	2	U15	D	2
C4	C	3				U16	D	2
C5	C	3	R1	B	3	U17	D	2
C6	C	3	R2	B	3	U18	A	2
C7	D	3	R3	C	3	U19	A	2
C8	D	3	R4	C	3	U20	A	2
C9	D	3	R5	C	3	U21	B	2
C10	A	3	R6	C	3	U22	B	2
C11	B	3	R7	C	3	U23	B	2
C12	B	3	R8	C	3	U24	B	2
C13	C	3	R9	C	3	U25	C	2
C14	A	2	R10	C	3	U26	C	2
C15	B	2	R11	C	3	U27	C	2
C16	B	2	R12	C	3	U28	C	2
C17	C	2	R13	A	2	U29	D	2
C18	C	2	R14	A	2	U30	D	2
C19	C	2	R15	A	2	U31	D	2
C20	D	2	R16	A	2	U32	A	1
C21	A	2	R17	A	2	U33	A	1
C22	A	2	R18	A	2	U34	A	1
C23	A	2	R19	A	2	U35	A	1
C24	B	2	R20	A	2			
C25	B	2	R21	A	2	VR1	C	3
C26	D	2	R22	A	2	VR2	A	2
C27	A	1	R23	A	2	VR3	A	2
			R24	A	2	VR4	A	2
CR1	C	3	R25	A	2	VR5	A	2
CR2	C	3	R26	B	2	VR6	A	2
			R27	B	2			
DS1	A	2	R28	B	2	Y1	D	3
DS2	A	2	R29	B	2			
DS3	A	2	R30	B	2			
DS4	A	2	R31	B	2			
DS5	A	2						
			S1	A	2			
J1	A	3						
J2	A	3	U1	A	3			
J3	A	3	U2	A	3			
J4	A	3	U3	A	3			
J5	A	1	U4	D	3			
J6	A	1	U5	A	2			
J7	A	1	U6	A	2			
J8	A	1	U7	A	2			
J9	C	1	U8	B	2			
J10	D	1	U9	B	2			
J11	D	2	U10	B	2			



REF DES	SUPPLY	PIN NUMBER
U3P	+5V DCOM	16 8
U4P	+5V DCOM	14 7
U5P	+5V DCOM	16 8
U6P	+5V DCOM	16 8
U7P	+5V DCOM	16 8
U8P	+5V DCOM	16 8
U10P	+5V DCOM	14 7
U13P	+5V DCOM	20 10
U16P	+5V DCOM	16 8
U17P	+5V DCOM	16 8
U21P	+5V DCOM	14 7
U28P	+5V DCOM	20 10

Figure 1
Service Sheet 18 3

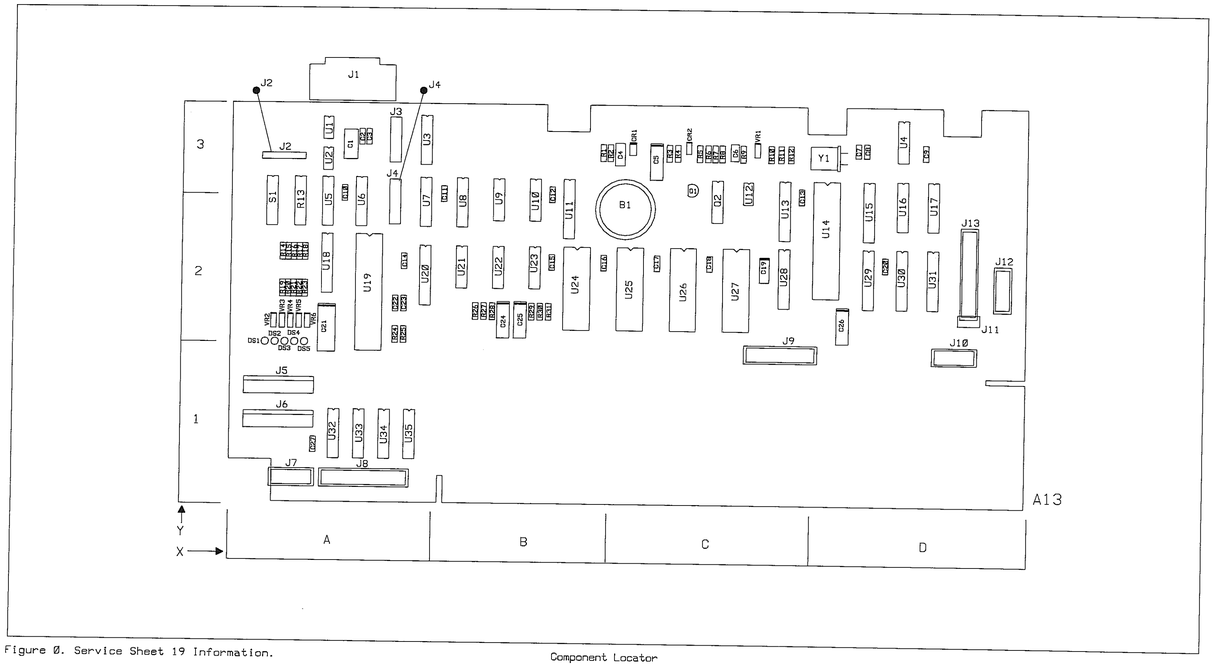


Figure Ø. Service Sheet 19 Information.

Component Locator

NOTES:

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Data is transferred positive true from ROM or RAM memory to the microprocessor on the data bus (DØ-D7).
3. Address data is transferred positive true from the microprocessor on the buffered address bus (AØ-A14).

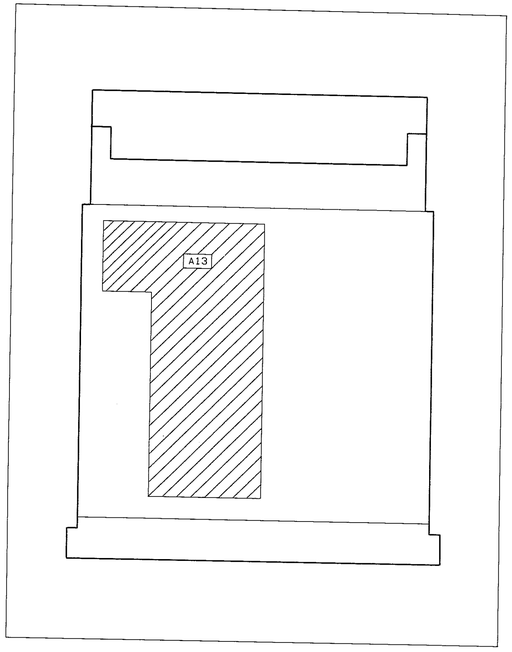
LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
IS MORE NEG. THAN IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A13 — SEE REVERSE SIDE

ADDRESS BUFFERING AND DECODING SERIAL I/O AND CONTROL

SS18



Service Sheet 19

MEMORY

PRINCIPLES OF OPERATION

General

The Signal Generator's internal memory consists of 2k bytes of random access memory (RAM) and 32k bytes of read only memory (ROM). The RAM utilizes a battery back-up whenever the Signal Generator is unplugged or in standby. This saves the contents of the RAM until power is restored.

RAM

Valid Memory Address (VMA) and RAM Select (RS) inputs enable RAM U24. VMA is inverted to VMA(L) by U21F before being applied to the RAM's enable input. The read/write mode is selected by a control signal to U24 pin 27. The memory location of the RAM is selected by addresses A0 through A12. The RAM data input/output is connected directly to the data bus D0 through D7. Vbat is connected to the RAM Vcc input at U24 pin 28. When the Signal Generator is ON, the Vbat input is equal to the +5V supply voltage. When the Signal Generator is in unplugged or in STBY, Vbat is approximately +2.65 Vdc.

ROM

Each ROM is enabled by a low VMA(L) inverted by U21F, and a low ROM 1, ROM 2, or ROM 3 enable pin 20 of U25, U26, and U27. The memory location of the ROM 1 is selected by addresses A0 through A14, ROM 2 and ROM 3 by addresses A0 through A12. The ROM data output is connected directly to the data bus D0 through D7. ROM 1, ROM 2, and ROM 3 enable inputs are decoded from addresses A13, A14, and A15 by U8A (refer to Service Sheet 18).

TROUBLESHOOTING USING KEYBOARD-INVOKED TEST 5

Troubleshooting is done to the circuits of Service Sheet 19 when a defect seems to be related to the ROM or RAM circuits. The ROM troubleshooting information provided is firmware initiated tests on power-on, and keyboard-invoked tests. If nothing definite is discovered in performing these checks, refer to Service Sheet 17 or consider the other possibilities listed on Block Diagram 4.

Test 1. Microprocessor and RAM/ROM Functional Checks

The Microprocessor and RAM/ROM Functional Checks verify that ROM and RAM are correctly operating. The following procedure may help to identify any problems in the ROM, RAM, or in the supporting circuitry.

1. Verify enabling of ROM by checking that A13U21F-12 (VMA), A13U26-20 (ROM), and A13U27-20 (ROM) toggle.
2. When the POWER switch is set to ON an internal memory check is initiated. If a memory failure is detected, a RAM or ROM error code is shown in the FREQUENCY Display window. The error code remains displayed until any front-panel key is pressed. Refer to Table 1 for the codes and the respective faults.

Table 1. Power-On Error Codes.

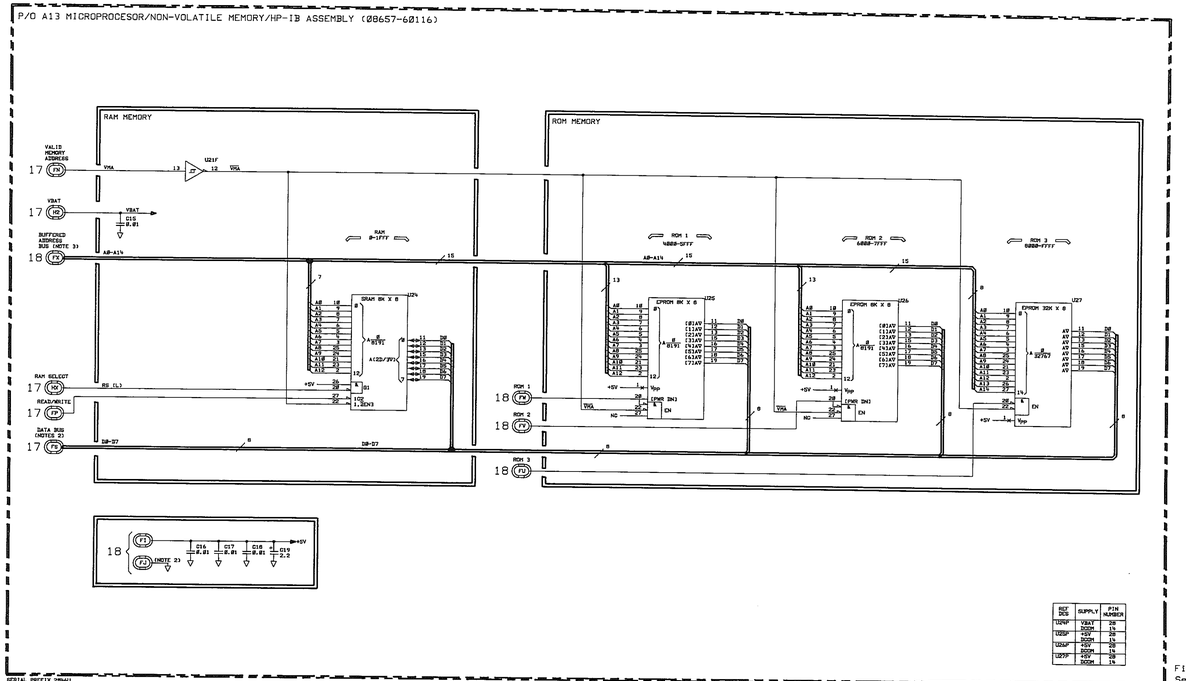
Error Code	Faulty Device	Location
1000	RAM Error	A13-U24
0100	ROM1 Error	A13-U25
0010	ROM2 Error	A13-U26
0001	ROM3 Error	A13-U27

The ROM can be checked by entering the Keyboard-Invoked Test subroutine Test 5. Checksums with the ROM are checked and an error code is displayed if appropriate. The test will halt if a failure occurs after checking the entire memory. If an error does not occur, the test is repeated and a pass number in the AMPLITUDE Display is incremented.

- Enter the Keyboard-Invoked Tests by first pressing the **SHIFT** key, and then pressing the **INCR SET** key.
- Press the **AMPTD** ⇧ key until a "5" is shown in the MODULATION Display window. Test 5, ROM Test, is ready to run.
- Press the **INCR SET** key to start the test. The test will repeat until stopped.
- If the ROM is malfunctioning, error code "50" will be shown in the FREQUENCY Display window.
- Press the **AMPTD** ⇧ key to stop the test.
- To exit the Keyboard-Invoked Tests, press the **AMPTD** ⇧ key until a "7" is displayed in the MODULATION Display window. Then press the **INCR SET** key; the Signal Generator is initialized as in Power-On.

A13 Component Coordinates

COMP	X	Y
B1	C	2
C1	A	3
C2	A	3
C3	A	3
C4	C	3
C5	C	3
C6	C	3
C7	D	3
C8	D	3
C9	D	3
C10	A	3
C11	B	3
C12	B	3
C13	C	3
C14	A	2
C15	B	2
C16	B	2
C17	C	2
C18	C	2
C19	C	2
C20	D	2
C21	A	2
C22	A	2
C23	A	2
C24	B	2
C25	B	2
C26	D	2
C27	A	1
CR1	C	3
CR2	C	3
DS1	A	2
DS2	A	2
DS3	A	2
DS4	A	2
DS5	A	2
J1	A	3
J2	A	3
J3	A	3
J4	A	3
J5	A	1
J6	A	1
J7	A	1
J8	A	1
J9	C	1
J10	D	1
J11	D	2
J12	D	2
J13	D	2
Q1	C	3
Q2	C	2
R1	B	3
R2	B	3
R3	C	3
R4	C	3
R5	C	3
R6	C	3
R7	C	3
R8	C	3
R9	C	3
R10	C	3
R11	C	3
R12	C	3
R13	A	2
R14	A	2
R15	A	2
R16	A	2
R17	A	2
R18	A	2
R19	A	2
R20	A	2
R21	A	2
R22	A	2
R23	A	2
R24	A	2
R25	A	2
R26	B	2
R27	B	2
R28	B	2
R29	B	2
R30	B	2
R31	B	2
S1	A	2
U1	A	3
U2	A	3
U3	A	3
U4	D	3
U5	A	2
U6	A	2
U7	A	2
U8	B	2
U9	B	2
U10	B	2
U11	B	2
U12	C	3
U13	C	2
U14	D	2
U15	D	2
U16	D	2
U17	D	2
U18	A	2
U19	A	2
U20	A	2
U21	B	2
U22	B	2
U23	B	2
U24	B	2
U25	C	2
U26	C	2
U27	C	2
U28	C	2
U29	D	2
U30	D	2
U31	D	2
U32	A	1
U33	A	1
U34	A	1
U35	A	1
VR1	C	3
VR2	A	2
VR3	A	2
VR4	A	2
VR5	A	2
VR6	A	2
Y1	D	3



REF DES	SUPPLY	PIN NUMBER
U2N*	VBAT	28
	ROM	14
U22*	+5V	28
	ROM	14
U23*	+5V	28
	ROM	14
U27*	+5V	28
	ROM	14

Figure 1
Service Sheet 19 5

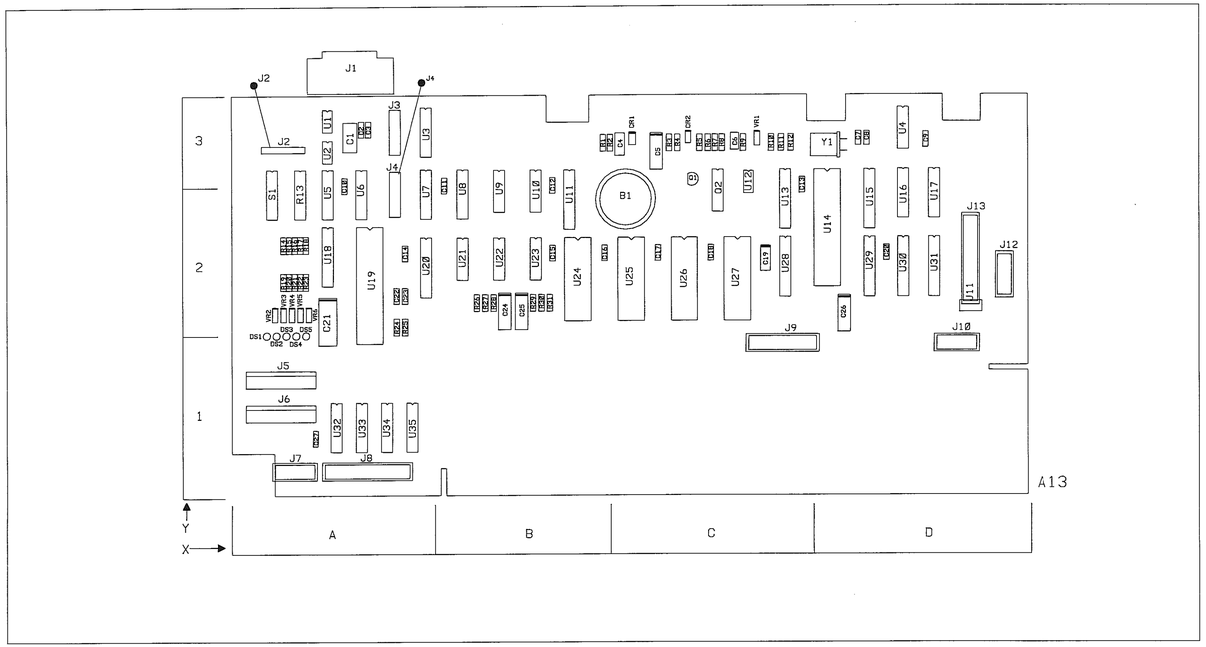


Figure Ø. Service Sheet 2Ø Information.

Component Locator

NOTES

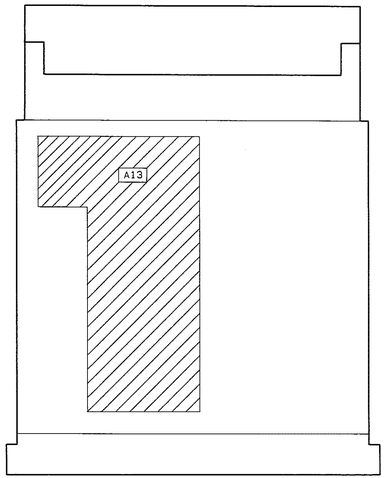
1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. HP-IB addresses greater then 3Ø are invalid.
3. HP-IB chassis ground is achieved by W18J7 pin 12, 18 thru 24 connection and mechanical contact through nuts holding PC board to cover.
4. Data transferred on the data bus (DØ-D7) is positive true.
5. Data transferred on the data input/output bus (DIØ1-DIØ8) is negative true.

LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
IS MORE NEG. THAN IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A13 MEMORY SS19

SEE REVERSE SIDE



Service Sheet 20

HP-IB INTERFACE

PRINCIPLES OF OPERATION

General

Inputs to the Signal Generator from the external controller are in the form of encoded control and data information. Control information is input to the Signal Generator via five control lines (four are used in this instrument) and three handshake lines. The control lines allow the controller to gain the Signal Generator's attention and impart other appropriate control information. The handshake lines provide asynchronous control information for data transfer between a talker (computer controller) and the listener (Signal Generator).

In the handshake mode, the Signal Generator first indicates when it is ready to listen (receive data). The controller responds by indicating when the data that appears on the data lines, DI01 through DI08, is valid. The Signal Generator then indicates to the controller when the data has been accepted.

Data transferred to the Signal Generator contains all the information required to control each mode of operation. It also contains the level or frequency information for each mode; for example, an AM depth of 50%, an RF output amplitude of −10 dBm, and a frequency of 100 MHz.

The HP-IB Address Switch Buffer U18 sends the Signal Generator's internally-set HP-IB address to U19 via the data lines when enabled by the HP-IB General Purpose Interface Adapter U19. The HP-IB Interface Buffer, U20, is enabled when IB Sel (pin 19) goes low. The Read/Write mode determines if data is written onto or read from the Data Bus. Note that the Read/Write line is tied in parallel to the HP-IB Interface Buffer U20, and the HP-IB Interface Adapter U19.

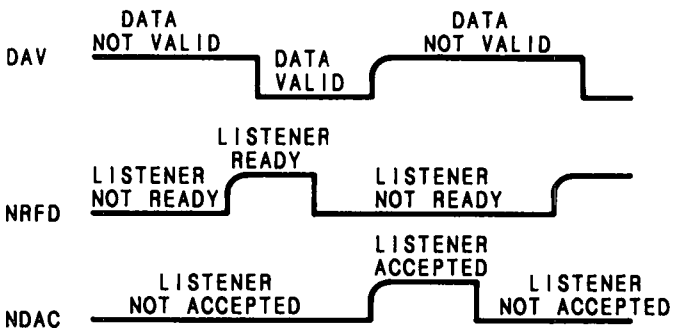
HP-IB Data Bus and Control/Handshake Buffers

The HP-IB Data Bus and Control/Handshake Buffers (U32, 33, 34, and 35) are permanently enabled by hard-wire connections to ground. The HP-IB Data Bus output buffers are disabled (pins 3, 5, 11 and 13 of U32, U33, and U34 are tied high) since the Signal Generator functions as a listener only. The Signal Generator does not have the capability to issue a service request (SRQ). The handshake control lines output only the NRFD and NDAC. See Figure 1 for more information about the HP-IB Handshake Control.

HP-IB Interface Adapter

The U19 Interface Adapter provides the interface between the HP-IB external controller and the Signal Generator's digital circuits. The Address Select Enable, ASE (L),and HP-IB Interrupt Request, IBI (L), are generated as a result of inputs from the external controller.

The Microprocessor, under the control of the HP-IB subroutines stored in ROM, outputs control and address signals to U19 to control the data input from the external controller. Interface Bus Select, IB SEL (L), selects the HP-IB mode. A0, A1, and A2 input the addressing to the register select lines RS0, RS1, and RS2 of U19. Data and control information is thus selected to flow to and from the Microprocessor circuits on the data bus. Read/Write, R(H)/W(L), determines if data is written onto the data lines D0 through D7 or if the internal address is read by U19.



Start with the talker waiting for the listener to release NRFD (not ready for data) indicating it is ready.

When the listener is ready, NRFD goes high (false). The talker then places valid data on DIO1 through DIO8 and sets DAV (data valid) low (true).

NRFD then goes low (true) and the talker waits for the listener to indicate it has accepted the data (or ignored it) by releasing the NDAC (not data accepted) to a high (false, i.e., data is accepted).

The talker sets DAV high (false) and again waits for the listener to release NRFD.

(NOTE that if ATN is true, all instruments on the bus must handshake regardless of whether they are talkers, listeners, or bystanders. Being in remote or local has nothing to do with handshaking. If ATN is false, they only handshake if addressed.)

Figure 1. *Simplified HP-IB Handshake between a Talker (Computer Controller) and One Listener (Signal Generator).*

A13 Component Coordinates

COMP	X	Y
B1	C	2
C1	A	3
C2	A	3
C3	A	3
C4	C	3
C5	C	3
C6	C	3
C7	D	3
C8	D	3
C9	D	3
C10	A	3
C11	B	3
C12	B	3
C13	C	3
C14	A	2
C15	B	2
C16	B	2
C17	C	2
C18	C	2
C19	C	2
C20	D	2
C21	A	2
C22	A	2
C23	A	2
C24	B	2
C25	B	2
C26	D	2
C27	A	1
CR1	C	3
CR2	C	3
DS1	A	2
DS2	A	2
DS3	A	2
DS4	A	2
DS5	A	2
J1	A	3
J2	A	3
J3	A	3
J4	A	3
J5	A	1
J6	A	1
J7	A	1
J8	A	1
J9	C	1
J10	D	1
J11	D	2
J12	D	2
J13	D	2
Q1	C	3
Q2	C	2
R1	B	3
R2	B	3
R3	C	3
R4	C	3
R5	C	3
R6	C	3
R7	C	3
R8	C	3
R9	C	3
R10	C	3
R11	C	3
R12	C	3
R13	A	2
R14	A	2
R15	A	2
R16	A	2
R17	A	2
R18	A	2
R19	A	2
R20	A	2
R21	A	2
R22	A	2
R23	A	2
R24	A	2
R25	A	2
R26	B	2
R27	B	2
R28	B	2
R29	B	2
R30	B	2
R31	B	2
S1	A	2
U1	A	3
U2	A	3
U3	A	3
U4	D	3
U5	A	2
U6	A	2
U7	A	2
U8	B	2
U9	B	2
U10	B	2
U11	B	2
U12	C	3
U13	C	2
U14	D	2
U15	D	2
U16	D	2
U17	D	2
U18	A	2
U19	A	2
U20	A	2
U21	B	2
U22	B	2
U23	B	2
U24	B	2
U25	C	2
U26	C	2
U27	C	2
U28	C	2
U29	D	2
U30	D	2
U31	D	2
U32	A	1
U33	A	1
U34	A	1
U35	A	1
VR1	C	3
VR2	A	2
VR3	A	2
VR4	A	2
VR5	A	2
VR6	A	2
Y1	D	3

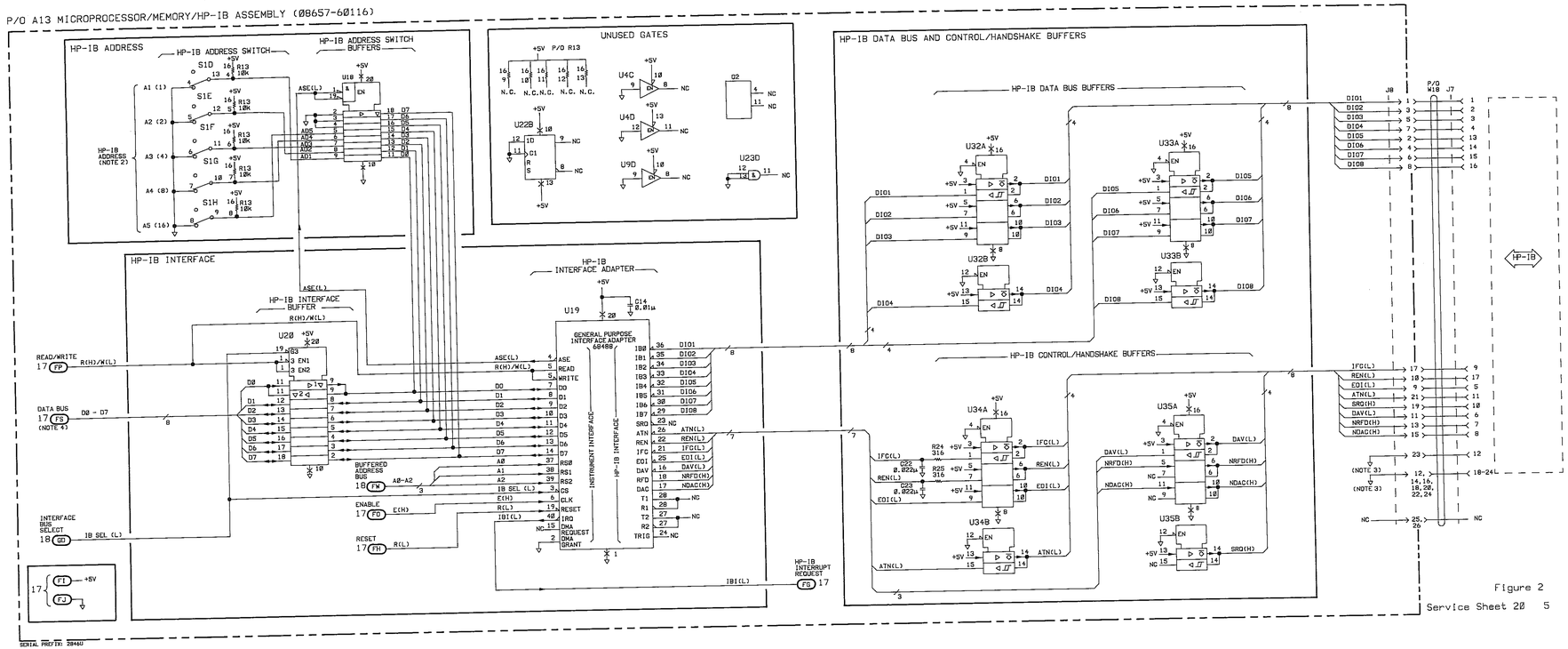


Figure 2

Service Sheet 20 5

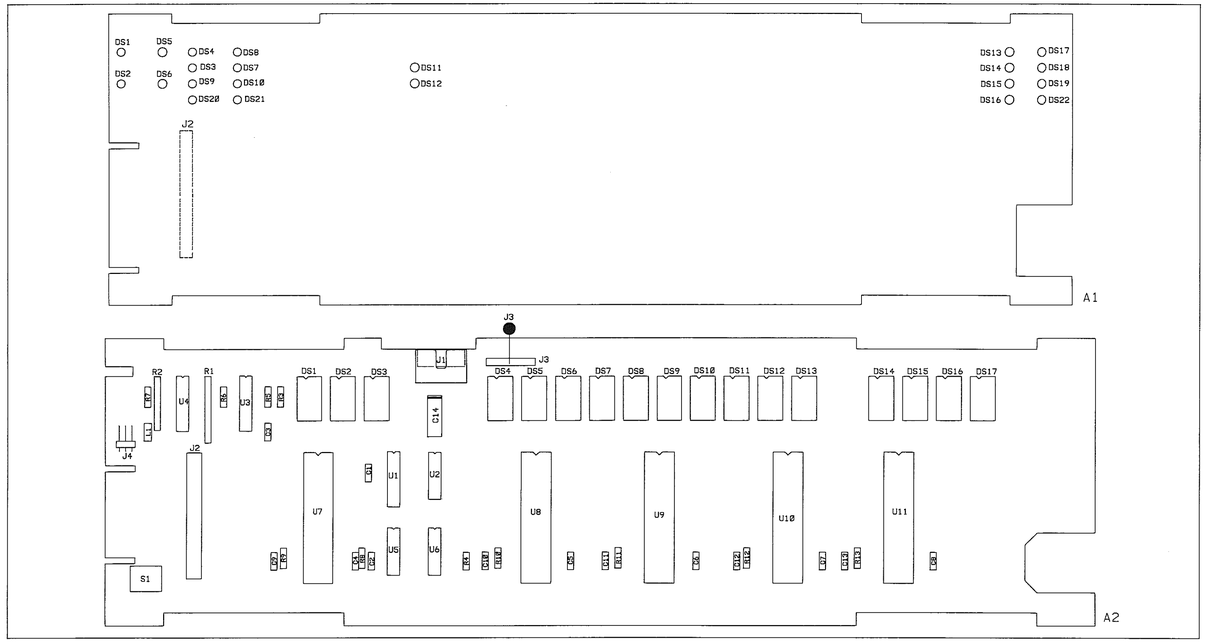


Figure Ø. Service Sheet 21 Information.

Component Locator

NOTES

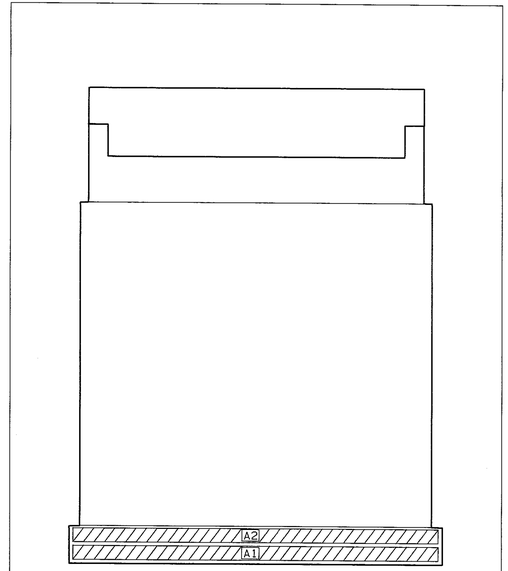
1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. A1 chassis ground is achieved by A1J1-16 connection and mechanical contact through nuts holding PC board to frame.
3. A2 chassis ground is achieved by A2J1-16 connection and mechanical contact through nuts holding PC board to frame.
4. Second functions (blue) are activated by first pressing the blue "SHIFT" key.
5. Pressing "SHIFT" and then "DIAG" (Incr Set) activates the Keyboard Invoked Tests. These tests are referred to in troubleshooting procedures.

LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	0.8V	1.5V
IS MORE NEG. THAN IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A13 HP-IB INTERFACE SS2Ø

SEE REVERSE SIDE



Service Sheet 21

KEYBOARD AND ENCODER

PRINCIPLES OF OPERATION

Keyboard Encoding (A1 and A2)

The Keyboard Assembly, A1, is composed of 48 keys. They are hard-wired in an 8-row by 6-column matrix. With no keys pressed, each of the 8-row lines are pulled high (+5V) through an 22k ohm resistor A2R1 and each of the 6-column lines are pulled low (0V) through an 100k ohm resistor A2R2. The resultant keyboard data is shown in Table 1.

Whenever a key is pressed, a row line is connected to a column line through the dividing network of the 22k ohm and 100k ohm resistors (located on the Display Assembly A2). As long as the key remains pressed, the column line remains high and the keyboard interrupt remains issued to the Microprocessor by the Keyboard Interrupt Generator U6.

When the Microprocessor is interrupted, it enters its keyboard-read subroutine. The KSTB1, KSTB2 and RKRD latched bits of U1 are low. When the microprocessor receives the KIN (keyboard interrupt), serial data is clocked from the microprocessor into U1. Data is clocked in by the low to high transition of the CLK. The data is latched to the output by the low to high transition of the LATCH input. The first high serial data bit is latched and the KSTB1 output is switched from low to high. The KSTB1 low to high transition strobes the data bits found on Col 1 through Col 6 are read into the Key Column Data Latch/Shift Register U4. Once keyed the column data will consist of five low bits (refer to Table 1 and Service Sheet 21) and one bit strobed high that corresponds to the key column pressed.

Table 1. Keyboard Data (KDA) With No Keys Pressed.

Column Data (A2U4)							Row Data (A2U3)							
Pin Number	11	12	13	14	3	4	11	12	13	14	3	4	5	6
Keyboard Data	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Once the column data is latched, the Microprocessor sends another high serial data bit. The Read Key Row Data (RKRD) signal is set high forcing all 6-column lines low so that the row data can be read. When the column lines are all forced low, the row line associated with the pressed key is also forced low. (Forcing the column lines low also disables the keyboard interrupt.) Next the microprocessor sends the third high serial data bit to U1, and keyboard strobe (KSTB2) is set from low to high. The keyboard strobe (KSTB2) strobes Row 1 through Row 8 data into the Key Row Data Latch/Shift Register U3. The row data consists of seven high bits and one strobed low bit. The low bit is in the bit position that is associated with the row of the pressed key. The Microprocessor is now ready to receive keyboard data via the Serial Keyboard Data line (KDA). A parallel-to-serial conversion takes place as each row bit is shifted out of U3 (pin 9), and each column bit is shifted out of U4 (pin 9) into U3 (pin 10). After 16 keyboard clocks (KCL), all 16 bit of keyboard data is shifted to the Microprocessor. If the **FREQUENCY** key had been pressed, the resultant keyboard data sent to the Microprocessor would be as shown in Table 2.

Data entered from the front panel is also displayed. The correct data bit is latched into U1, inverted by U2 for the low CS1 through CS5 outputs. The low CS1 through CS5 outputs enable the Display Drivers to accept microprocessor data to turn on the correct display or LED.

Table 2. Keyboard Data (KDA) With Frequency Key Pressed.

Column Data (A2U4)							Row Data (A2U3)							
Pin Number	**11**	**12**	**13**	**14**	**3**	**4**	**11**	**12**	**13**	**14**	**3**	**4**	**5**	**6**
Keyboard Data	**0**	**SH**	**0**	**0**	**0**	**0**	**1**	**SL**	**1**	**1**	**1**	**1**	**1**	**1**
SH = Strobe High SL = Strobe Low														

Decoupling

Capacitors C1 through C8 and C14 filter the +5V supply to the Display Assembly circuitry.

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 21 when a malfunction seems to have occurred on the keyboard or display. Perform the Troubleshooting on Service Sheets 17, 18, and 19 before attempting to troubleshoot these circuits using this procedure. Procedures for checking the A1 Keyboard Assembly, and part of the A2 Display Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, for example, ⟨✓1⟩

Troubleshooting Help

Block Diagram 4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Test Equipment

Oscilloscope ..... HP 54100A
Oscilloscope Active Probe ..... HP 54001A

⟨✓1⟩Keyboard Interrupt and Serial Keyboard Data Output to Microprocessor

1. Press any front-panel key.
2. Verify that a negative going TTL pulse occurs at A2J3-7 (KIN) each time a key is pressed.
3. Verify that at least one pulse train about 16-bits long occurs at A2J3-6 (KDA).

⟨✓2⟩Control Inputs from Microprocessor

1. Press any front-panel key.
2. Verify that a series of keyboard clock pulses appear on A2J3-5 (CLK).
3. Verify that keyboard strobes appear on A2J3-8 (RKRD), A2J3-2 (KST1), and A2J3-3 (KST2). Note that the signal on A2J3-8 comes from the Amplitude Annunciator Latch A2U1. The strobes for A2U1 as well as the strobes seen on A2J3-2 and A2J3-3 come from the strobe decoders A13U16 (shown on Service Sheet 18).

⟨✓3⟩Key Column Data Lines

1. Press a front-panel key.
2. Verify that the column data line which includes the pressed key is a positive-going pulse. The other column data lines should remain low.

⟨✓4⟩Key Row Data Lines

1. Press a front-panel key.
2. Verify that the row data line that includes the pressed key is a negative-going pulse. The other row data lines should remain high.

TROUBLESHOOTING USING KEYBOARD-INVOKED TEST

Troubleshooting is done on the circuits of Service Sheet 21 when a defect seems to be related to the keyboard. If nothing definite is discovered in performing the keyboard-invoked test consider the other possibilities shown on Service Sheet BD4.

Remember that the serial data from the keyboard encoding circuits does pass through the data bus buffers on the way to the Microprocessor (refer to Service Sheet 17). Also, several of the strobes, clocks, and control signals are decoded on the circuits of Service Sheet 18. The Load Keyboard Data Strobes are decoded on the circuits of Service Sheet 22. The Read Key Row Data Strobe is latched into A2U1.

Refer to the paragraph 8-8 entitled "REPAIR" for front-panel keyboard disassembly instructions.

Keyboard-Invoked Test Procedure

The Keyboard-Invoked Test verifies transmission of encoded addresses from Keyboard to Microprocessor.

The front-panel keyboard can be checked by entering the Keyboard-Invoked Test subroutine Test 4. This test allows for checking of the actual code which the Microprocessor (A13U14) sees when individual keys are pressed. Running this test will verify correct operation of the front-panel and supporting circuitry to the Microprocessor or will identify two problem areas as follows:

If the key code is incorrect when any front-panel key is pressed, but the last key code shown in the FREQUENCY Display remains, then the last pressed key is at fault.

If the key code is incorrect when any front-panel key is pressed, then the supporting circuitry to the Microprocessor is at fault (refer to Service Sheets 17, 18, and 21).

1. Enter the Keyboard-Invoked Tests by first pressing the **SHIFT** key, and then pressing the **INCR SET** key. A "1" should be shown in the MODULATION Display window.
2. Press the **AMPTD** ⇧ key until a "4" is shown in the MODULATION Display window. Test 4, Keyboard Key Test, is ready to run.
3. Press the **INCR SET** key to start the test. A "07" should be shown in the FREQUENCY Display window.
4. Use Table 3, Keyboard Key Codes, to verify keyboard operation.
5. Whenever the **AMPTD** ⇧ or ⇩ key is pressed it is understood that the test is to be exited. A "00" is shown in the AMPLITUDE Display window, and the correct key code is shown in the FREQUENCY Display window. If the test was not meant to be exited, pressing the **INCR SET** key will immediately reinvoke Test 4.
6. To exit the Keyboard-Invoked Tests, press the **AMPTD** ⇧ key until a "7" is shown in the MODULATION Display window. Then press the **INCR SET** key; the Signal Generator is initialized as in Power-On.

Table 3. Keyboard Key Codes.

Value Decimal	Key Name	Value Decimal	Key Name
01	Shift	25	dBf
02	EXT	26	mV
03	AM	27	LOCAL
04	FM	28	INT 1 kHz
05	FREQUENCY	29	DOWN AM (↓)
06	AMPTD	30	DOWN FM (↓)
07	INCR SET	31	FINE TUNE
08	7	32	DOWN FREQ (↓)
09	8	33	DOWN AMPTD (↓)
10	9	34	SAVE
11	MHz	35	1
12	dBm	36	2
13	V	37	3
14	INT 400 Hz	38	%
15	UP AM (↑)	39	dB
16	UP FM (↑)	40	μV
17	COARSE TUNE	41	OFF
18	UP FREQ (↑)	42	RF OFF/ON
19	UP AMPTD (↑)	43	RECALL
20	SEQ	44	0
21	4	45	.
22	5	46	-
23	6	47	←
24	kHz	48	EMF

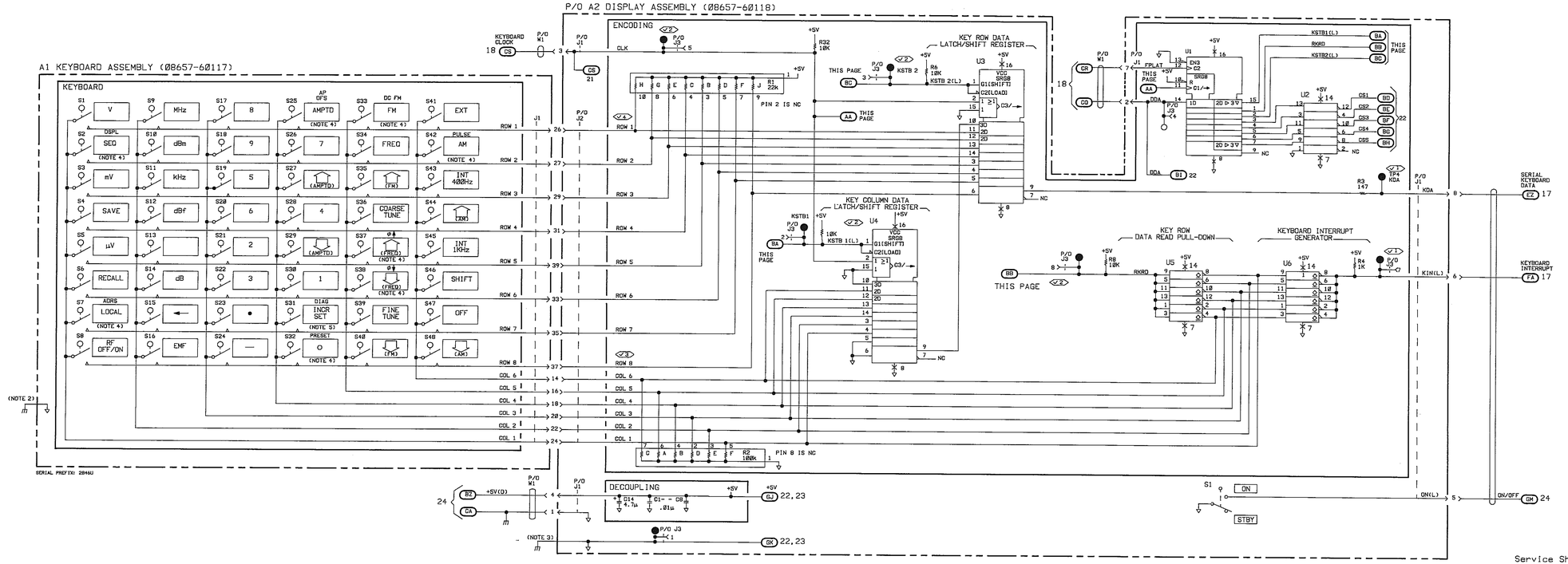


Figure 1
Service Sheet 21 7

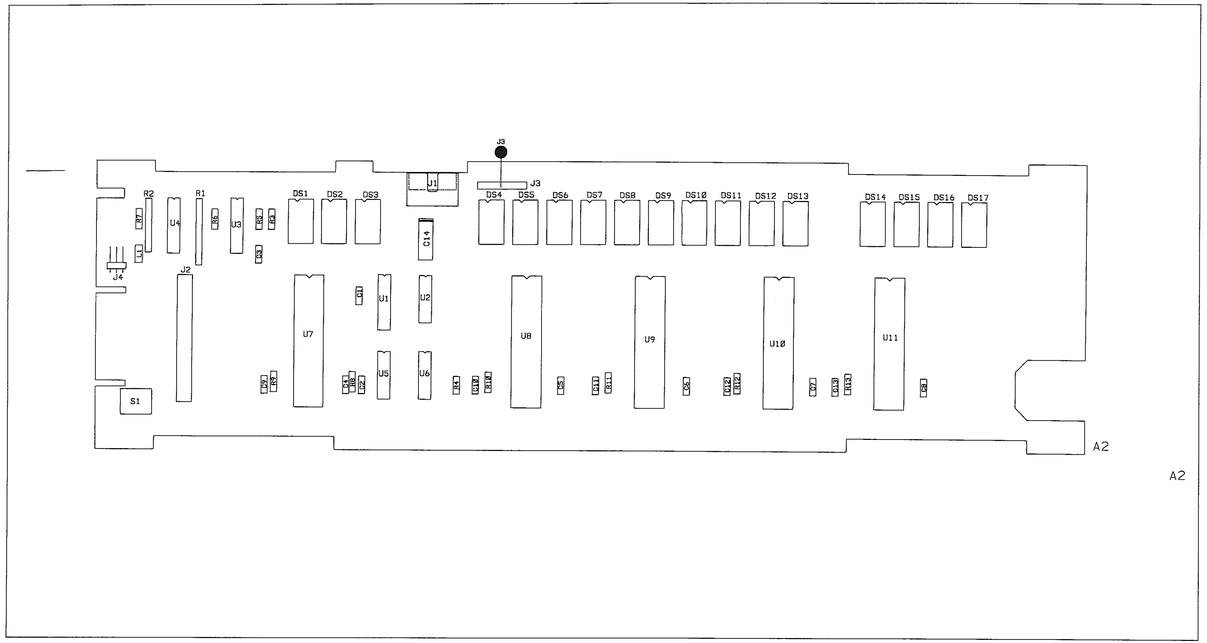


Figure Ø. Service Sheet 22 Information.

Component Locator

NOTES

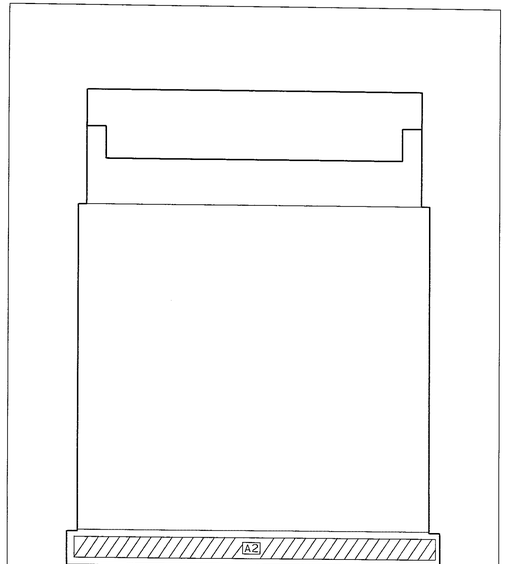
1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.

LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
IS MORE NEG. THAN / IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A1 KEYBOARD
P/O A2 DISPLAY
SEE REVERSE SIDE

SS21



Service Sheet 22

DISPLAY CONTROL

PRINCIPLES OF OPERATION

Display Control

Thirtysix bits of serial display data (DDA) are sent from the Microprocessor via the Serial I/O control circuits (refer to Service Sheet 18) to Display Data Shift Registers U7, U8, U9, U10, and U11. The display drivers are all enabled by CS1, CS2, CS3, CS4, and CS5 at pin 23 of each driver respectively. When each driver is enabled 36 bits of of serial data is input at pin 22 and clocked into the enable driver at pin 21. The first bit sent is always a 1. The next 35 bits turn on or off the LED Display connected to it. After the 36th bit is received the leading 1 then latchs the 35 bits bits of data and clears the shift register. The 35 bits latched turn on and off the LEDs and display segments.

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 22 when a malfunction seems to have occurred in the keyboard or display. Perform the Troubleshooting Using Signature Analysis on Service Sheets 17, 18, and 19 as well as the Troubleshooting on Service Sheet 21 before attempting to troubleshoot these circuits using this procedure. Procedures for checking part of the A2 Display Assembly circuits are given below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, for example, ⟨✓1⟩.

Test Equipment

Oscilloscope	HP 54100A
Oscilloscope Active Probe	HP 54001A

⟨✓1⟩ Display Clocks

1. Verify that the display changes and/or the correct strobe occurs with each keystroke as shown in Table 1.

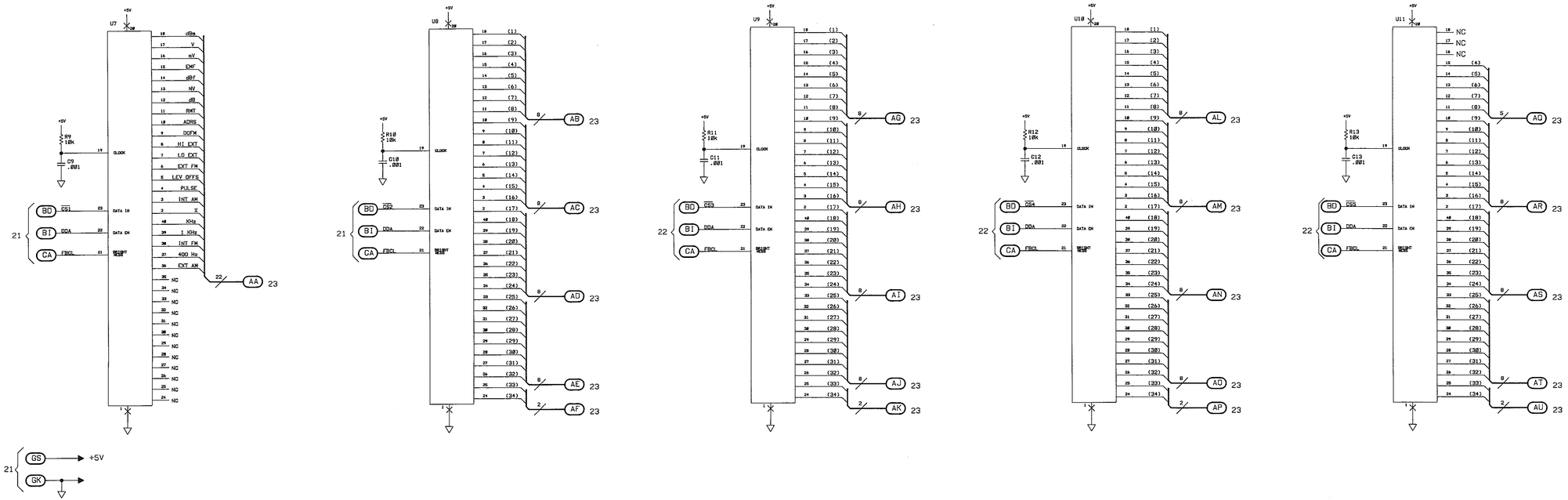


FIGURE 1
SERVICE SHEET 22 3

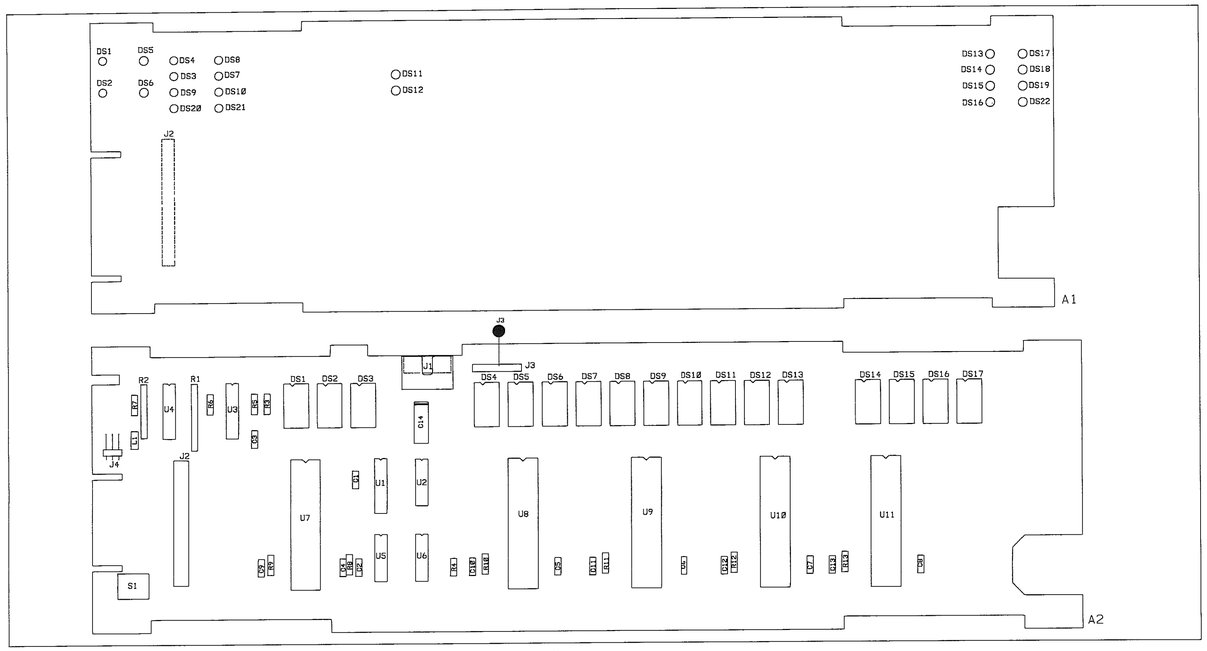


Figure Ø. Service Sheet 23 Information.

Component Locator

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.

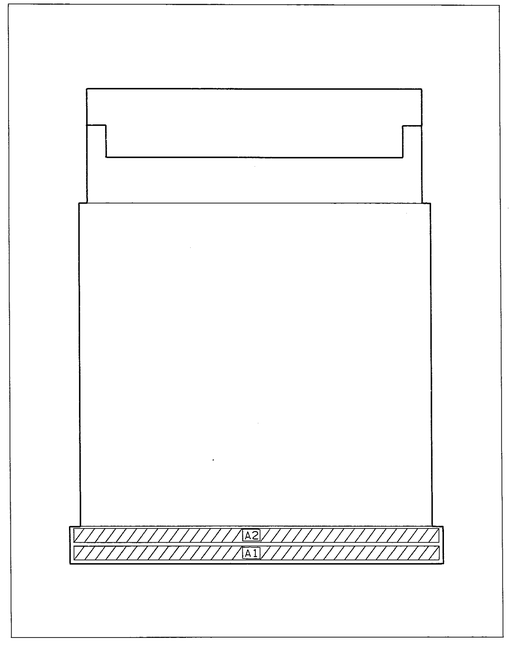
LOGIC LEVELS

	TTL	CMOS
HIGH	2V	3.5V
LOW	Ø.8V	1.5V
IS MORE NEG. THAN IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

P/O A2

SEE REVERSE SIDE

DISPLAY SS22



Service Sheet 23

FREQUENCY DISPLAYS

PRINCIPLES OF OPERATION

General

Seventeen 7-segment, common-cathode devices DS1 through DS17 are used to display frequency, amplitude and modulation values. The decimal points associated with frequency digits DS8 through DS13, modulation digit DS3 and amplitude digits DS15 through 17 are the only decimal points that can be lit. The frequency display decimal point drive circuitry has been previously discussed (refer to Service Sheet 22). Frequency Digits DS4 through DS7 have their decimal point control line tied low which inhibits them from being lit.

The four Latch/Decoder/Drivers U8 through U11 decode display data, store the decoded data, and drive the associated frequency display digit. As previously mentioned 36 bits of serial display data are sent from the Microprocessor to the display circuitry (refer to Service Sheet 22). Each Display Driver is hard-wired to decode and drive the associated display.

Twenty-two LED's are driven by display driver U7. When the control line is low, the associated LED is lit.

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 23 when a malfunction seems to be associated with a 7-segment display or LED. Determine if the malfunction occurs in single or multiple digits. If multiple digit displays are incorrect, ensure that you trace the fault to the correct display driver and:

1. Perform the Troubleshooting on Service Sheet 22.

If pairs of digits are incorrect, suspect the display drivers shown on Service Sheet 22. If single digits are incorrect, continue troubleshooting on this service sheet to determine if displays themselves are faulty.

Procedures for checking part of the A2 Display Assembly circuits are given below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, for example, ⟨✓1⟩

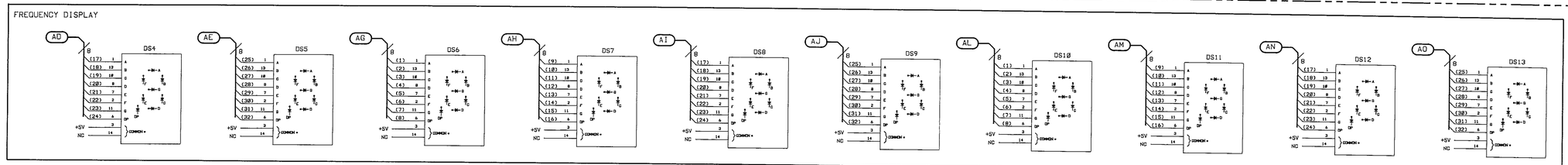
Test Equipment

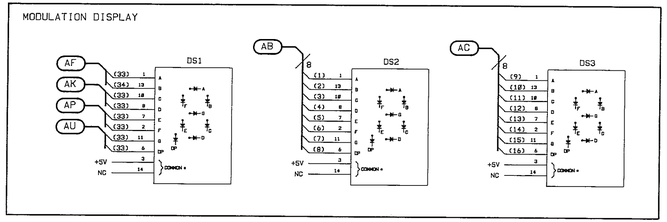
Oscilloscope	HP 54100A
Oscilloscope Active Probe	HP 54001A

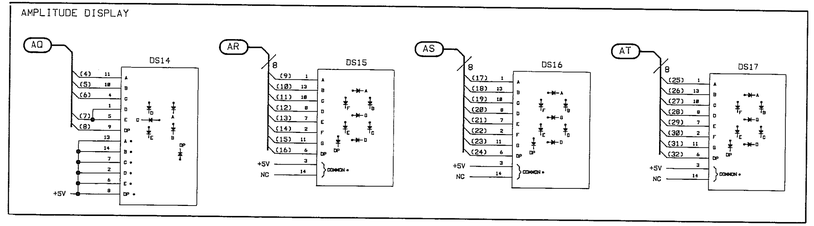
⟨✓1⟩ Frequency Display Digital Drive Levels versus Visual LED Outputs

1. Verify that the 7-segment drive logic levels from the Display Driver matches the visual output for the equivalent segment.
2. Verify that the decimal point drive from the latch and drivers (refer to Service Sheet 22) matches the visual decimal point output.

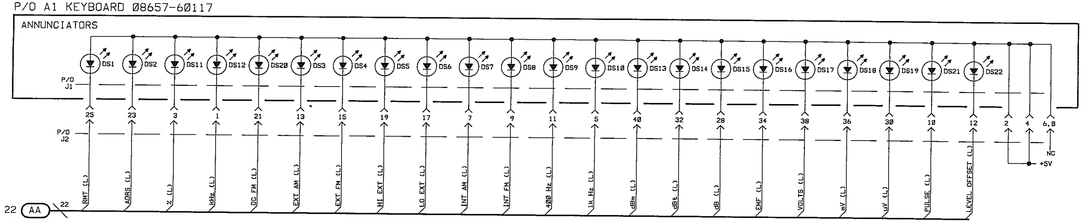
P/O A2 DISPLAY BOARD 08657-60118

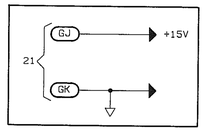






P/O A1 KEYBOARD 08657-60117





SERIAL PREFIX: 2944J

FIGURE 1
SERVICE SHEET 23 3

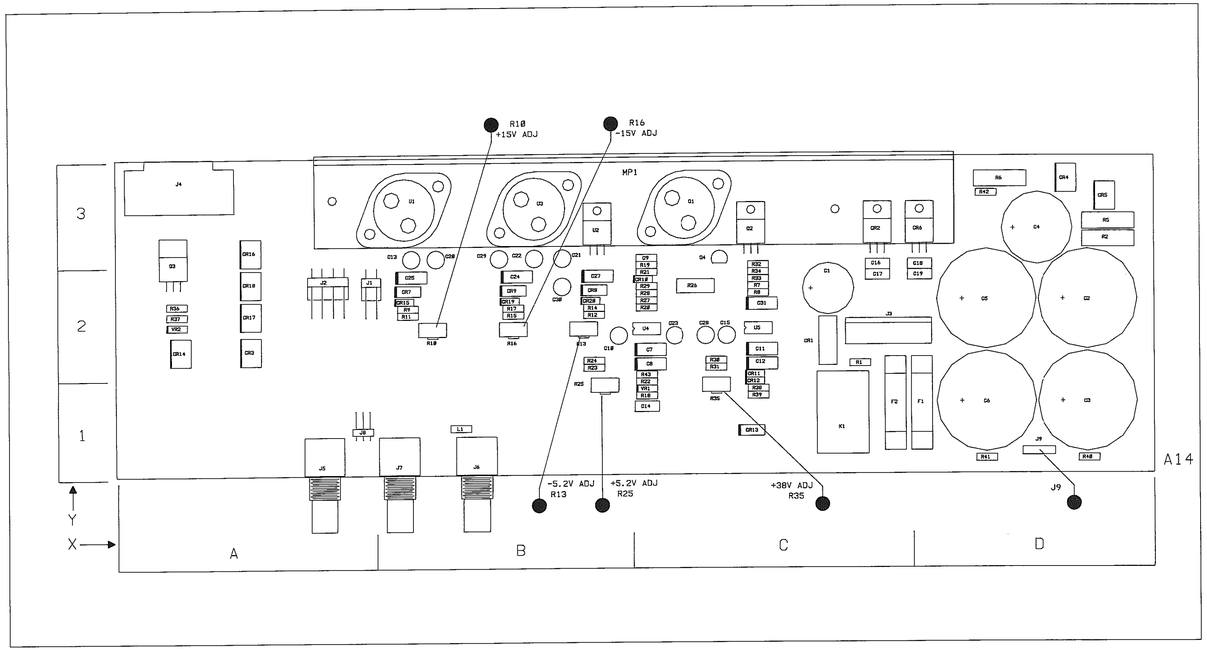


Figure Ø. Service Sheet 24 Information.

Component Locator

WARNING

This instrument does not have a primary power switch. The following voltages are always present whenever the instrument is connected to an AC outlet:

A. Line voltage
B. Primary and secondary AC voltages at T1
C. Unregulated DC voltages (+5.2v,+38v,+15v,-15v,+24v)

WARNING

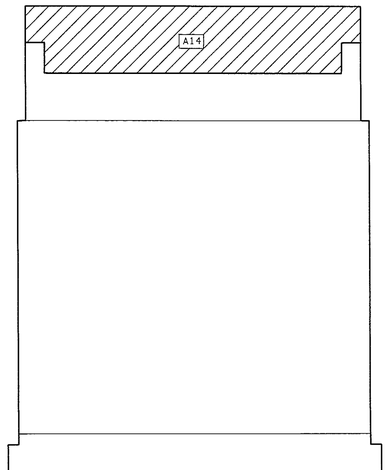
The line power module and T1 may require removal for troubleshooting the A14 power supply board. Live voltages are present on this module whenever it is connected to an AC power source. Extreme caution should be used when working on the power supply with the input power module in an external mode. The transformer must be extended on the service bracket or a service ground must be attached between transformer plate and instrument chassis before proceeding with any power supply troubleshooting.

NOTES

1. For an explanation of schematic symbols, see "SCHEMATIC DIAGRAM NOTES" in Section 8.
2. Removal of this device may inadvertantly defeat chassis ground. Refer to above "WARNING". Additional grounding may be required for service.
3. Energised by the "POWER" switch put to "ON".
4. Removal of the rear panel for serviceing power supply may disconnect J1 and power to cooling fan B1.

P/O A1 KEYBOARD
P/O A2 DISPLAY
SEE REVERSE SIDE

SS23



Service Sheet 24

POWER SUPPLY

PRINCIPLES OF OPERATION

General

The power supply is a linear type providing regulated +15 V dc, −15 V dc, +5 V dc, −5 V dc, and +38 V dc. An unregulated voltage of +24 V dc is also supplied. The supply outputs have very low noise and ac ripple voltage. The supply outputs are protected for overvoltage. The +5.2 V dc is limited by an SCR circuit to +6.2 V dc, the remaining regulated supplies have overvoltage protection in the form of diodes that limit output to their unregulated value.

Regulated Supplies

The ac voltages from the secondary of the power transformer are rectified by +5 V bridge (CR6), a +/-15 V bridge (CR2, CR4, CR5), and a +38 V bridge (CR1). The −5 V dc supply is regulated from −15 V as the source.

The +5 V dc output is protected by an overvoltage crowbar that limits the output voltage to be less than +6.2 V dc. The circuit is composed of VR2, Q3, R36, and R37. If the voltage exceeds +6.2 V dc, VR2 will turn on which will turn on SCR Q3 and clamp the output to ground. When the voltage drops to below +6.2 V dc the crowbar will shutoff and turn the +5 V circuit on.

All of the remaining supplies (except for +38 V) are protected by clamping diodes that limit the output to be no more than .3 V dc above the unregulated value. The +15 V regulator U1 is protected by CR15. The −5 V regulator U2 is protected by CR20. The −15 V regulator U3 is protected by CR19. The +38 V dc supply does not have overvoltage protection.

The +38 V dc supply is regulated in a way that is significantly different than the other supplies. Voltage regulation actually takes place on the negative leg output of the rectifier bridge. This configuration provides the lowest possible noise on the output of the +38 V supply. The output of CR1 is +38 V on the positive leg and −12 V on the negative leg when calibrated. The difference voltage potential is always 50 V. The output of the positive leg can be varied by changing the negative leg voltage. A reference voltage of +5.2 V is brought from the +5 V through the variable voltage divider composed of R39, R38, and R5. A voltage between +4.8 V and 5..2 V can then be set at U5-5 by adjusting R35. The output at U5-7 will be approximately −8 V when calibrated. There is about a 4 V drop across the Q5 and Q2 circuit (example: −8 V at U5-7 and −12 V at emitter of Q4). This arrangement causes the positive leg of CR1 to become a voltage follower, the positive voltage must follow and drop across voltage divider R1 and R30 so that U5-5 and U5-6 become equal in value and the difference between the negative and positive rectifier outputs is 50 V.

LED's A13DS1 through A13DS5 are lit when the power supplies are providing an output voltage. The LED's are switched on when voltages reach an acceptable minimum set by zener diodes A13VR2 through A13VR6, current is set by resistors A13R19 through A13R23.

TROUBLESHOOTING

Procedures for checking the circuits shown on Service Sheet 24 are given below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, for example, ⟨✓1⟩

Troubleshooting Help

Block Diagram 4
Section 4. Performance Tests
Section 5. Adjustment and Post Repair Adjustments

Test Equipment

Digital Multimeter ..... HP 3478A
Oscilloscope ..... Tekitonix 2235

⟨✓1⟩ Voltage Check

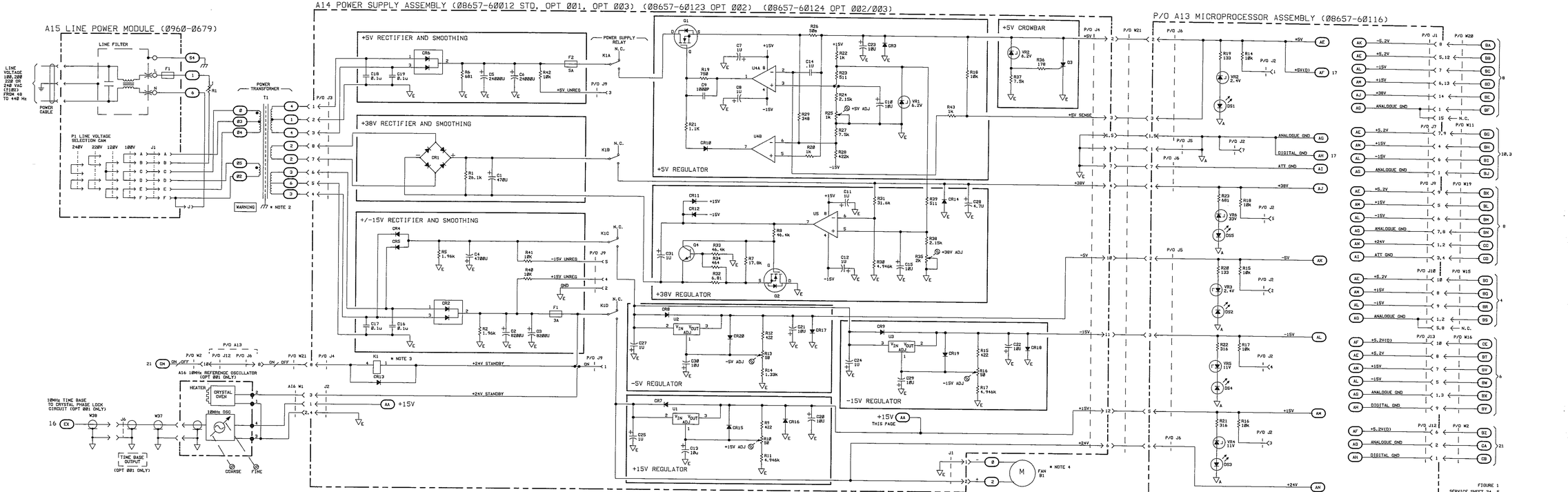
1. Verify that the voltages shown in table 1 are correct.

Table 1. Power Supply Measurements.

Volts	A13J2					A14J3				
	1	2	3	4	5	1 or 3	2	4 or 6	5	7 or 8
Vdc	+5.2	−5	+15	−15	+38	N.A.	gnd	N.A.	gnd	N.A.
Vpp	0.02	0.02	0.02	0.02	0.04	20	gnd	50	gnd	50

A14 Component Coordinates

COMP	X	Y
C1	C	2
C2	D	2
C3	D	1
C4	D	3
C5	D	2
C6	D	1
C7	C	2
C8	C	2
C9	C	3
C10	B	2
C11	C	2
C12	C	2
C13	B	3
C14	C	1
C15	C	2
C16	C	3
C17	C	2
C18	D	3
C19	D	2
C20	B	3
C21	B	3
C22	B	3
C23	C	2
C24	B	2
C25	B	2
C27	B	2
C28	C	2
C29	B	3
C30	B	2
C31	C	2
CR1	C	2
CR2	C	3
CR3	A	2
CR4	D	3
CR5	D	3
CR6	D	3
CR7	B	2
CR8	B	2
CR9	B	2
CR10	C	2
CR11	C	2
CR12	C	1
CR13	C	1
CR14	A	2
CR15	B	2
CR16	A	3
CR17	A	2
CR18	A	2
CR19	B	2
CR20	B	2
F1	D	1
F2	C	1
J1	A	2
J2	A	2
J3	C	2
J4	A	3
J5	A	1
J6	B	1
J7	B	1
J8	A	1
J9	D	1
L1	B	1
MP1	B	3
Q1	C	3
Q2	C	3
Q3	A	3
Q4	C	3
R1	C	2
R2	D	3
R5	D	3
R6	D	3
R7	C	2
R8	C	2
R9	B	2
R10	B	2
R11	B	2
R12	B	2
R13	B	2
R14	B	2
R15	B	2
R16	B	2
R17	B	2
R18	C	1
R19	C	2
R20	C	2
R21	C	2
R22	C	1
R23	B	2
R24	B	2
R25	B	1
R26	C	2
R27	C	2
R28	C	2
R29	C	2
R30	C	2
R31	C	2
R32	C	2
R33	C	2
R34	C	2
R35	C	1
R36	A	2
R37	A	2
R38	C	1
R39	C	1
R40	D	1
R41	D	1
R42	D	3
R43	C	2
U1	B	3
U2	B	3
U3	B	3
U4	C	2
U5	C	2
VR1	C	1
VR2	A	2


A14 POWER SUPPLY ASSEMBLY (08657-60012 STD, OPT 001, OPT 003) (08657-60123 OPT 002) (08657-60124 OPT 002/003)
A15 LINE POWER MODULE (0960-0679)
P/O A13 MICROPROCESSOR ASSEMBLY (08657-60116)
LINE FILTER
LINE VOLTAGE 100,220 220 OR 240 VAC CEILING FROM +5 TO 440 Hz
POWER CABLE
P1 LINE VOLTAGE SELECTION CAM
240V 220V 120V 100V
POWER TRANSFORMER
WARNING
* NOTE 2
+5V RECTIFIER AND SMOOTHING
+38V RECTIFIER AND SMOOTHING
+/-15V RECTIFIER AND SMOOTHING
POWER SUPPLY RELAY
+5V UNREG
+5V REGULATOR
+5V CROWBAR
+5V SENSE
+5V ADJ
+38V REGULATOR
+38V ADJ
-15V UNREG
-5V REGULATOR
-5V ADJ
-15V REGULATOR
-15V ADJ
+15V REGULATOR
+15V ADJ
+15V THIS PAGE
+24V STANDBY
* NOTE 3
A16 10MHz REFERENCE OSCILLATOR (OPT 001 ONLY)
10MHz TIME BASE TO CRYSTAL PHASE LOCK CIRCUIT (OPT 001 ONLY)
HEATER
CRYSTAL OVEN
10MHz OSC
TIME BASE OUTPUT (OPT 001 ONLY)
COARSE
FINE
* NOTE 4
FAN 01
ANALOGUE GND
DIGITAL GND
ATT GND
FIGURE 1
SERVICE SHEET 24 S

A14 POWER SUPPLY
P/O A13 MICROPROCESSOR
SEE REVERSE SIDE

SS24