Agilent 4352S
VCO/PLL Signal Test System
Optimizing VCO/PLL Evaluations and PLL Synthesizer Designs

Application Note

Introduction

Today's mobile communication systems demand higher communication quality, higher data rates, higher frequency operation, and more channels per unit bandwidth. As much of this equipment is portable, low power consumption and small size are also required. All of these constraints combine to make the whole design including component selection and evaluation quite challenging. One portion of this design that is very critical with regard to all of the requirements mentioned above is the synthesized oscillator. Typical synthesized oscillators combine a Voltage Controlled Oscillator (VCO) with a Phase-Locked Loop IC (PLL), frequency reference (e.g. Crystal / TCXO) and a loop filter. The VCO is used to generate the RF output frequency. The PLL (which is of the "analog type"; i.e. different from a pure digital PLL) is used to stabilize and control the frequency. The loop filter design must integrate all of the components to establish, among other things, a tradeoff between noise and transient response (Figure 1).

This Application Note will describe the evaluation of the PLL and VCO and relate those evaluations to information that will allow the circuit designer to optimize the whole oscillator design including the loop filter.
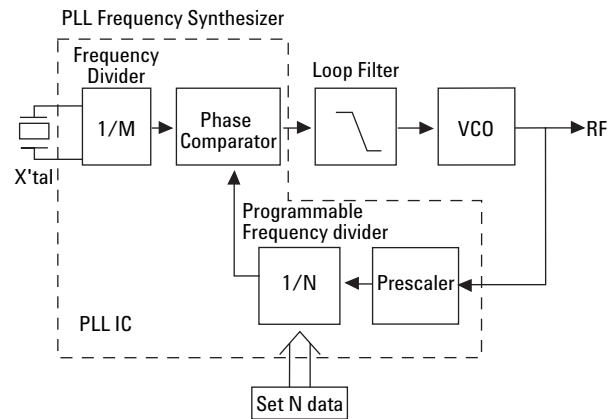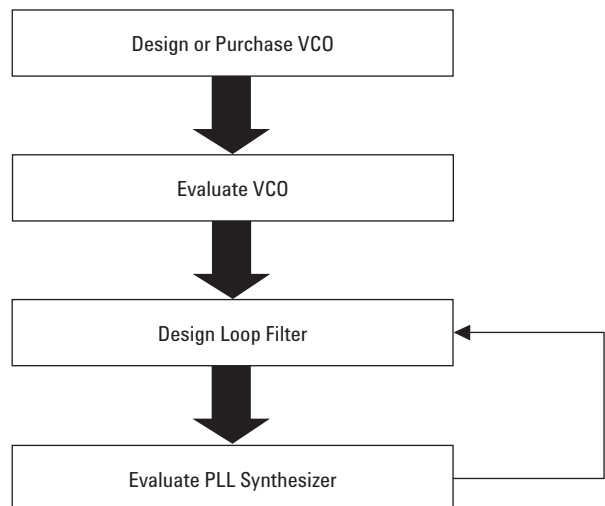

Fig. 1: Basic Block Diagram of PLL Frequency Synthesizer

Fig. 2: PLL Frequency Synthesizer Design Flow

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1 VCO Characteristic Parameters and Problems with the Conventional Evaluation Method

1-1 VCO characteristic parameters to be evaluated

Shown below are many of the common VCO evaluation parameters. To perform these evaluations, many instruments and set-ups are required even including special DC sources for both the power supply and tuning voltage.

1) Oscillation frequency [Hz]
2) Oscillation power level [dBm]
3) Phase noise [dBc/Hz]
4) Residual FM [Hz rms]
5) DC consumption current [mA]
6) Tuning sensitivity [Hz/V]
7) Harmonic/spurious [dBc]
8) Frequency pushing [Hz/V] and frequency pulling [Hz p-p]

Nine or more measuring instruments including a DC voltage source (for VCO power supply), a DC control (tuning) voltage source and a spectrum analyzer are required to evaluate these characteristics. A controller and control and analysis programs are also required to control these instruments and analyze measurement results.

For example, the VCO changes its oscillation frequency if there is a change in DC voltage level applied to its control terminal. To determine the VCO basic performance, evaluate the output frequency vs. DC control voltage characteristic (F-V characteristic). A program that can measure the output frequency with a frequency counter is required to accomplish this. The program should display the measurement results in graphical form as the DC control voltage level from the DC voltage source is changed. Another important VCO parameter is tuning sensitivity with respect to the VCO control voltage. The tuning sensitivity is the derivative of the VCO frequency by the tuning voltage. It significantly affects the loop characteristics. PLL design should measure and graphically display the tuning sensitivity of the VCO.

The absolute level of oscillation power depends primarily on the DC control voltage. This level should be maintained constant over the entire frequency range within which the VCO can oscillate. It is critical to evaluate the oscillation power level vs. DC control voltage characteristic. A program that can measure the oscillation power level and display the measurement results in graphical form while changing the DC voltage level is required.

1-2 Impact of control voltage source noise characteristic on VCO

Using a general purpose DC power supply as the DC control voltage source for the VCO may degrade the measured VCO phase noise characteristic due to large noise component contained in the supplied power. As a result, the measurement result obtained will be similar to that shown in Fig.3. This result does not represent the real VCO characteristic. To suppress this noise component, provide a noise elimination filter (low-pass filter) with a low cutoff frequency at the DC control voltage input terminal of the VCO. The lower the cutoff frequency the longer the time constant, and longer time it takes for the VCO frequency and its output level to stabilize. This results in longer measurement time. The longer measurement time can cause the carrier frequency to vary due to change in temperature, humidity, or external noise, thus making it difficult to evaluate accuracy.
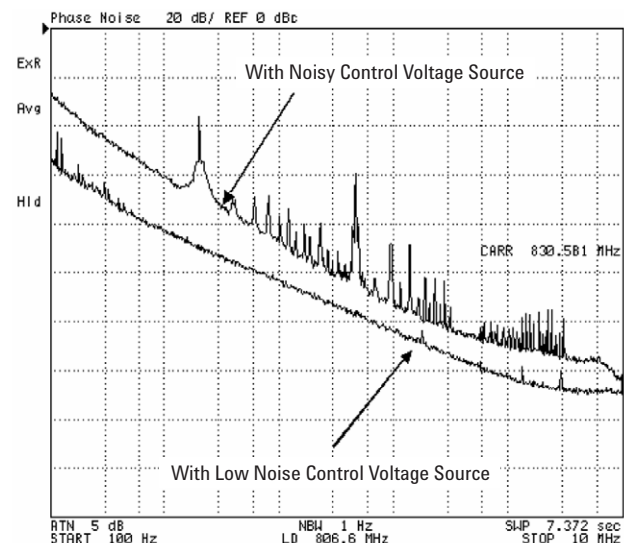

Fig. 3: Impact of Control Voltage Source Noise Characteristic on VCO

1-3 VCO oscillation frequency stability and phase noise characteristic evaluation

Phase noise is a random noise. It is expressed as the ratio of "power spectrum density at a specified offset frequency" to "carrier signal level". Averaging is essential to ensure proper repeatability of measurement results. (See Fig.4.)
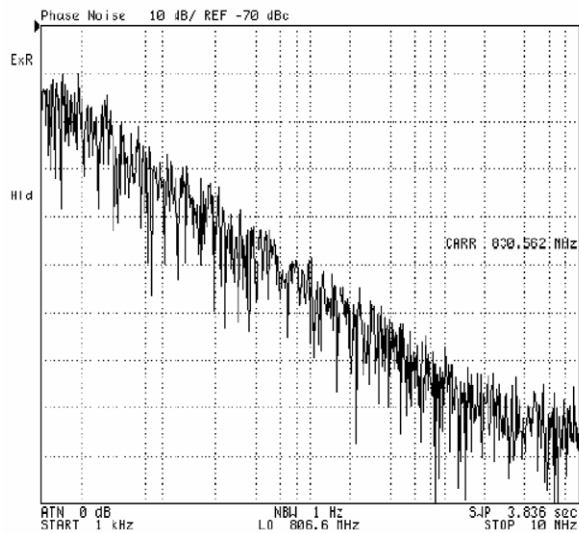

Fig. 4: Phase Noise Measurement Results without Averaging

A difficulty caused by VCO oscillation frequency drift or jump may occur when using a spectrum analyzer to measure VCO phase noise. Such frequency drift or frequency jump occurs when there is a temperature change, vibration or shock during the measurement period. Measurement errors may occur if the previous conditions were present during the measurement. (See Fig.5.) Since these error factors are usually not repeatable, they cannot be removed or calibrated by averaging or other methods. To make accurate VCO phase noise measurement, it is important to keep VCO oscillation frequency stable during the measurement. However, VCO frequency is so sensitive to its environmental disturbance that it is very difficult to keep VCO oscillation frequency constant without sophisticated stabilizing mechanism in the measurement system.
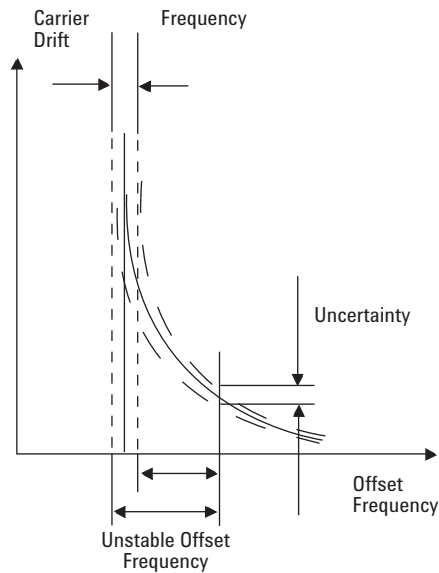

Fig. 5: Impact of Carrier Drift on Phase Noise Characteristic

1-4 Phase noise measurement of DUT and phase noise of measurement system

The measurement system should have better phase noise performance than that of DUT (Device Under Test). The measurement system cannot measure phase noise of the DUT whose phase noise level is lower than the system noise floor. However, even when the system noise floor is lower than DUT noise, the measurement result will have relatively large error if the DUT phase noise level is close to the system noise floor. To get an accurate and reliable result, the system noise floor of the measurement system must be carefully evaluated and compared with the DUT phase noise.

1-5 Phase noise of end product (equipment) and phase jitter requirements

With today's mobile communication, digital modulation for improved frequency band use efficiency and a variety of schemes for reduced bit error rate are commonplace. For example, ACPR (Adjacent Channel Power Ratio), that represents the purity of transmitted and received signals, includes not only distortion and AM noise caused by digital signal but also phase noise. For this reason, when it is desired to measure only
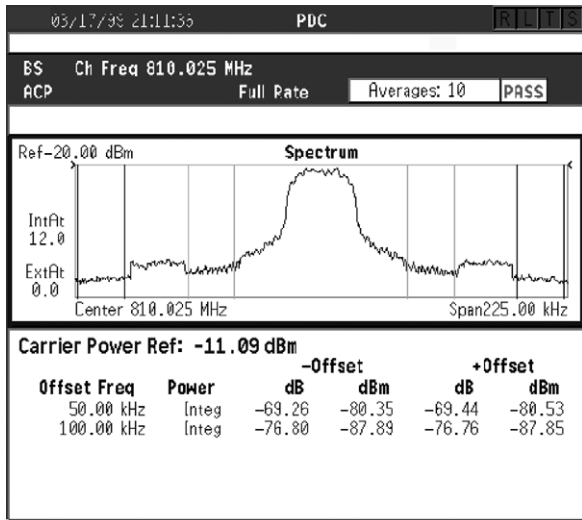
Fig. 6: Example of ACPR (Adjacent Channel Power Ratio) Measurement Using the E4406A

phase noise power in a specific frequency range, there is no alternative but to use a measurement system dedicated to that purpose. This is in despite to growing demands to reduce phase noise, eventually requiring a large amount of time and cost. (Fig.6 shows an example of ACPR measurement for PDC-modulated signals using the E4406A vector signal analyzer.)

Phase jitter measurement of wavelength or clock frequency is of significant importance for evaluating the performance of radar, laser length measuring machine, A-D and D-A converters as well as digital communication systems. An increase in phase jitter causes transmit, receive distance, and quantization

errors as well as bit errors due to irregular sampling. Phase jitter is equivalent to residual phase modulation and determined by phase noise. A dedicated phase noise measurement system is required to calculate phase jitter based on phase noise. As mentioned previously, it has been difficult to make efficient phase jitter measurement and analysis.

2　VCO Characteristic Evaluation Using the 4352S and Features of the 4352S

2-1　VCO testing capabilities of the 4352S

The Agilent 4352S is a self-contained solution for performing virtually all measurements required for thorough VCO evaluation (Figure 7). Specialized sources and measurement equipment have been combined to achieve this dedicated task with ease and accuracy. For example, the system contains a low noise power supply to power the DUT and an ultra low noise DC tuning / control voltage source (Figures 5 & 6). The system is integrated and includes the switching and firmware to perform all of the following tests accurately and with ease.

1) Oscillation Frequency [Hz]
2) Oscillation Power level [dBm]
3) Phase noise [dBc/Hz]
4) Residual FM [Hz rms]
5) Drive consumption current [mA]
6) Tuning sensitivity [Hz/V]
7) Harmonic/spurious [dBc]
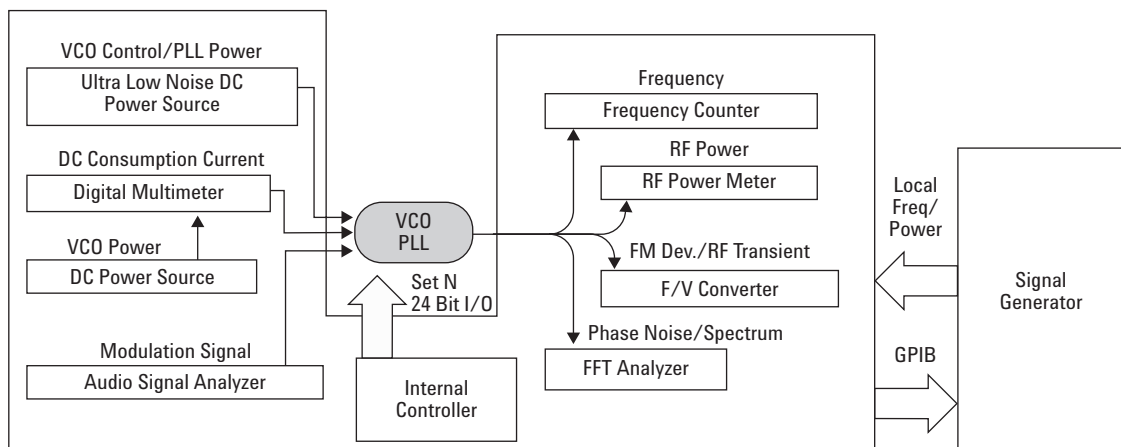8) Frequency pushing [Hz/V]

Fig. 7: 4352S System Block Diagram

These functions will alleviate the tasks of configuring a measurement system, correcting measurement data and creating measurement and analysis programs. The result is improved design and evaluation efficiency. For example, the 4352S makes it possible to readily measure and graphically display basic VCO performance parameters such as RF output power vs. DC control voltage characteristic, RF output frequency vs. DC control voltage characteristic (F-V characteristic) and tuning sensitivity characteristic. (See Fig.8 and Fig.9.)
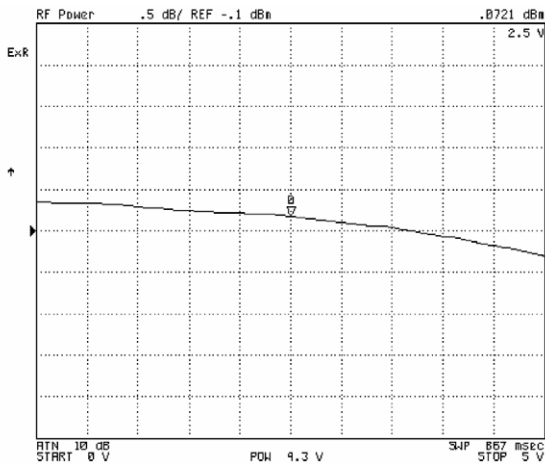
Note also that the 4352S can measure frequency pushing (oscillation frequency change with change in DC power supply voltage level) by controlling the voltage level of the VCO power supply through its IBASIC programming function. Figure 10 shows an evaluation example of the output frequency vs. DC power supply voltage characteristic. In this example, three different DC power supply voltage level settings are used.

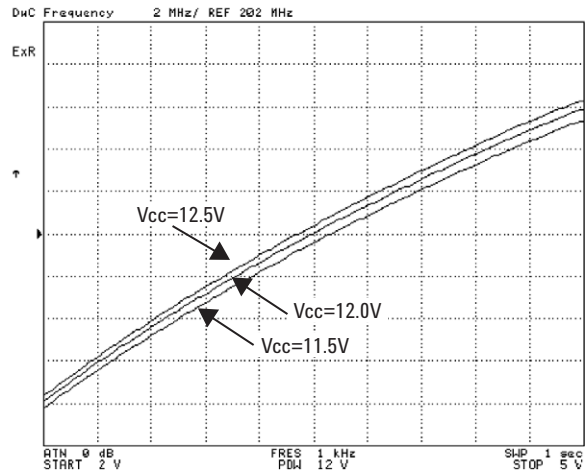Fig. 8: RF Output Power vs. DC Control Voltage Curve Obtained
through the 4352S

Fig. 10: Example of Frequency Pushing Measurement
(Examples of Frequency vs. DC Voltage Characteristic
during Change in DC Power Supply Voltage Level)

2-2 Ultra low noise DC voltage source

The 4352S incorporates a VCO power supply (DC POWER, $10nV/\sqrt{Hz}$@10kHz offset) and an ultra low noise VCO control voltage source (DC CONTROL, $1nV/\sqrt{Hz}$@10kHz offset) for testing VCO. Because it is not necessary to add a DC power supply for VCO testing or low-pass filter to remove noise, it is possible to quickly determine the real VCO phase noise characteristic without waiting during DC power voltage setting change.

2-3 High speed SSB phase noise measurement function and automatic frequency control function

The 4352S includes a "Carrier lock multi-mode PLL circuit", developed for high-speed phase noise measurement. The stepped FFT technique and the

Fig. 9: Output Frequency vs. DC Control Voltage Curve Obtained
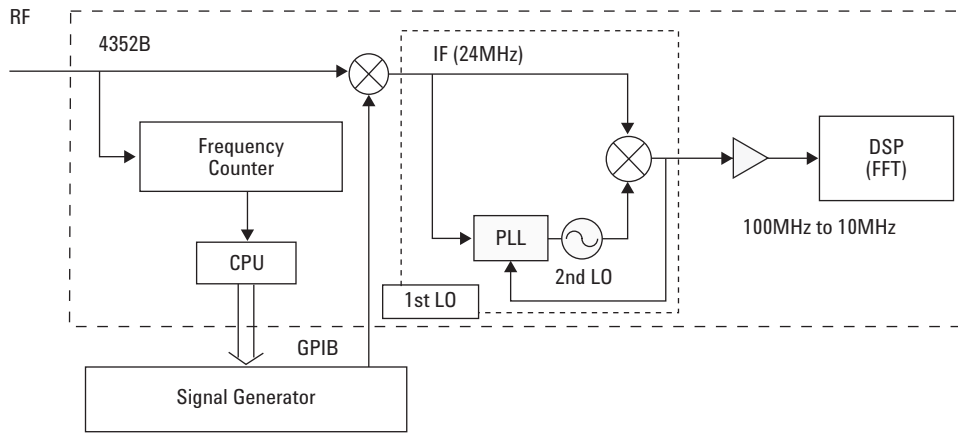Using the 4352S

Fig. 11: Carrier Lock Multi-mode PLL Block Diagram

ultra low noise DC control voltage source, enable fast and easy VCO phase noise measurements (several tens of times faster than the conventional method). Figure 11 shows the block diagram of the carrier lock multi-mode PLL circuit. The VCO frequency is measured, and then the carrier frequency is translated into IF of 24 MHz through the mixer, with the local signal from the external signal source. The phase noise of the signal is measured in the carrier lock multi-mode PLL circuit with the orthogonal phase detection method. This phase noise measurement circuit continually locks to the drifting carrier frequency enabling quick and accurate phase noise measurement with high repeatability. Because the 4352S has automatic control over all necessary settings, including the external signal source frequency, the phase noise measurement can be made with ease. (See Fig.12.)

The 4352S Automatic Frequency Control, which operates with the built-in frequency counter and DC tuning voltage source, automatically controls the DC tuning voltage. Therefore, VCO phase noise at a specific carrier frequency can easily be measured by directly entering the desired frequency. (See Fig.13.)
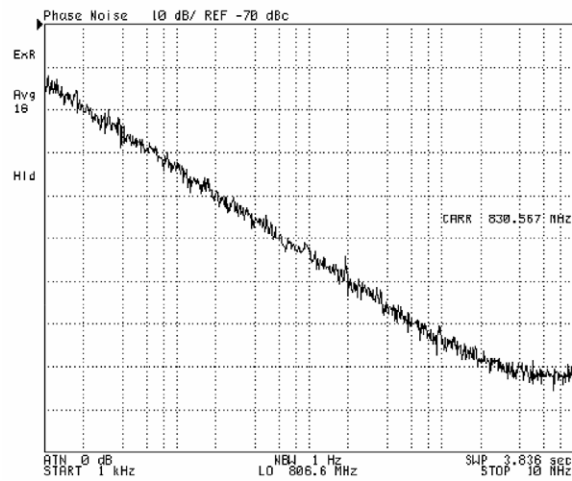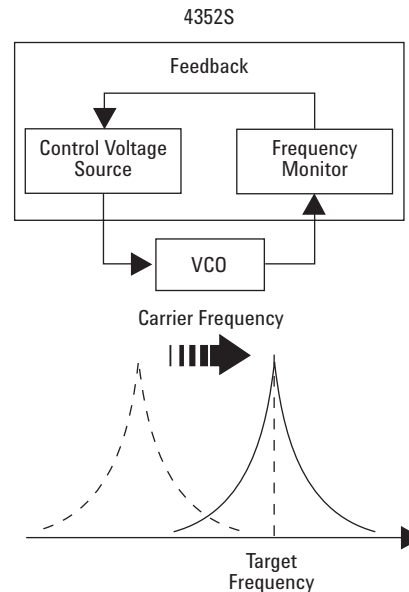

Fig. 12: Example of VCO Phase Noise Measurement Using the 4352S

Fig. 13: Automatic Frequency Control Function

2-4 Phase noise characteristic of the 4352S

The 4352S is designed to have phase noise of -157dBc/Hz (typical with 1 GHz carrier frequency @1 MHz offset frequency). This is sufficiently lower than the phase noise level of VCO's used in ordinary cellular phones. (See Fig.14.)
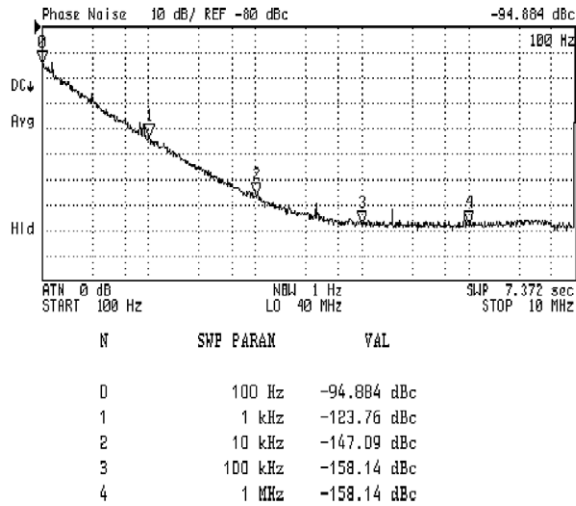

N	SWP PARAM	VAL
0	100 Hz	-94.884 dBc
1	1 kHz	-123.76 dBc
2	10 kHz	-147.09 dBc
3	100 kHz	-158.14 dBc
4	1 MHz	-158.14 dBc

Fig. 14: Typical 4352B Phase Noise Characteristic

A consideration must be made to the phase noise generated by external local signal source when configuring a measurement system. For more information on how to select the optimal signal generator, see "1) Selecting Local Signal Source (Standard Signal Generator) for the 4352S" of "Considerations for Configuring Optimal 4352S System" in the last chapter.

2-5 Integrated phase noise measurement function and phase jitter calculation

Adjacent channel power ratio, a standard requirement to be met by final products, is represented as the ratio of power at the carrier frequency to integrated power within the specified offset frequencies. This is unlike the standard representation of phase noise.

The 4352S displays phase noise and integrated phase noise power within the specified frequency range on the same screen for improved development and design efficiency.

Figure 15 shows a phase noise vs. offset frequency trace measured with the 4352S. The total phase noise power [dBc] within the cursor-specified offset frequency range (1 kHz) appears at the lower left corner of the screen.
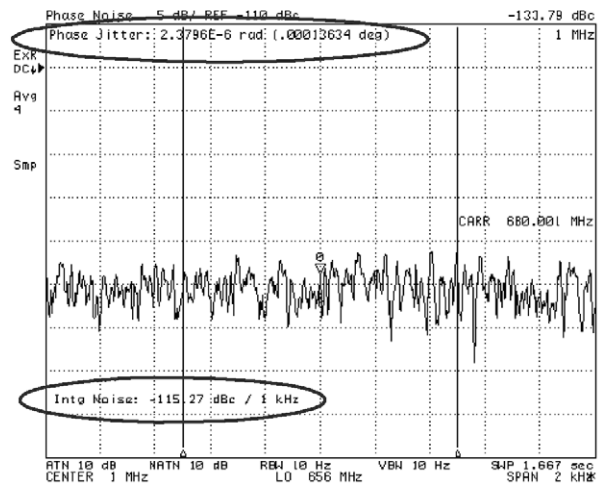

Fig. 15: Example of Phase Noise Power Measurement Using the 4352S

Common logarithmic scale is normally used for offset frequency when a phase noise trace is displayed, however, linear scale is used for offset frequency when an adjacent channel power ratio trace is displayed. Similarly, the 4352S selects linear sweep for offset frequency when measuring phase noise power.

The 4352S measures the integrated phase noise and can calculate phase jitter based on phase noise measurement results using IBASIC programming function. The following example demonstrates how to calculate phase jitter:

The relationship between phase noise L(f) and phase transition spectrum density Sø(f) is expressed as follows:

$$L (f) \left[dBc / Hz \right] = \frac{1}{2} S\text{ø}(f) \left[rad^2 / Hz \right]$$

$$Phase\ Jitter = \sqrt{\int_A^B S\text{ø}(f)}\ [rad]$$

$$= \frac{360}{2\pi} \sqrt{\int_A^B S\text{ø}(f)}\ [degrees]$$

Note that L(f) and Sø are represented in [dBc/Hz] and [rad^2/Hz], respectively. The value measured with the 4352S is $\int_A^B L (f)$ [dBc]. If this measured value is P [dBc], phase jitter can be obtained as follows:

$$Phase\ Jitter = \sqrt{\int_A^B 2L(f)}$$

$$= \sqrt{\int_A^B L(f)}$$

$$= \sqrt{2 \cdot 10^{P/10}}[rad\ rms]$$

The following sample program converts integrated phase noise value obtained with the 4352S and displays phase jitter converted from phase noise:

```
10 ASSIGN @Agilent4352 TO 800
20 OUTPUT @Agilent4352;"DISA BASS"
30 OUTPUT @Agilent4352;"INTGNOIS?"  ! Query for Integ Noise
40 ENTER @Agilent4352;Integ_noise  !
50 Phase_jitter=(2*10^(Integ_noise/10))^.5  ! Integ Noise to Phase Jitter
60 Phase_jitter_d=360/(2*PI)*Phase_jitter  ! in degree
70 Disp_pj1$="Phase Jitter: "
80 Disp_pj2$=VAL$(DROUND(Phase_jitter,5))
90 Disp_pj3$=" rad rms("
100 Disp_pj4$=VAL$(DROUND(Phase_jitter_d,5))
110 Disp_pj5$=" deg rms)"
120 DISP Disp_pj1$;Disp_pj2$;Disp_pj3$;Disp_pj4$;Disp_pj5$
130 END
```

Through IBASIC programming the 4352S calculates phase jitter based on the above formula. The result is then displayed on the screen. The numbers shown on the upper left corner in Fig.15 is the phase jitter value obtained through the above program.

The 4352S functions discussed above will assist with determining the synthesizer parameters that should be modified. The modifications will improve the end product system performance, and decrease product development time.

3 Measuring Other Parameters for VCO Performance Evaluation and Considerations for Measurement

3-1 Measuring other parameters

3-1-1 Other measurement functions of the 4352S

The 4352S incorporates the following functions for measuring additional parameters:

1) Spectrum analyzer function with a maximum span of 10 MHz for automatic detection of 2nd and 3rd harmonics during harmonic level measurement (Note that the permissible range for automatic harmonic frequency detection is between 10 MHz and 3 GHz. A desired frequency must be specified if it exceeds 3 GHz.)

2) Frequency drift (post tuning drift) measurement function (zero span measurement function in the F-V measurement mode (1 hour max.), measurement for over 1 hour available through IBASIC programming function)

3) 1 kHz modulating signal source and high accuracy peak deviation measurement function for identification of frequency modulation (FM) characteristic

4) Frequency counter and spectrum analyzer functions for frequency pushing measurement

3-1-2 Measuring frequency pulling with the 4352S and other equipment

Frequency pulling gives the sensitivity of the free-running VCO's compared to the load fluctuations at the VCO output.

Normally, a phase shifter and attenuator (variable or fixed at approx. 6dB) are used to generate return loss on the order of 9.5 to 12 dB (or VSWR of 2 to 1.67). At the same time, the phase is varied from 0 to 2π radians (0-360 deg.). Frequency pulling is determined as the maximum and minimum oscillation frequencies. In general, one of the following two methods is used:

1) A directional bridge is connected between the VCO's RF terminal and the phase shifter. The RF signal frequency, fed through one of the branches of the bridge, is measured with a frequency counter or spectrum analyzer. (Fig.16 shows an example of connection using the 4352S.)

2) The RF signal frequency, that leaks out through the VCO's drive voltage or control voltage terminal, is measured with a spectrum analyzer or frequency counter. (See Fig.17.)
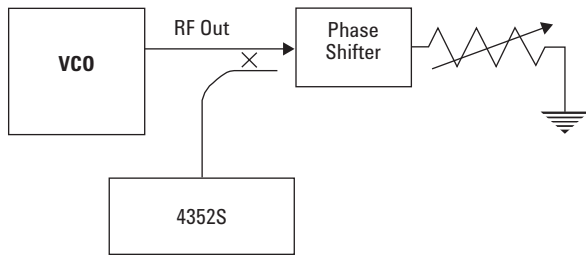

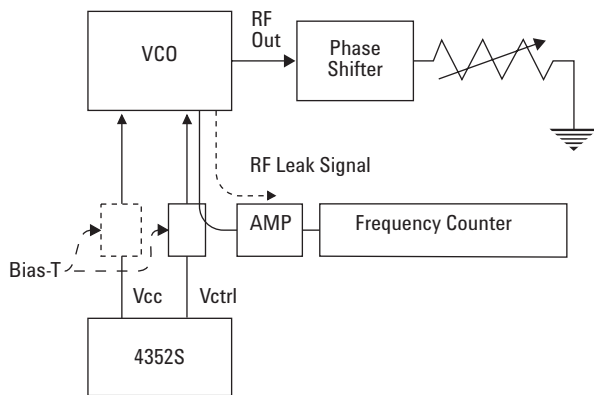**Fig. 16: Example (1) of Frequency Pulling Measurement**

Fig. 17: Example (2) of Frequency Pulling Measurement

Bear the following in mind when conducting frequency pulling measurement:

1) Check that specified VSWR (or return loss) is obtained.

   Normally, the phase shifter's attenuation varies with change in frequency or phase. Evaluate VSWR for the overall load (as seen from the VCO) in advance at the actual measurement frequency using a network analyzer or other appropriate devices. If the VSWR does not match the desired level, adjust the phase shifter properly so that VSWR reaches the correct level before initiating VCO performance evaluation.

2) If measurement method (2) shown in Fig.17 is used, use a filter (or DC Bias-Network (Bias-T); 11612A) to extract only the RF component and allow only the DC component from the DC voltage source to be applied to the VCO. This prevents the RF component from reflecting back toward the DC voltage source, and ensures proper VCO oscillation with no impact caused by RF component reflection. If RF leak signal level is extremely small, provide an RF amplifier, or similar tool, to properly increase the signal level.

   Selecting a test method and measuring instruments that best fit the characteristics of the target VCO is of prime importance for proper design and evaluation.

3-1-3 Automating VCO performance evaluation

The 4352S measures all VCO performance parameters other than frequency pulling without changing the system configuration. This makes it possible to create a test sequence program using the built-in IBASIC programming function.

Fig.18 shows an example for shipment inspection on the VCO production line. Similar sequence programs are readily adaptable to quality control evaluation or acceptance inspection. Note that sequence programs created with the IBASIC programming function can exchange data with external equipment such as handlers.

```
Measurement Time   :          9.450 second

  DC POWER     :          4.30 V          5.37 mA
  DC CONTROL :         1.00 V          2.50 V          4.00 V
  Frequency  :       816.914 MHz    836.853 MHz    857.108 MHz
  RF Power   :           .18 dBm          .05 dBm         -.10 dBm

  Freq. Pushing : (@ -.25 V)          -112 kHz
  Freq. Pushing : (@  .25 V)           107 kHz
  Sensitivity   :                   13.40 MHz/V

Auto Frequency Control [ AFC Target = 835 MHz ]
  AFC Frequency :                   835.000 MHz
  Vcontrol for AFC Frequency :        2.360 V
  Phase noise   :
            ( @ 5 kHz )              -96.52 dBc/Hz
            ( @ 25 kHz )            -110.73 dBc/Hz
            ( @ 600 kHz )          -138.10 dBc/Hz
  FM Deviation  :  [ Detection BW : 300Hz - 3kHz ]
  Residual FM (S/N @ S=3.5kHzp-p) :    7.11 Hzrms (S/N= 50.8 dB)
  1kHz FM Signal (@ Mod-Amp= .35mV): 10.81 kHzp-p
  2nd Harmonics Level :              -18.7 dBc
  3rd Harmonics Level :              -45.1 dBc
```

Fig. 18: Measurement Example on the VCO Production Line Using the 4352S

3-2 Considerations for connecting the DC voltage source (handling control voltage terminal and cables)

Because the 4352S's DC control voltage source has an extremely low noise level (1nV/√Hz@10kHz offset), it is unnecessary to provide a filter for noise elimination when measuring most of the VCO performance parameters.

The VCO oscillation frequency component, however, may leak through the VCO's DC control voltage input terminal. When this occurs, signal reflection may take place between the VCO's DC control voltage input terminal and the 4352's DC control voltage source. This is because of mismatch between the VCO impedance and the voltage source input impedance or cable characteristic impedance are affected by the oscillation frequency. Consequently, the VCO output characteristics, including, in particular, output frequency and RF power are affected.

In this case, insert a low-pass filter (cutoff frequency: 100 kHz to 1 MHz) at the VCO's DC control voltage input terminal, as shown in Fig.19, to attenuate the oscillation frequency component. Additionally, use a coaxial cable to connect the DC control voltage source or DC drive power supply to the target VCO.
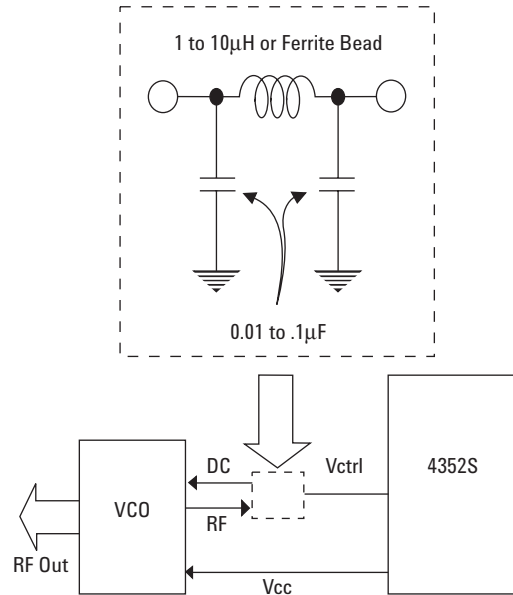

Fig. 19: Example of Low-pass Filter Circuit Inserted between the VCO and HP4352B's Vcontrol Terminal

4 PLL Characteristic Evaluation Parameters and Problems with the Conventional Evaluation Method

PLL frequency synthesizers must generate pure signals.

In designing a synthesizer, evaluate the performance characteristics of VCO, prescaler, PLL IC chip and crystal resonator design a loop filter that best suits such characteristics. Determine the carrier frequency stability (PLL frequency bandwidth). Determine if the synthesizer can substantially reduce phase noise and spurious level at frequencies around the carrier frequency under steady oscillation conditions. Determine the synthesizer response. Determine if it can quickly change the carrier frequency.

A PLL frequency synthesizer has a structure that allows the reference frequency component leak (reference leak) from the phase comparator to be convoluted upon the VCO input. This causes the PLL output to be frequency-modulated, thus generating some spurious component. In designing a loop filter, minimize phase noise at frequencies around the carrier frequency while at the same time suppressing the spurious component.

The PLL lockup time (frequency transition time during change in PLL frequency division ratio) is substantially affected by the loop filter characteristics. In general, the higher the loop filter's cutoff frequency, the smaller the loop filter time constant. In this case, PLL spurious characteristic is worse although the PLL can respond more quickly and the lockup time becomes shorter.

The dynamic characteristics of the PLL frequency synthesizer cannot be readily determined. Because it is influenced by the combination of VCO/PLL IC chip / loop filter etc. in addition to the performance of an individual component. Instead, you must repeatedly evaluate and analyze these characteristics under actual loop operating conditions.

4-1   PLL frequency synthesizer measurement parameters

Stability and response of the PLL frequency synthesizer are mutually contradictory. In the PLL prototyping stage, alternately evaluate the dynamic characteristics of the parameters shown below to design an optimal loop filter that can meet all requirements.

1) Oscillation frequency [Hz]
2) Oscillation power level [dBm]
3) Phase noise characteristic [dBc/Hz]
4) Reference leak (spurious characteristic) [dBc]
5) Lockup time characteristic [sec]
6) Loop bandwidth [Hz]

A PLL frequency synthesizer consists of analog and digital circuits, each of which contains a large number of semiconductor devices. In designing a synthesizer consider component level characteristics and variations in such characteristics for increased production volume.

4-2   Connecting measurement system and target device and necessary setup

A variety of measuring instruments is required to evaluate the performance of a PLL frequency synthesizer:

1) Modulation domain analyzer for lockup time measurement

2) Phase noise measurement system

3) Spectrum analyzer for spurious characteristic evaluation

4) Controller (PC) for controlling the PLL

A measurement system that is even more extensive than a system dedicated to measuring VCO performance is required.

In a conventional method, when it is desired to change the loop filter characteristics or oscillation frequency, connections between the DUT and each of the measuring instruments must be changed. The instrument settings must be changed as well. Evaluation efficiency will be affected. Additionally, when cable connections are changed, attenuation level and other figures at the connector may change. To ensure high repeatability, evaluate the measurement system each time connections are changed. If the system is not evaluated product development time may be extended because of poor design and evaluation inefficiency.

A test is possible with VCO by the applied DC voltage only, but PLL frequency synthesizer is set to a desired frequency by digitally controlling the PLL IC chip.

With the conventional evaluation method, a control circuit is required. An example of a control circuit is a CPU controller within a cellular phone. The control circuit can be built into the final product or a program may be created to run a program that controls the IC chip from an external PC. To practically evaluate the synthesizer, wait until either the control circuit or the program is ready. Further, it is difficult to determine if the measurement starts synchronously when the PLL changes its frequency. Correct the measured lockup time.

4-3   Time and frequency resolution during frequency transient measurement

Conventional PLL lockup time measurement (frequency transient measurement) method is based on the operating principle of frequency counter. (For example, modulation domain analyzer.) In this case, the sampling interval and the measurement frequency bandwidth affect measurement frequency resolution. The problem with it is that if you select a shorter sampling rate in order to trap extremely rapid frequency transient characteristic, you end up obtaining frequency resolution that is inadequate for the frequency to be measured.

5 PLL Characteristic Evaluation Using the 4352S and Features of the 4352S

5-1 All-In-One measurement system architecture

In addition to a variety of measurement functions mentioned earlier for VCO performance evaluation, the 4352S can set up and control PLL frequency synthesizer. It is possible to readily measure all para- meters for PLL performance evaluation other than loop bandwidth. It is possible to measure high-speed SSB phase noise and spectrum without changing con- nections, as shown in Fig.20 and Fig.21. Further, as with VCO parameter measurement, the 4352S's fast phase noise measurement function ensures reduced measurement and evaluation time for substantially improved loop filter design efficiency.
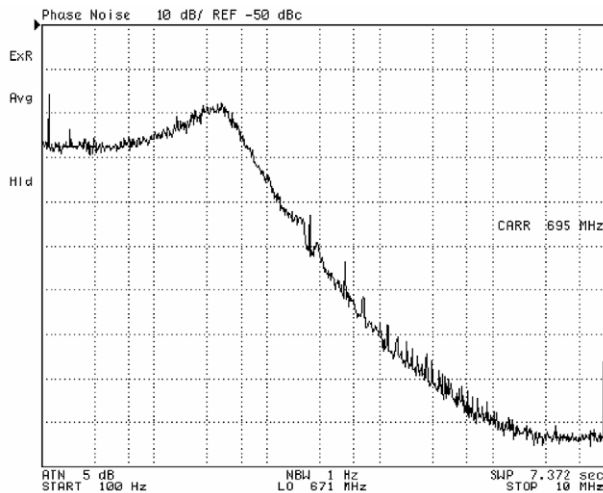

Fig. 20: Example of PLL Phase Noise Measurement Using the 4352S

5-2 Controlling PLL using the IBASIC programming and 24-bit digital I/O functions

When the 4352S is used for testing a PLL frequency synthesizer, it is easy to specify a desired frequency division ratio and make sure that the measurement starts synchronously with frequency change of the target PLL synthesizer. To accomplish this, create a simple program using the built-in IBASIC programming

function and control the target synthesizer through the 24-bit digital I/O feature. No external PC is required. (See Fig. 22) Use the control circuit that will be built into the final product or an external PC to do the same.
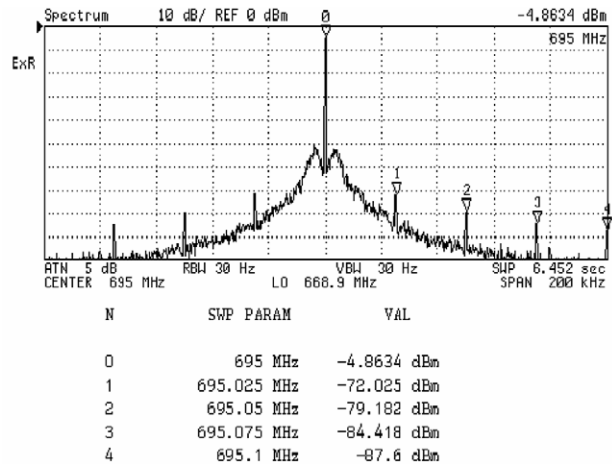

Fig. 21: Example of PLL Spurious Measurement Using the 4352S
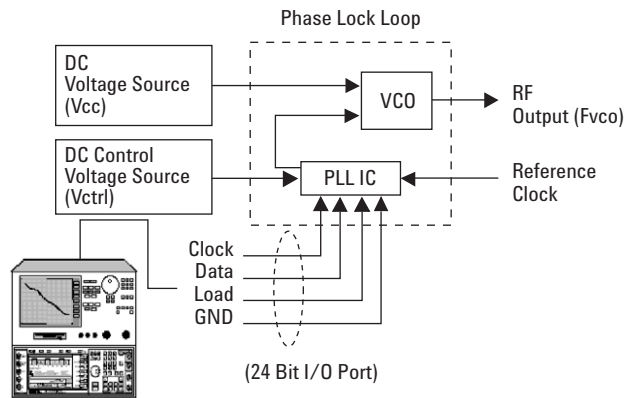
Fig. 22: Conceptual Connection Diagram of the 4352S and PLL Frequency Synthesizer

5-3 Frequency transient measurement function and example of characteristic evaluation

Figure 23 shows the block diagram of the 4352S's fre- quency transient measurement section. The 4352S uses a frequency discriminator to convert frequency to voltage and allows frequency transient measurement with 12.5_sec time resolution and 50 Hz frequency res- olution over the entire measurement frequency range. (See Fig.24.)

Fig. 23: Block Diagram of the 4352S's Frequency Transient Measurement Section

Fig. 24: Example of Frequency Transient Measurement Using the 4352S

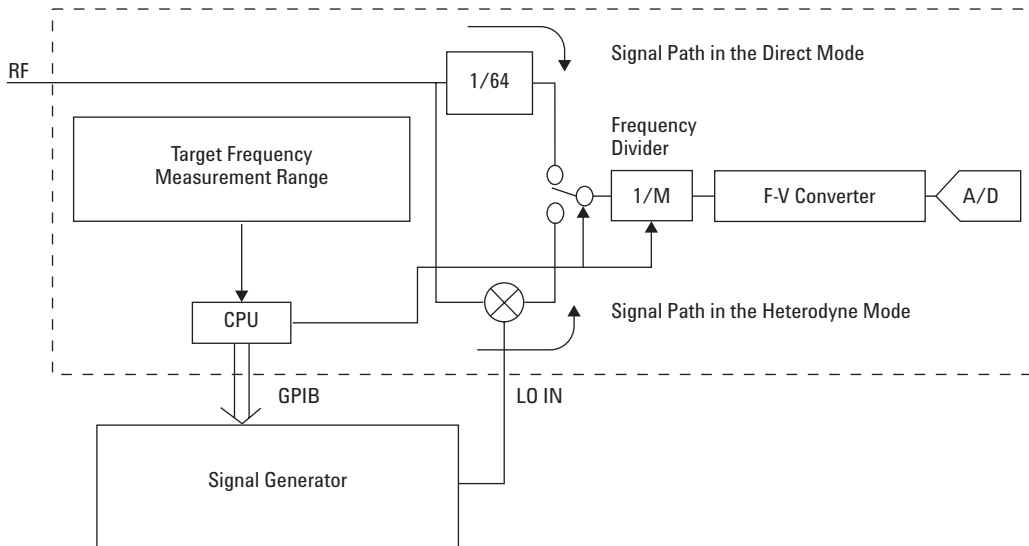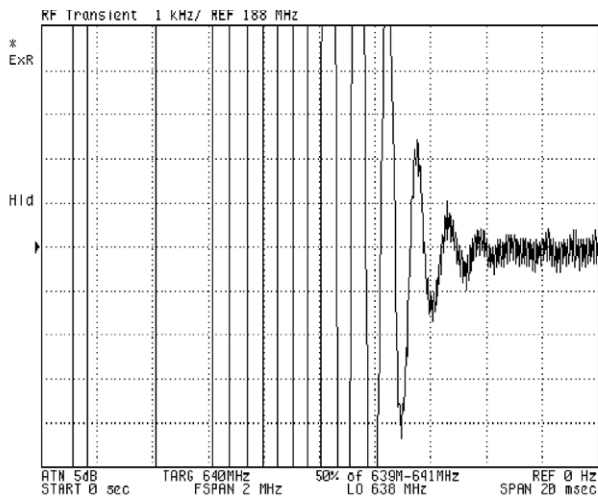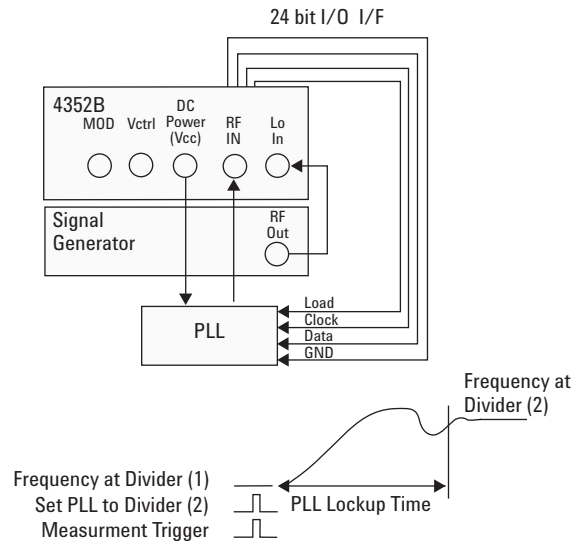**Fig. 25: Cable Connections between the 4352S and PLL Frequency Synthesizer and Timing Diagram from Frequency Setting Change to Measurement Start**

6 Example of PLL Lockup Time Measurement Using the 4352S

6-1 Making cable connections

6-1-1 Outline of PLL connections, frequency change settings, and measurement

Figure 25 shows cable connections between the 4352S and a PLL frequency synthesizer and the timing diagram from the frequency setting change to the end of measurement.

The PLL frequency synthesizer's frequency can be controlled by three signals, namely, CLOCK, LOAD (or LOAD ENABLE / LE) and DATA signals. When the 4352S is used, these signal cables should be connected to the 24-bit digital I/O port as shown in order to utilize the built-in IBASIC programming function to change the PLL frequency setting. Also, the 4352S can send a measurement trigger to itself while at the same time sending

a frequency setting signal to the PLL, thereby initiating the lockup time measurement synchronously (typically 85μsec max.) when the PLL changes its frequency. Thus, the 4352S provides trouble-free PLL lockup time measurement through its frequency transient measurement and synchronization functions of measurement with setting change using the IBASIC programming.

6-1-2 Precautions for making connections

Some PLL frequency synthesizers have parallel data input ports or come with additional control signal lines. The 24-bit digital I/O interface with the general-purpose D-sub/36-pin connector is standard with the 4352B. The 4352B can readily accommodate additional control signal lines. Note that this interface is designed to drive the DUT at the TTL level. If the target device operates at any other logic level, insert a level converter (for example, voltage dividing resistor) between the 4325B and the DUT. Also, use a flat cable or lead wire for connection.

6-2 Controlling PLL through the IBASIC programming and 24-bit digital I/O functions

6-2-1 Specifying frequency division ratio: outline

The format of frequency division ratio data fed to the PLL IC chip may vary in bit pattern depending on individual chips. Use the IBASIC programming function to handle such variations. Many PLL IC chips use the pulse swallow method to determine the frequency division ratio and are comprised of devices such as a reference counter, programmable counter, swallow counter and dual modulus prescaler, as shown in Fig.26.

When a PLL IC chip of similar kind is used, the VCO output frequency can be determined by the following formula:

$$F_{vco}=[(M \times N)+A] \times F_{osc}/R$$

F_{vco}: VCO oscillation frequency
F_{osc}: Reference signal source frequency
M: Prescaler's frequency division ratio
N: Programmable counter's frequency division ratio
A: Swallow counter's frequency division ratio
R: Reference counter's frequency division ratio

Because the phase comparison frequency (Ref_freq), defined in accordance with the PLL frequency synthesizer application, and the reference signal source frequency (Fosc) are known, the frequency division ratio (R) that is an integer fed to the reference counter can be readily obtained as follows:

$$R=INT(F_{osc}/Ref\_freq)$$

Both the programmable counter's frequency division ratio (N) and that of the swallow counter (A) are integers. N must always be greater than A. Because the comparison frequency division ratio (Divide) is an integer obtained by dividing the VCO oscillation frequency (Fvco) by the phase comparison frequency (Ref_freq), the above formula can be used to calculate N and A based on the specified oscillation frequency (Fvco).
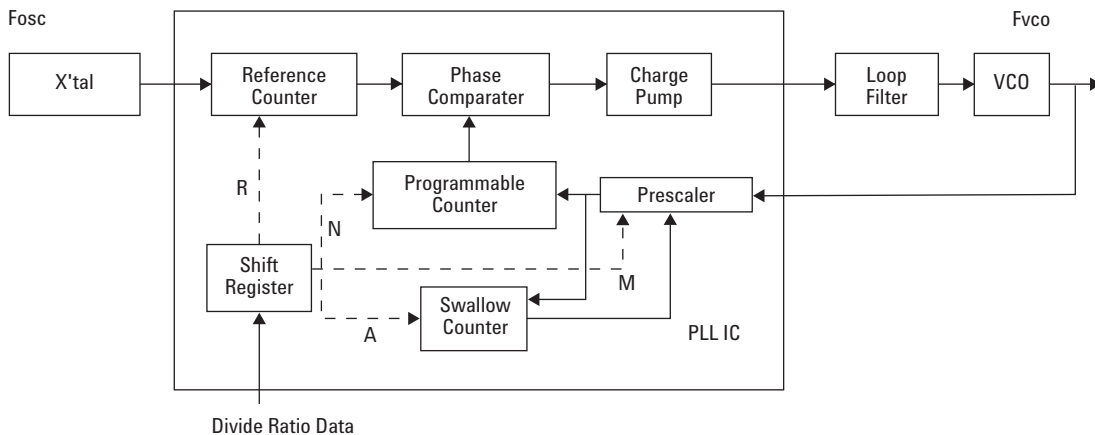

Fig. 26: PLL Internal Block Diagram

Divide=INT(Fvco/Ref_freq)
N=INT(divide/M)
A=Divide: N×M

6-2-2 Example of data format for frequency division ratio

Normally, the PLL IC chip receives the serial frequency division ratio data (integer in binary notation) through its shift register. The data is then fed to the appropriate counter from the shift register through the strobe signal. An example of the frequency division ratio data format for the synthesizer tested by Agilent 4352S is shown in Fig.27.
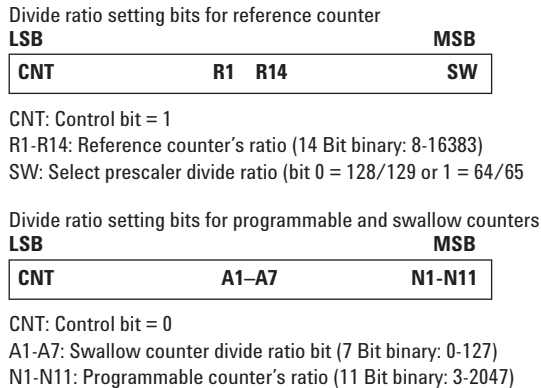
Divide ratio setting bits for reference counter

LSB				MSB
CNT		R1	R14	SW

CNT: Control bit = 1
R1-R14: Reference counter's ratio (14 Bit binary: 8-16383)
SW: Select prescaler divide ratio (bit 0 = 128/129 or 1 = 64/65)

Divide ratio setting bits for programmable and swallow counters

LSB		MSB
CNT	A1–A7	N1-N11

CNT: Control bit = 0
A1-A7: Swallow counter divide ratio bit (7 Bit binary: 0-127)
N1-N11: Programmable counter's ratio (11 Bit binary: 3-2047)

Fig.27: Format of Data Fed to PLL IC Chip (Example)

The content of the CNT bit (LSB) determines which data is sent to the reference counter or to the programmable and swallow counters.

The SW bit (MSB) of the data for the reference counter can be used to select either 128/129 or 64/65 as the prescaler's frequency division ratio. The frequency division ratio data for the reference, programmable, and swallow counters is 14 bits (8-16383), 11 bits (3-2047) and 7 bits (0-127) long, respectively.

6-2-3 Example program for sending ratio data through the 24-bit digital I/O port

This section examines how to change the PLL frequency using the 4352S's IBASIC programming function and the 24-bit digital I/O port. In this example, the A0 (pin 5), A1 (pin 6) and OUTPUT1 (pin 3), available on the 24-bit digital I/O port of the rear panel, are used to output data, clock, and strobe signals, respectively. The GND pin is connected to the ground terminal. At this time, the reference counter's frequency division ratio is sent to the PLL using the following program:

```
180 ASSIGN @Agilent4352 TO 800
190 OUTPUT @Agilent4352;"POSL"
200 INTEGER Pll_reference(1:16)
210 Pll_reference(1)=1
220  FOR I=2 TO 15 STEP 1
230   Pll_reference(I)=BIT(Ref_divider,I-2)
240  NEXT I
250 Pll_reference(16)=1  !Prescaler=64/65
260 !
270 OUTPUT @Agilent4352;"OUT1L"
280  FOR I=16 TO 1 STEP -1
290   WRITEIO 16,0;Pll_reference(I)
300   WRITEIO 16,0;Pll_reference(I)+2
310   WRITEIO 16,0;Pll_reference(I)
320  NEXT I
330  OUTPUT @Agilent4352;"OUT1H"
340 OUTPUT @Agilent4352;"OUT1L"
```

Line 190 selects positive logic for the I/O port.
Line 210 sets the CNT bit to "1."
Lines 220 to 240 contain the reference counter's frequency division ratio (in binary notation) in the array.
Lines 280 to 320 serially sends the ratio to the A0 while at the same time sending "0", "1" and "0" to the A1 to generate a clock signal.
Line 330 sends a strobe signal to the OUTPUT1.
Similarly, you can send frequency division ratios to the programmable and swallow counters using the IBASIC programming function.

6-2-4 Program for PLL lockup time (frequency transient) measurement

To measure the lockup time for a PLL frequency synthesizer, make sure that the measurement starts synchronously when the PLL changes its frequency. With the 4352S use the IBASIC programming function to send a strobe signal to the PLL IC chip synchronously with a measurement trigger. The following shows an example program that changes the PLL frequency from frequency 1 to frequency 2 while at the same time sending a measurement trigger:

```
130 ASSIGN @Agilent4352 TO 800
160 OUTPUT @Agilent4352;"TRGOUT ON"
170 OUTPUT @Agilent4352;"OUT1ENVH"
180 OUTPUT @Agilent4352;"OUT1L"
190 GOSUB Send_pll_freq1
200 OUTPUT @Agilent4352;"OUT1H"
210 OUTPUT @Agilent4352;"OUT1L"
220 GOSUB Send_pll_freq2
230 EXECUTE "SING"
240 OUTPUT @Agilent4352;"OUT1L"
```

"TRGOUT ON" on line 160 turns ON the trigger synchronous output.

Line 170 sends "OUT1ENVH" to make sure that the OUTPUT1 goes high when a trigger synchronous output is received.

Lines 180 to 210 selects division ratio of frequency 1 for the target PLL.

Line 220 sends division ratio of frequency 2 to the target PLL.

Line 230 starts a measurement. At the same time, a strobe signal (high level) is sent to the OUTPUT1 following the trigger synchronous output, thus switching the division ratio of PLL frequency over to frequency 2.

6-2-5 Specifying frequency transient measurement parameters and example of measurement

When frequency transient is measured, it is necessary to predict the frequency that can be obtained based on the division ratio. Specify in advance when to start displaying measurement data, the frequency resolution and measurement frequency range. As mentioned in the previous section, the IBASIC program triggers the measurement. Use keys on the front panel to readily specify measurement parameters.

6-2-6 Procedure for specifying parameters

As shown in Fig.23, two signal paths are available with the 4352S's frequency transient measurement section. One signal path is for the direct mode in which variations in frequency over a wider range can be observed. The other signal path is for the heterodyne mode in which higher frequency resolution is provided a signal path is automatically selected in accordance with specified measurement parameters. The frequency resolution is automatically determined in each mode independently of the sampling time.

To observe the frequency transient characteristic over a wide frequency range, press [TARGET FREQ] and specify a desired center frequency. Then, press [FREQ SPAN] and select "MAX" for measurement frequency range. (At this time, the direct mode is automatically selected.) Press [TARGET FREQ] and enter a desired center frequency (between 64 MHz and 3 GHz). The measurement frequency range and resolution are automatically determined. Note that the upper and lower limit frequencies of one measurement range are included in other measurement ranges as seen in Table 1. Switch to another range as necessary by pressing [TARGET FREQ] or [Ref Freq For Scale].

To observe the frequency transient characteristic with higher resolution, select 20 or 2 MHz for measurement frequency range [FREQ SPAN] (at this time, the heterodyne mode is automatically selected). The frequency resolution is set to 500 Hz for the 20 MHz range and 50 Hz for the 2 MHz range.

Table 1: Measurement Frequency Range, Max. and Min. Frequencies, and Frequency Resolution for Frequency Transient Measurement in the Direct Mode

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Measurement Range (MHz)	128	256	384	512	640	768	896	1024	1152	1280	1408	1536	1664	1792	1920	2048
RF MAX (MHz)	192	384	576	768	960	1152	1354	1536	1728	1920	2112	2304	2496	2688	2880	3000
RF MIN (MHz)	64	128	192	256	320	384	448	512	576	640	704	768	832	896	960	1024
Frequency Span (MHz)	128	256	384	512	640	768	906	1024	1152	1280	1408	1536	1664	1792	1920	1976
Frequency Resolution (MHz)	3.2	6.4	9.6	12.8	16	19.2	22.4	25.6	28.8	32	35.2	38.4	41.6	44.8	48	51.2

6-2-7 Example of PLL lockup time measurement

In this section, examples of how to measure a PLL frequency synthesizer lockup time when the PLL frequency is switched from 680 MHz over to 695 MHz will be examined. This synthesizer has been designed for use in a PDC mobile terminal.

Figure 28 shows an example in which 695 MHz and MAX were selected respectively as measurement range ([TARGET FREQ], [FREQ SPAN]). In this example, the entire frequency transient during switching from 680 to 695 MHz (frequency range: 256-768 MHz) was measured at a total of 81 points with the frequency and time resolutions set respectively at 12.8 kHz and 12.5μsec. In this figure, compare two traces for analysis, one representing the first measurement result (during switching from 680 to 695 MHz) stored in the internal memory and the other representing the second measurement result.

To accurately determine the lockup time it is essential to determine the PLL frequency transient near the target frequency.

Figure 29 shows an example in which 695 MHz and 2MHz were selected respectively as [TARGET FREQ] [FREQ SPAN] to define measurement range. The time span was set at 5m sec. The frequency transient around the target frequency was measured at a total of 401 points with the frequency and time resolutions set respectively at 50 Hz and 12.5μsec. When compared to the waveform obtained with the same measurement range as in Fig.28 (switching from 680 MHz to 695
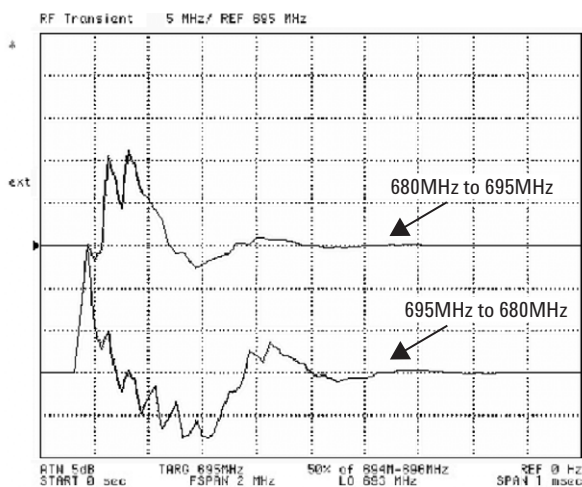
MHz), the waveform in Fig. 29 shows that accurate PLL frequency variations were measured. The variations were measured with the resolution of 50 Hz, in the range where the frequency is converging to the target. Note, however, that aliasing caused by image frequency appears at frequencies outside the measurement frequency range.
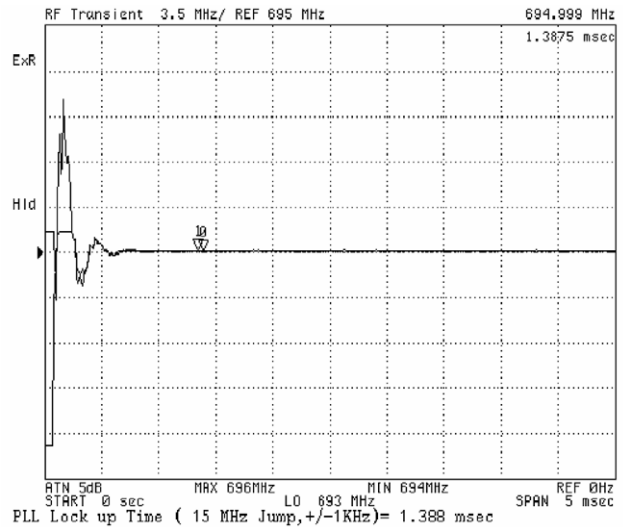

Fig. 29: Example of Frequency Transient Measurement Using the 4352S

Fig.30 shows an enlarged view of the waveform shown in Fig.29. Because part of the waveform near the target frequency is zoomed up, it is possible to perform in-depth evaluation of ringing during a time period immediately prior to the convergence of the PLL frequency. Additionally, it is possible to use your IBASIC program to display markers at the maximum and minimum permissible frequencies for automatic lockup time measurement or use the limit line function to make Pass/Fail judgment of synthesizers under test. In the examples shown in Fig.29 and Fig.30, markers 0 and 1 have been set to appear at 1 kHz below and above 695 MHz, respectively. As a consequence, the lockup time has been automatically measured as approximately 1.39 msec.

The 4352S offers the capabilities (IBASIC programming and 24-bit I/O functions) required to readily specify a desired frequency division ratio for the target PLL frequency synthesizer and make sure that the measurement starts synchronously when the PLL changes its frequency, thus providing efficient lockup time measurement.
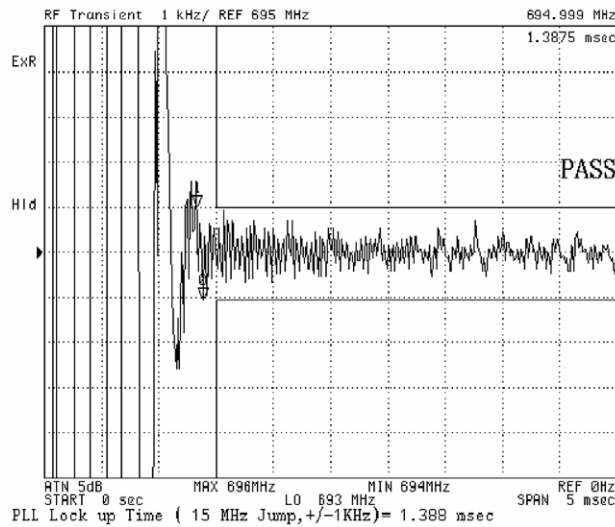

Fig. 28: Example of Frequency Transient Measurement Using the 4352S (Max. Span)

Fig. 30: Example of PLL Lockup Time Measurement using the 4352S

6-3 Spurious and lockup time measurement for designing loop filter

This section examines a measurement example in which parameters required for loop filter design, regarded as the most critical step in PLL design, were measured using the 4352S. A loop filter is a low-pass filter inserted between the phase comparator and the VCO's control voltage input terminal. It eliminates the high frequency component contained in the phase correction pulse generated by the phase comparator and ensures that only the DC component contained in that pulse is fed to the VCO. The lower the loop filter cutoff frequency, the more the reference leak from the phase comparator to be impressed upon the VCO control voltage input is suppressed. As a result, PLL spurious is suppressed at the same time, as shown in Fig.31. Reducing loop filter cutoff frequency does not suppress phase noise near the carrier frequency although the closed loop negative feedback region becomes smaller, as shown in Fig.32.

Further, reduction in loop filter cutoff frequency leads to slower PLL response, thus resulting in longer settling time (PLL lockup time) during frequency switching. Conversely, increasing cutoff frequency provides faster PLL response and therefore shorter PLL lockup time as shown in Fig.33. As a result, phase noise near the carrier frequency is suppressed while reference leak is not. PLL output is frequency-modulated and therefore contains high spurious, as shown in Fig.34.

In practical loop filter design, consider not only phase noise/spurious/PLL lockup time tradeoffs but also varying loop filter frequency characteristic depending on the oscillation frequency and some margin required to handle variations in VCO characteristic. Evaluate spurious level, phase noise and frequency transient in each frequency range under various conditions. Efficiency in evaluation of each of such characteristics provides shorter development period.
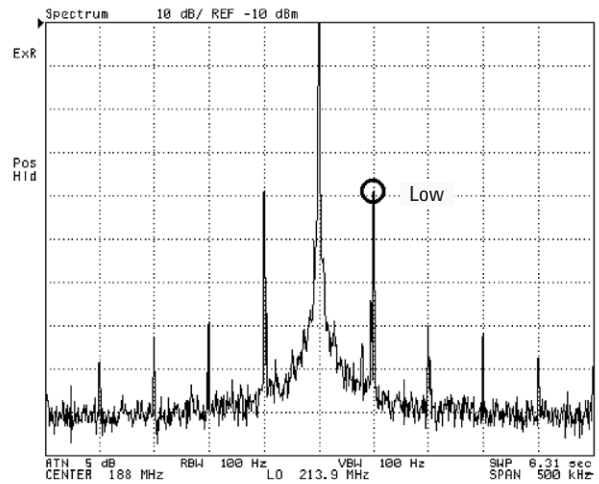

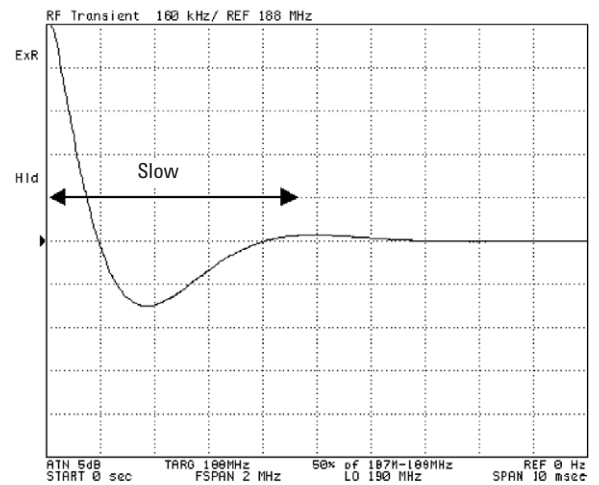**Fig. 31: Example of Spectrum Characteristic with Low Loop Filter Cutoff Frequency**

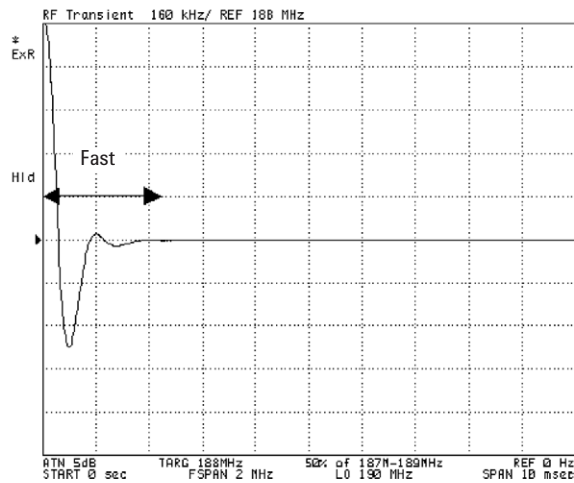**Fig. 32: Example of Lockup Time with Low Loop Filter Cutoff Frequency**

RF Transient 160 kHz/ REF 188 MHz

*
ExR

Fast

Hld

ATN 5dB   TARG 188MHz   50% of 187M-189MHz   REF 0 Hz
START 0 sec   FSPAN 2 MHz   LO 190 MHz   SPAN 10 msec

Fig. 33: Example of Lockup Time with High Loop Filter Cutoff Frequency

Spectrum   10 dB/ REF -10 dBm

ExR

Pos
Hld

High

ATN 5 dB   RBW 100 Hz   VBW 100 Hz   SWP 6.31 sec
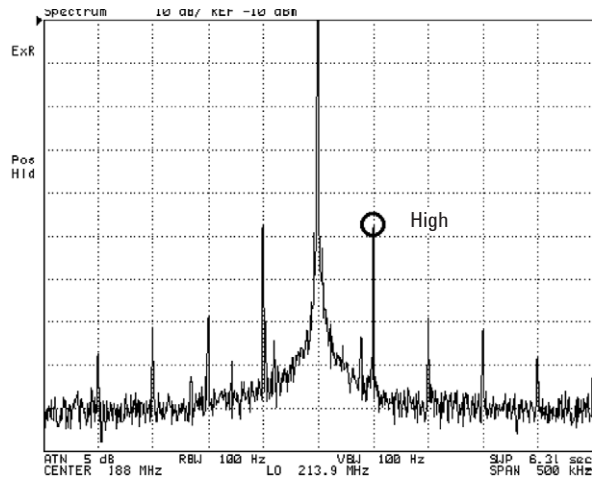CENTER 188 MHz   LO 213.9 MHz   SPAN 500 kHz

Fig. 34: Example of Spectrum Characteristic with High Loop Filter Cutoff Frequency

6-4 Changing and measuring PLL frequency from external PC

In the development stage, some PLL manufacturers supply a program to control PLL frequency synthesizer from the PC. In this case, it is not difficult to change the PLL frequency. To measure the PLL lockup time, make sure that the 4352S triggers frequency transient measurement synchronously when the PLL changes its frequency.

Follow one of the two procedures described below to achieve proper synchronization.

6-4-1 Triggering the 4352B at TTL level from the PC

It is possible to achieve synchronization by sending an external TTL level trigger to the 4352B through the EXT TRIG terminal provided on the rear panel, as shown in Fig.35.
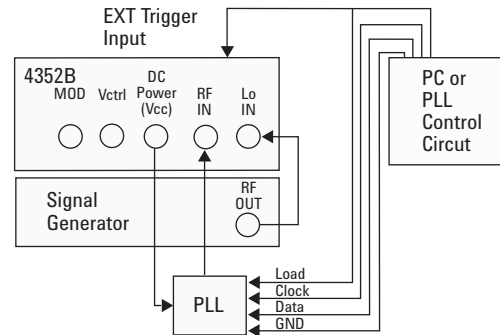

Fig. 35: Cable Connections for Measurement Using the External PC

6-4-2 Using the 4352B's value trigger function

Much like the level trigger available with an oscilloscope, the value trigger function is designed to automatically initiate the measurement synchronously when the PLL frequency input to the RF IN terminal exceeds or falls below the specified frequency. In this case, the 4352S does not start displaying measurement data when the PLL practically starts changing its frequency. It is not necessary to make special cable connections. Simply change the PLL frequency from the PC and evaluate the frequency transient characteristic during a time period immediately prior to the convergence of the PLL frequency. Also, consider conducting continuous testing to detect problems usually associated with early stages of design, including frequency change due to PLL unlocking and frequency variations caused by external noise. Figure 36 shows a connection diagram to use the value trigger function for measurement.
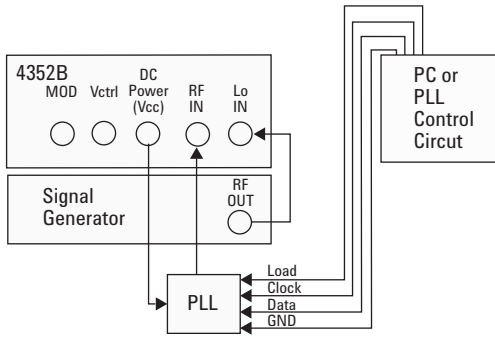
19

Fig. 36: Cable Connections for Measurement Using the Value Trigger Function

7 Microwave VCO Evaluation Using the 43521A Downconverter Unit

Today, cellular phones operating in the band around 2 GHz are increasing in number. To test such phones for signal generator and harmonic frequencies, it is essential that a measurement system be able to measure frequencies beyond 3 GHz. Efforts to use higher frequency signals will continue to accelerate in the future. Examples include the next generation wireless LAN (over 5 GHz), automatic billing system for expressways (ETC) (over 5 GHz) and satellite communication (over 6 GHz).

The conventional evaluation of microwave VCO performance has the following drawbacks:

1) Because the VCO's RF output level becomes smaller with increase in frequency, an amplifier must be provided to amplify the RF output before it is fed to the measurement system, if the RF output level is -10 dBm or less.

2) A microwave reference signal source with excellent phase noise characteristic must be provided for the external downconverter.

3) The local signal from the downconverter leaks out to the RF input, thereby affecting the VCO oscillation characteristic and causing variations in its frequency and output level.

4) A downconverter for use in the microwave region consists of various components including a mixer, amplifier and attenuator. The overall frequency characteristic of all components combined such as frequency gain and loss can vary substantially. Therefore, this frequency characteristic must be corrected. To do this, additional measuring instruments are required to evaluate the characteristic. As a consequence, it takes additional time and cost before VCO's can be tested.

The 43521A is a downconverter that has been designed for use with the 4352S (4352B rev. 02.00 or later) to measure and evaluate RF signals in the 3-12.6 GHz range. Figure 37 shows the block diagram of the 4352S when the 43521A is used.

The 43521A offers the following advantages:

1) Incorporates a low noise amplifier (+20 dB typical) to allow measurement even in the event of low RF output level (20 dBm input). (RF frequency: 2.4 to 12.6 GHz)

2) Incorporates an ultra low phase noise signal generator as local signal source to provide the measurement capability up to 12.6 GHz

3) Comes with a low noise amplifier and attenuator between its input terminal and mixer to minimize impact of local signal on the target VCO

4) Communicates with the 4352B to change its internal switch settings and automatically correct internal gain and loss for highly accurate measurement of RF power at a position very close to the DUT.

The 43521A expands all 4352B's measurement and evaluation functions other than harmonic frequency setting for spectrum measurement (2 x CARR and 3 x CARR) to 12.6 GHz for efficient microwave VCO design.

Connecting a downconverter such as Agilent Technologies 71707A that is capable of handling even higher frequencies can make measurement of phase noise at frequencies beyond 12.6 GHz. (26.5 GHz max. for the 71707A) Note, however, that the DUT's RF output level is not legible on the 4352S. Use a power meter (for example) to correct the output level and become sufficiently familiar with the frequency characteristics (internal gain and loss) of the external downconverter before making the measurement.
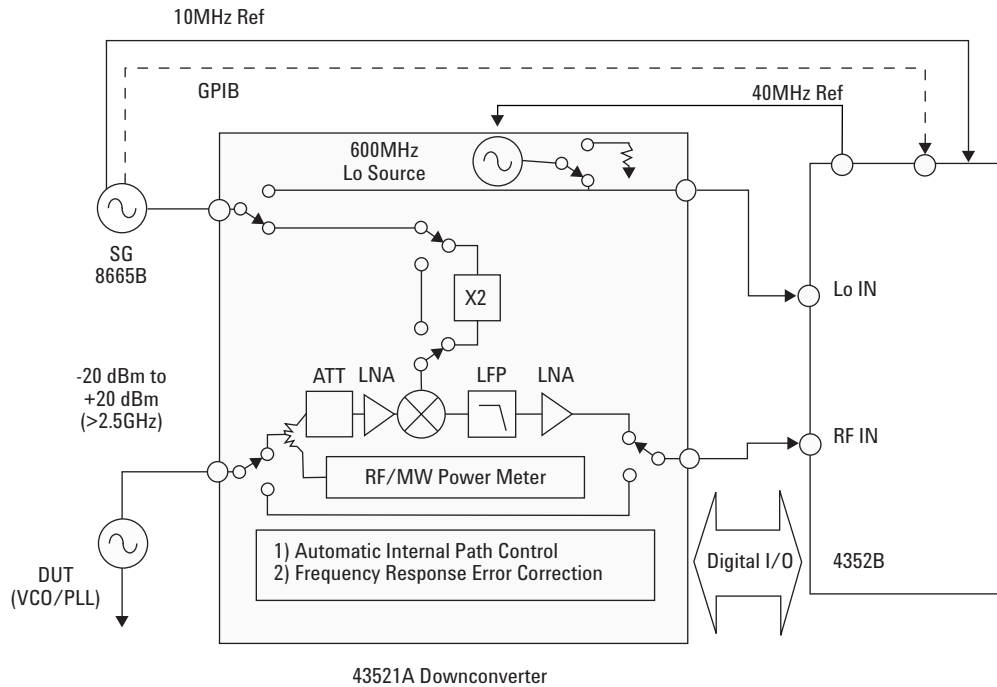
Fig. 37: Block Diagram of the 43521A Microwave Downconverter

8 Considerations for Configuring Optimal 4352S System

8-1 Selecting local signal source (standard signal generator) for the 4352S

To configure an optimal measurement system, select a local signal generator carefully to provide the appropriate overall system performance. This section examines the requirements for selecting a local signal source for the 4352S.

Consider the following when making a selection:

1) Make sure that the signal generator covers the required frequency range.

To measure harmonics as well as carrier frequency, it is essential that the signal source cover the target harmonic frequency range.

2) Select a signal generator that has sufficiently superior phase noise characteristic than that of DUT. Some signal generators offer excellent phase noise characteristic at frequencies around carrier

frequency while others are highly effective at high offset frequencies. Check that the signal generator's phase noise characteristic at the target carrier frequency is better than DUT over the entire target offset frequency range.

Normally, signal generators change in phase noise characteristic at offset frequency with change in oscillation frequency. Compare the phase noise characteristic of the DUT with that of the measurement system. Also, consider future DUT's with improved phase noise characteristic when configuring a measurement system.

Table 2 shows recommended signal generators for the 4352S. Note that signal generators for use with the 4352S are classified into 4 types depending on the GPIB control commands as follows:

SG TYPE 1: SCPI (HP-SL) command type
   (HP-SL: Hewlett-Packard System Language,
   IEEE 488.2-1987)
SG TYPE 2: 8657B command type
SG TYPE 3: SCPI command type (ver. 1992.0)
SG TYPE 4: Others

In addition to the signal generators listed in table 2, there are a number of other signal generators that support GPIB control commands of SG TYPE 1 to 3. For more information, please contact a regional Agilent Technologies sales office.

Even if the signal generator does not support any of SG TYPE 1 to 3 control commands, it may be possible to use SG TYPE 4. With SG TYPE 4, GPIB commands, used to control the signal generator frequency, are stored in the 4352B in advance. Once the commands are stored, they remain stored even if the 4352B is turned OFF, thus allowing control of the signal generator frequency similar to other signal generators. Note, however, that in this case the signal generator must be set up manually or by using a GPIB command at power-on such that the output level is maintained constantly at +10 dBm.

8-2 Correcting variations in RF power level caused by cable extension or amplifier

The cable connected between the DUT and the 4352S's RF IN terminal may attenuate RF power. On the other hand, if the DUT's RF power level is extremely low, use an amplifier to increase the power level. It is possible to correct variations in RF power level within the target carrier frequency range in advance. To make corrections, follow the following steps.

1) Use a network analyzer to measure in advance the attenuation level by the cable and the amplification level by the amplifier and determine the frequency characteristic (slope) for each of the attenuation and amplification levels at each of 0 Hz (DC) and 1 GHz.

2) Enter the obtained data as parameters for the 4352S's cable loss correction function.

8-3 RF power measurement error caused by distorted RF signal waveform

If the DUT's RF signal contains significant harmonic component, the RF power level at the carrier frequency may not be measured accurately. This is because the 4352S has a diode detector (peak detector) immediately after the RF IN terminal to provide high-speed measurement of RF power. In this case, it is possible to accurately measure the RF power output level of the fundamental frequency by adding a low-pass filter and extracting only the fundamental frequency. If a low-pass filter is utilized, use a network analyzer to determine the insertion loss characteristic of the filter and enter the data as parameters for the 4352S's cable loss correction function as done with the RF cable extension for accurately legible RF power level.

Table 2: Standard Signal Generator Recommended for the 4352S and Specification

Signal Generator (with Option)	4352S Frequency Range (when 43521A is used)	Phase Noise (typical)	SG type No.
8664A Option 004	10MHz to 3GHz (10MHz to 6.6GHz)	-135dBc/Hz (@ 10kHz offset at 1 GHz)	1
8665A Option 004	10MHz to 3GHz (10MHz to 9.0GHz)	-134dBc/Hz (@ 20kHz offset at 1 GHz)	1
8665B Option 004	10MHz to 3GHz (10MHz to 12.6GHz)	-134dBc/Hz (@ 20kHz offset at 1 GHz)	1
8644B Option 002	10MHz to 2.06GHz	-136dBc/Hz (@ 20kHz offset at 1 GHz)	1
8657B	10MHz to 2.06GHz	-125dBc/Hz (@ 10kHz offset at 1 GHz)	2
E4425B	10MHz to 3GHz	-134dBc/Hz (@ 20kHz offset at 1 GHz)	3

Conclusion

This application note provided an introduction to the problems associated with VCO and PLL performance evaluation, a step essential for PLL frequency synthesizer design and development, and solutions to these problems. It also includes examples of characteristic evaluation using the 4352S.

Improved product performance, shorter product development period, and lower development cost are only some of the challenges that are constantly demanded of the mobile communication industry, one of the most competitive markets today.

The 4352S provides fast and accurate measurement of evaluation parameters for efficient evaluation of PLL frequency synthesizer and VCO performance and contributes to shorter overall lead times, including production and quality inspection for value-added and highly profitable products.

References

- Masafumi Hagiwara and Yuichi Suzuki. "Practical PLL Frequency Synthesizers."(Japanese) Sogo Denshi Shuppan, 1995.
- "VCO Designer's Handbook." Mini-circuits.

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