Agilent E5052B Signal Source Analyzer

Boosting PLL Design Efficiency

From free-running VCO characterizations to closed-loop PLL evaluations

Application Note

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Introduction

A phase-locked loop (PLL) technique is widely used in today’s advanced communications and broadcasting systems, and PLL frequency synthesizers are an indispensable part of the system. Recent advances of higher data rates and more channels per unit of bandwidth have accelerated the need for higher performance PLL frequency synthesizers.

The requirements of modern PLL synthesizers are becoming stricter in terms of frequency stability, frequency switching speed, phase noise and reliability as well as in size, weight and power consumption. These constraints make PLL synthesizer design more challenging and time-consuming.

This application note tells you how to design and evaluate PLL synthesizers more efficiently. Examples also show how related PLL system components such as voltage controlled oscillators (VCOs), reference oscillators and frequency dividers/prescalers are characterized and evaluated.

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1. PLL Synthesizer Basics

A typical PLL frequency synthesizer consists of several key components, shown in Figure 1. Although pure digital PLLs have become popular in recent compact systems, analog VCOs and loop filters are still commonly used in many signal sources. Evaluating VCO performance is the first step toward designing a better PLL synthesizer. The second step is to design the optimal loop filter for lower phase/spurious noise and faster frequency transient response.

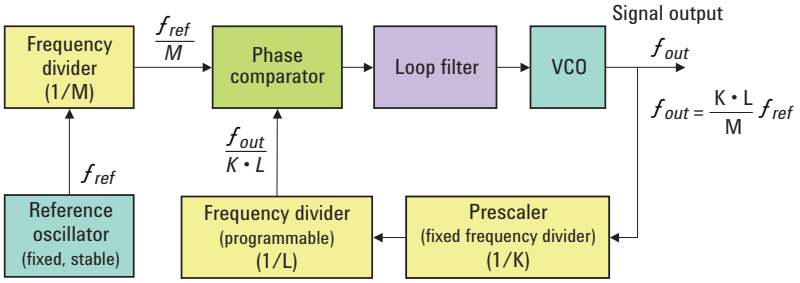
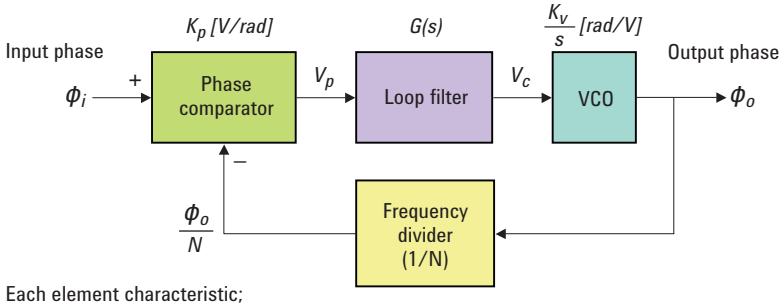


Figure 1. Basic block diagram of a typical PLL frequency synthesizer

Figure 2 shows a simple model of a PLL including the transfer function G(s) of a loop filter. The total performance of the PLL (for example, frequency stability, phase noise floor, frequency switching time, and phase settling time) mostly depends on the reference oscillator phase noise, VCO phase noise, frequency divider noise floor, set-up time of the divider number, and loop gain including G(s).



Each element characteristic;

Phase comparator: $V_p(s) = K_p \cdot \{\phi_i(s) - \phi_o(s)/N\}$ assuming *Kp [V/rad]* is constant

Loop filter: $V_c(s) = G(s) \cdot V_p(s)$

VCO: $\phi_o(s) = K_v \cdot V_c(s)/s$ assuming *Kv [rad/sec/V]* is constant

Closed-loop characteristic of the PLL model:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{\frac{K_p \cdot K_v \cdot G(s)}{s}}{1 + \frac{K_p \cdot K_v \cdot G(s)}{N \cdot s}}$$

where *s* is a differential operator (complex angular frequency)

$\frac{-K_p \cdot K_v \cdot G(s)}{N \cdot s}$ is the loop gain of the PLL

Figure 2. Simple PLL model

Once the model (or each block) is identified, a simple design flow such as the one shown in Figure 3 is used to characterize all components and optimize the whole synthesizer design including the loop filter.

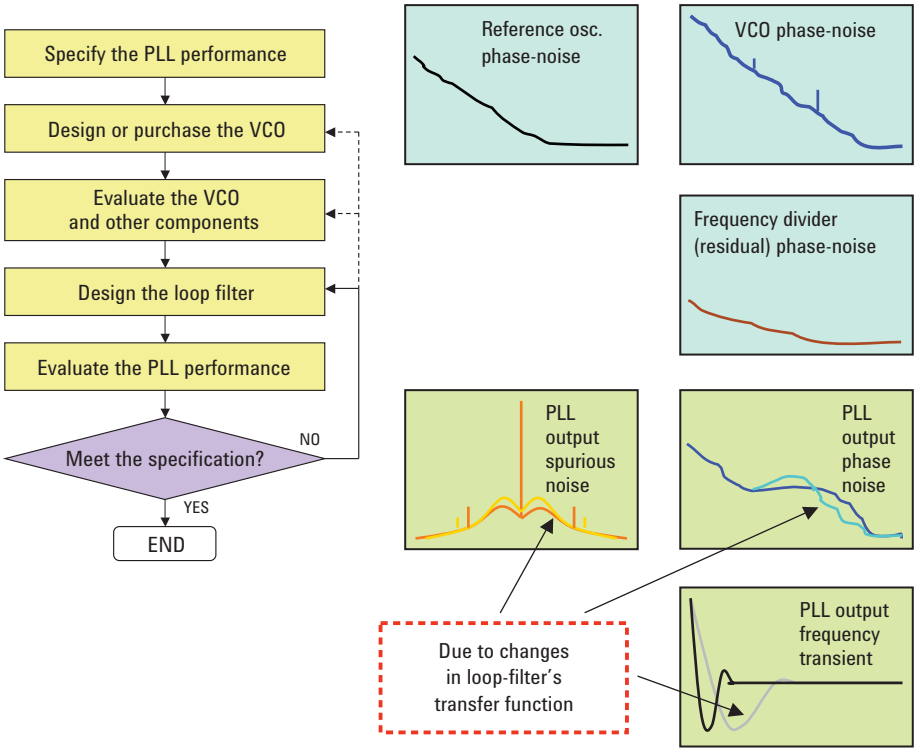


Figure 3. PLL design flow and loop filter optimization

2. VCO Characterization

2-1. VCO characteristic parameters to be measured

A typical VCO is a three-port device that has a DC power supply port, a tuning (DC control voltage) port and a signal output port. Sometimes the tuning port and or output port may be differential. Therefore, in order to characterize a VCO you need at least 2 (low noise) DC sources and one signal analyzer which can measure power, frequency, phase-noise, and so on. You may need additional DC multimeters to accurately measure the tuning voltage and current consumption of the DC power supply.

Frequently specified or characterized VCO parameters are as follows:

1) Output signal frequency [Hz] at specified tuning voltage points
   – Tuning characteristic: output signal frequency vs. tuning voltage
2) Tuning sensitivity [Hz/V]
   – Derived from the tuning characteristic: (Δ frequency)/(Δ tuning-voltage) vs. tuning voltage
3) Output signal power level [dBm] at specified frequency points or tuning voltage points
   – Power level variation: output signal power level vs. tuning voltage
4) Phase noise [dBc/Hz] at specified offset frequencies from a carrier frequency
   – Phase noise spectrum: phase noise spectral density vs. offset frequency

5) Residual FM [Hz rms] at a specified band of offset frequency
6) Amplitude noise (AM noise) [dBc/Hz] at specified offset frequencies from a carrier frequency
   – Amplitude noise spectrum: amplitude noise spectral density vs. offset frequency
7) Spurious noise or signals [dBc]
8) Harmonics of the output signal [dBc]
9) Consumption current from the DC power supply [A]
10) Input current of the tuning (DC control) voltage port [A]
11) Load pulling characteristic in frequency change [Hz p-p] or power level change [dBm p-p]
   – Frequency change or power level change vs. mismatched load magnitude/phase change
12) Oscillator pushing characteristic in frequency change [Hz/V] or power level change [dBm/V]
   – Frequency change or power level change vs. DC power supply voltage change
13) Tuning delay [sec]
   – VCO frequency response (time constant) when an ideal abrupt tuning voltage is applied
14) Power-on settling time [sec] or warm-up time [sec]
   – Settling time of output signal frequency or amplitude after power-on in a specified range
15) Temperature characteristics of each parameter

It is generally difficult and very time consuming to evaluate all of these parameters manually using only a few instruments. In 1994, Agilent Technologies introduced the first dedicated VCO/PLL tester, the 4352A, to solve the difficulty of VCO parameter measurements. The current E5052B signal source analyzer is a successor to the 4352A which includes many enhanced functions.

The E5052B has two low-noise internal DC sources that provide quick and stable automatic measurement of tuning/pushing characteristics. The E5052B can measure 10 MHz to 7 GHz carrier signals with 100 MHz or 40 MHz offset frequency in phase noise or amplitude noise respectively. Also the baseband noise spectrum (from 1 Hz to 100 MHz) can be observed for evaluating the DC source noise, which often affects VCO phase noise performance.

Advanced phase noise and transient response measurement techniques in the E5052B are described in another application note[1], and, how to extend E5052B's frequency range up to microwaves (26.5 GHz) and even to millimeter-waves (110 GHz) is provided in other documents[2]. This application note describes fundamental measurement configurations and potential problems to be aware of when characterizing the VCO parameters listed above with the E5052B signal source analyzer.

2-2. How to tame a free-running VCO

It is not easy to measure the phase noise of a free-running VCO accurately since the output frequency of the VCO under test always fluctuates even when the control voltage is ideally stable. The frequency fluctuation (often called frequency drift) causes signal phase instability called jitter (in the short term) or wander (in the long term) that may degrade the output signal quality of the PLL frequency synthesizer.

1. Refer to the "Literature References" section at the end of this document, number 1.
2. Refer to the "Literature References" section at the end of this document, numbers 2 and 3.

Figure 4 shows the frequency fluctuation of a free-running VCO as observed with a spectrum analyzer.

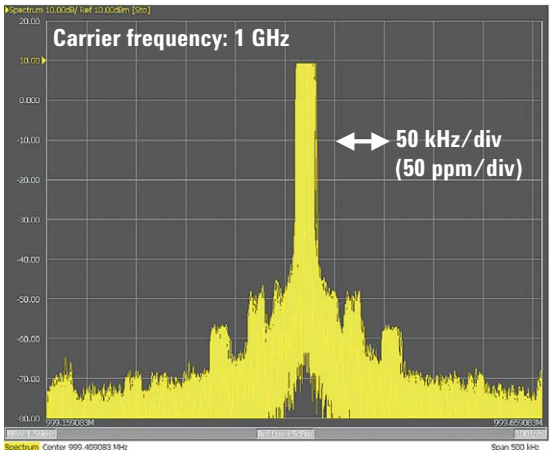
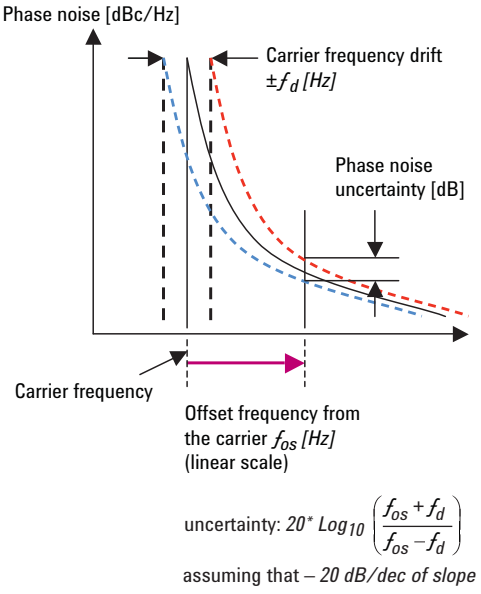


Figure 4. Drift of a free-running VCO at 1 GHz (for 30 seconds)

The frequency fluctuation of the free-running VCO generates a large amount of phase noise measurement uncertainty as shown in Figure 5. The output signal frequency is supposed to be stable enough to take the phase noise measurement. However, because phase noise measurements (especially at offset frequencies below 100 Hz) usually take a few seconds to a few minutes, it is not practical to keep the frequency at a sharp, fixed point during the measurement. Therefore, some kind of phase lock technique or drift cancellation technique should be used to overcome this difficulty.[1]



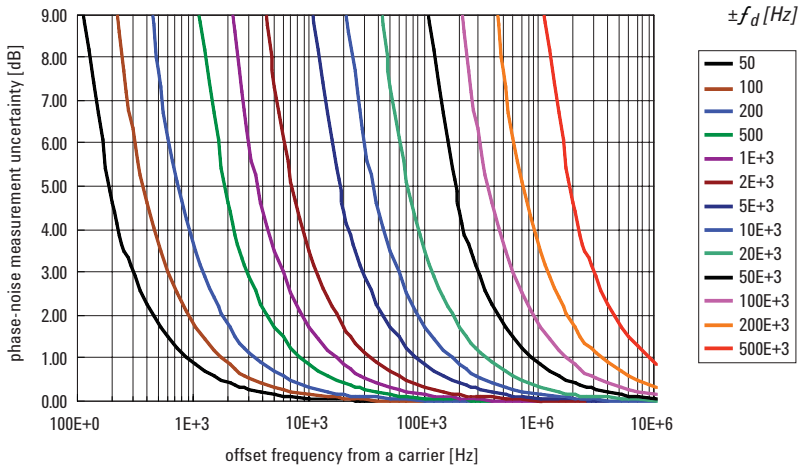


Figure 5. Impact of carrier fluctuation on phase noise measurement uncertainty

1. Refer to the "Literature References" section at the end of this document, numbers 1 and 4.

The E5052B uses a PLL (direct homodyne) method and a heterodyne digital frequency discriminator method to "tame" the frequency fluctuation of the free-running VCO under test. As shown in Figure 6, this simplifies the measurement configuration for phase noise, amplitude noise, tuning characteristics and oscillator pushing characteristics.

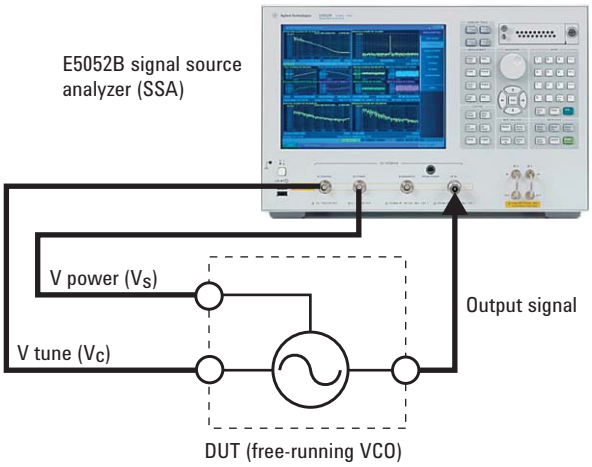


Figure 6. Measurement configuration for testing a free-running VCO

2-3. Tuning characteristics

Several tuning characteristics such as frequency, power level, consumption current and tuning sensitivity can be measured and displayed simultaneously by using the E5052B in the Freq & Power mode (see Figure 7). Each graph with markers is expandable to a full screen size for further analysis.

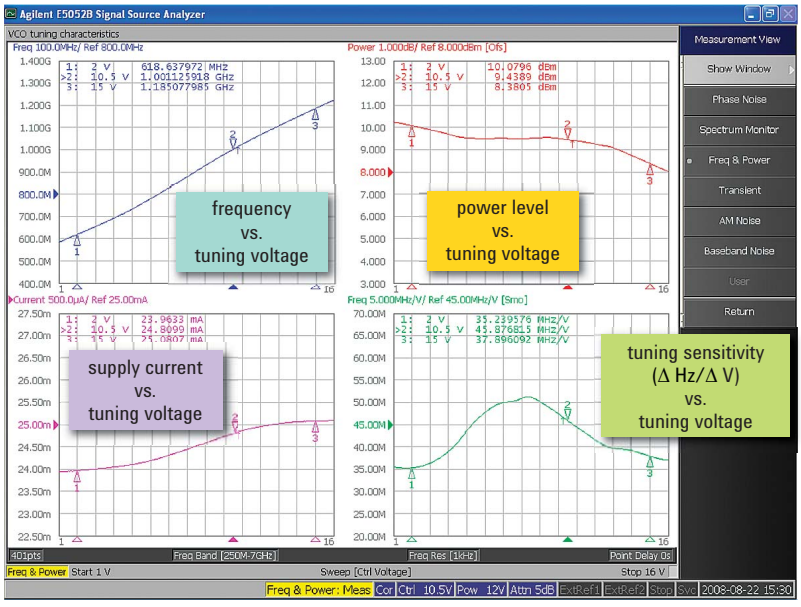


Figure 7. Frequency and power measurements

Figure 8 shows an example of a phase noise measurement result of a 1 GHz carrier frequency. Several spurs are identified (in black) with random noise spectrum (in blue). X-axis band marker analysis (band markers are shown as blue flags) shows the calculated values of equivalent RMS jitter in pico-seconds and residual FM in Hz; these are based on integrated phase noise from 2 kHz to 20 MHz offset frequency (i.e. by filtering with an ideal rectangular filter from 2 kHz to 20 MHz).

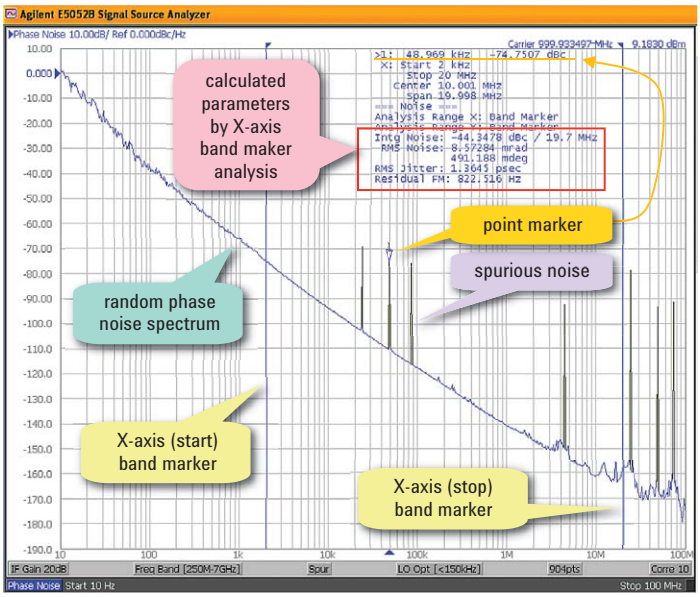


Figure 8. Phase noise spectrum measurement

You can easily set an arbitrary integral filter shape if the rectangular filter given by the X-axis band marker analysis function is not appropriate. Figure 9 shows an example of filtered phase noise spectrum using a band pass filter with 2 kHz low-end cutoff (+40 dB/dec) and 20 MHz high-end cutoff (–20 dB/dec). The E5052B's 'User Equation' function calculates RMS jitter and residual FM over the filtered spectrum from 10 Hz to 100 MHz.

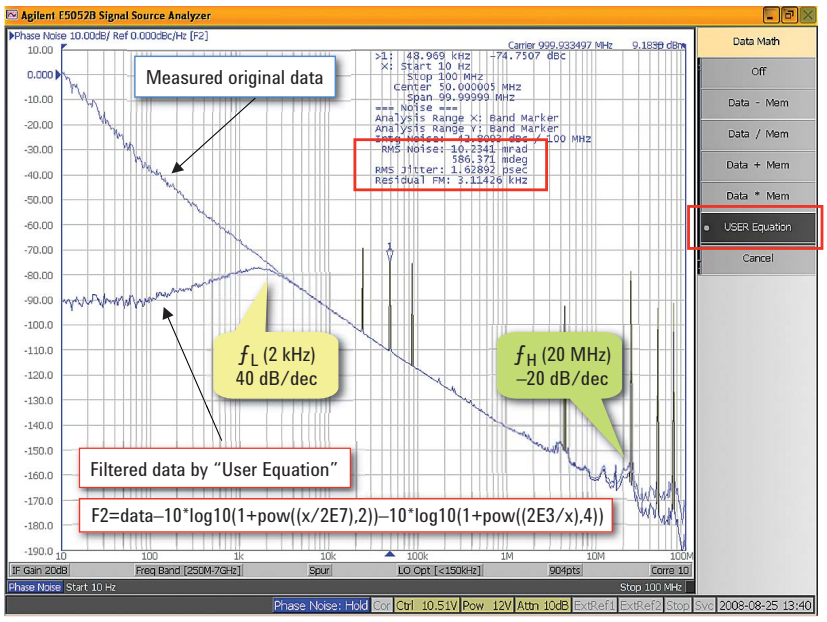


Figure 9. Filtering the measured spectrum

Random phase noise spectrum (in blue) and amplitude noise spectrum (in red) can be displayed on the same scale of dBc/Hz as shown in Figure 10. It should be emphasized that a traditional spectrum analyzer cannot separate both spectrums from each other, but the E5052B can distinguish the phase noise from the total modulation noise (PM + AM noise) with reasonable floor sensitivity (< –170 dBc/Hz).

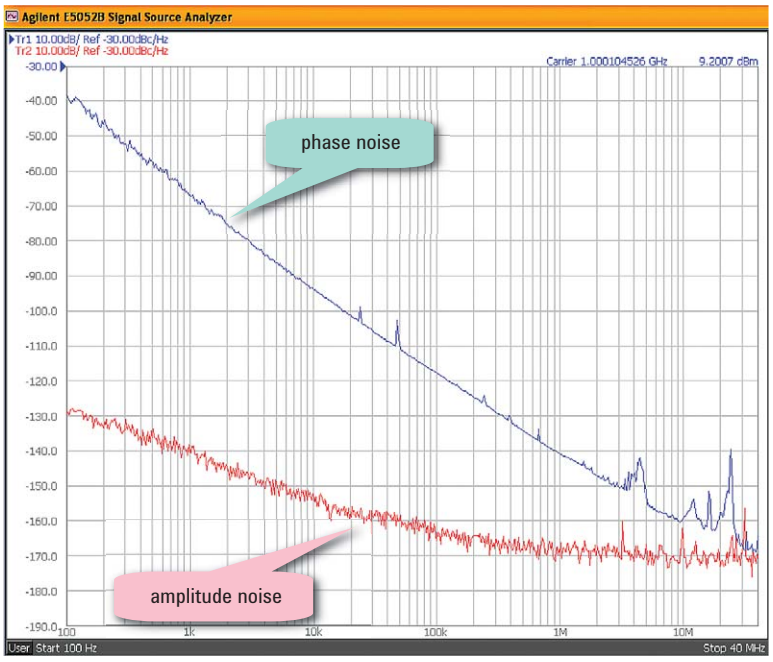


Figure 10. Phase noise and amplitude noise comparison

2-4. Oscillator pushing characteristics

Oscillator frequency changes are caused by small changes of DC power supply voltage(s), which is usually called “oscillator pushing” or “oscillator frequency pushing”. Therefore, oscillator (frequency) pushing is expressed in Hz/V, and is based on the calculation of Δ frequency/Δ supply voltage. Power level changes at the oscillator’s signal output, caused by the same factor, are sometimes called “oscillator (power) level pushing” and are expressed in dBm/V. However, this is not as common.

Changes in the DC power supply voltage may be caused by some static offset (dispersion) around a nominal value or random noise with some ripples of particular frequencies. The former causes a shift in the frequency tuning characteristic and the latter results in some degradation of the phase/amplitude noise spectrum. If a VCO circuit has poor power supply rejection ratio (PSRR) a small amount of voltage fluctuation in a DC power supply may contaminate the output signal significantly.

Oscillator pushing characteristics are evaluated using the same E5052B measurement configuration as the tuning characteristics. However, when measuring oscillator pushing characteristics, the DC power supply voltage is used instead of the tuning (control) voltage. The DC power supply voltage is changed to a specified tolerance range. Figure 11 shows an example of oscillator pushing of a 1 GHz carrier when the DC power supply voltage changes ±1 V at 12 V (nominal voltage).

V_{tuning} = 10.5 V

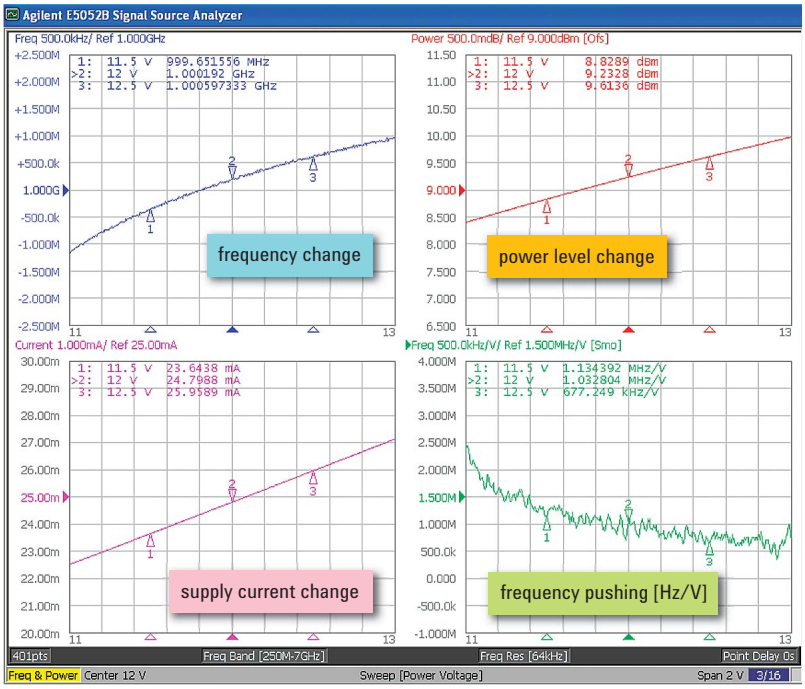


Figure 11. Oscillator pushing characteristics

The frequency shift due to the supply voltage change is caused by a number of different mechanisms[1], including;

(1) changes in device capacitance values due to modified reverse-biased junction capacitances
(2) changes in the oscillator's self-limiting characteristics
(3) changes in the active device gain of the oscillator
(4) changes frequency-determining elements like varactors
(5) changes in AM to FM conversion effects

Therefore, identifying oscillator pushing factors with one-to-one diagnostics among many root causes may be very time-consuming.

You should always use a stable and quiet (low-noise and small ripple) DC power supply to operate a low-noise VCO in order to create a low-noise PLL frequency synthesizer. Additional DC voltage regulators and/or filters should be considered only if a relatively poor DC power supply is used.

2-5. Low noise DC sources are required for precise VCO characterization

As described partially above, low-noise DC sources for the control and supply voltages are necessary when precise measurements of VCO characteristics are needed. Usually 1 nVrms/sqrt (Hz) to 10 nVrms/sqrt (Hz) of random noise floor level is preferable. A corner frequency of 1/f random noise should be below 10 kHz or as low as possible. Spurious noise or ripples at constant frequencies should also be very small (say less than 100 µVrms).

It is important to suppress DC power supply spurious noise above 10 kHz because it is easier to discover low-level spurs (spurs that are uncorrelated to the spurs and ripples of the DC power supply used) in phase noise at the offset frequency range beyond 10 kHz, where random noise is usually diminishing. A proper low-pass filter is sometimes inserted to reduce the high-frequency noise of a poor DC power supply.

Figure 12 shows a typical example of the phase noise difference between a noisy DC power supply and a low-noise DC power supply used. The comparison of noise spectrum for both the DC power supply output and the oscillator output is shown in Figure 13. You can easily identify the similarity between the DC supply noise spectrum and the output signal phase noise spectrum from these figures. This information gives you some hints on how to reduce phase noise level by improving DC power supply noise.

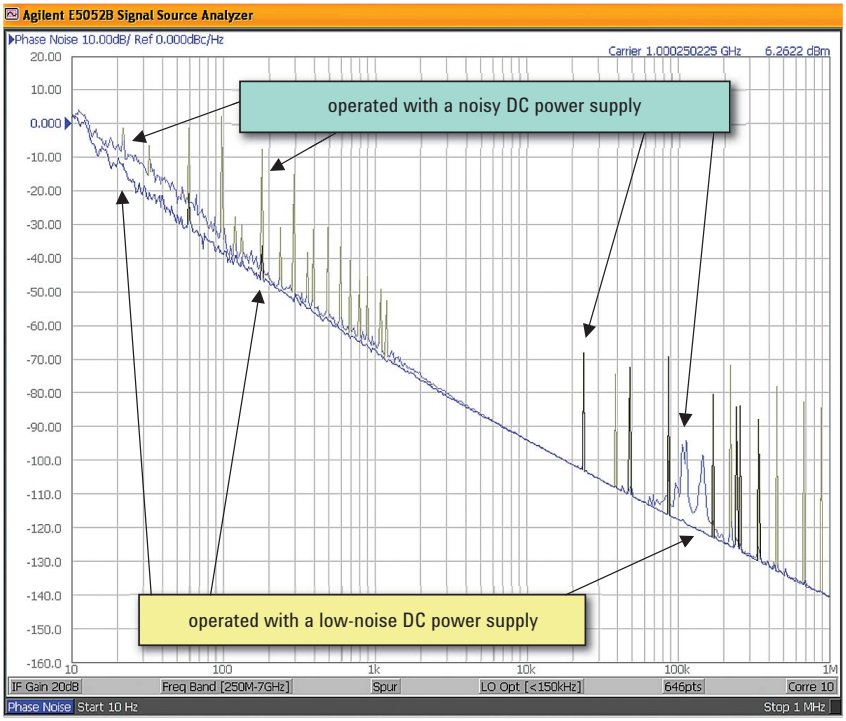


Figure 12. Impact of DC power supply noise on the phase noise spectrum

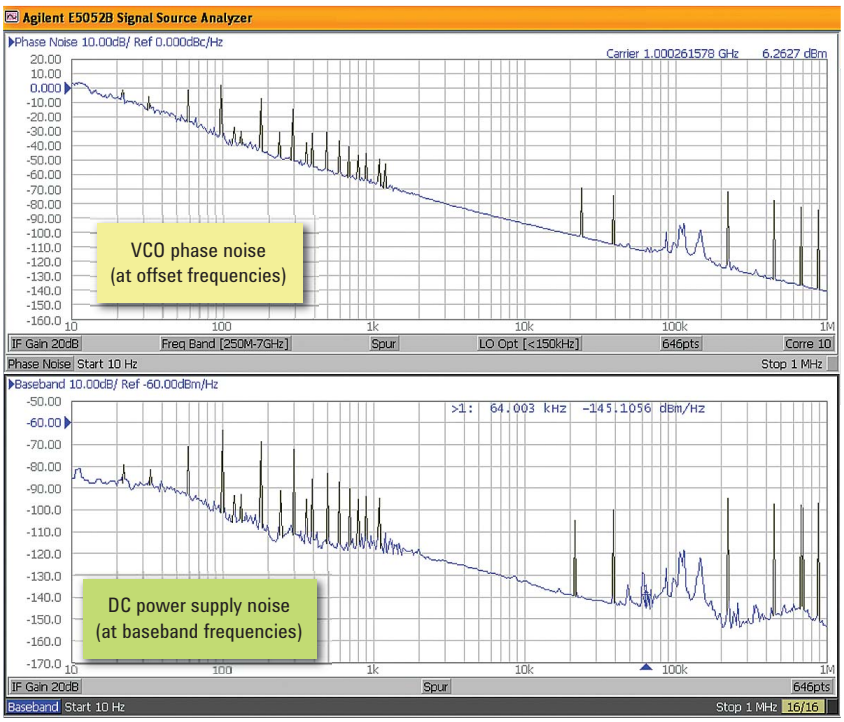


Figure 13. Relation between phase noise and DC power supply noise

Sometimes to evaluate a DC power supply's ripple impact on VCO phase noise, you can superimpose a ripple signal at a particular frequency onto the supply voltage on purpose. Figure 14 shows a typical configuration using a bias-tee circuit in order to add a ripple to the supply voltage. Component values of the bias tee are not critical because the E5052B, in the Baseband Noise Analysis mode, bias-tee can measure the ripple level accurately. You should set the injected ripple level at 1 to 3 mVrms (at most).

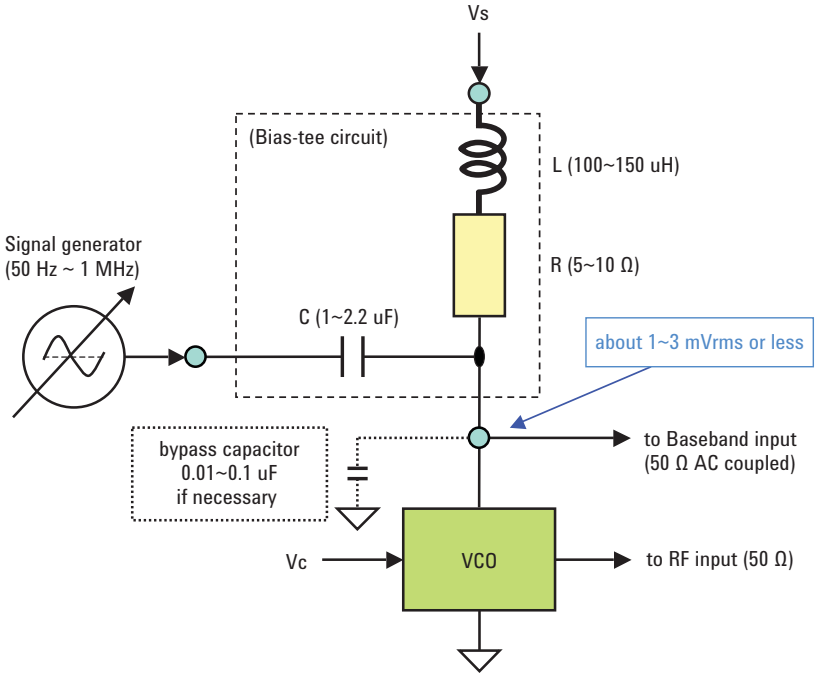


Figure 14. Superimposing a ripple on Vs

Of course, the noise of a DC control voltage (tuning voltage) source must be restricted more carefully.

Because the E5052B has an extremely low noise DC control voltage source (about 1 nVrms/sqrt (Hz) at 10 kHz), additional noise-eliminating filters are not needed for most VCO tests. However, a high output frequency signal may leak through the tuning port of the VCO under test. When this happens, some high-frequency signal reflection may take place between E5052B's DC control port and VCO's tuning port due to impedance mismatch at both ends of the connection cable. This phenomenon consequently affects VCO's output signal quality, in particular, frequency changes and power level changes.

If this occurs, insert a low pass filter (with a 100 kHz to 1 MHz cutoff frequency) at the tuning port of the VCO under test as shown in Figure 15.

A shielded filter and coaxial cables are recommended for this purpose. Note, a bypass capacitor which is connected to the inside and/or outside the VCO power supply port (Vs) is not shown in the Figure 15.

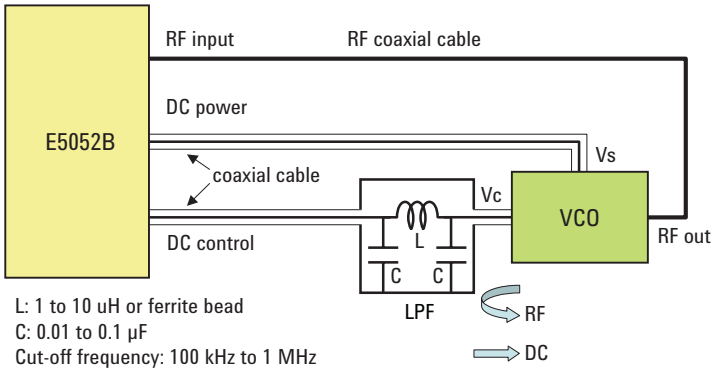


Figure 15. Example of an RF blocking filter in the DC control path

For testing high-performance VCO's, the two low-noise DC sources equipped in the E5052B are very versatile. However, ultra-low noise DC sources are not used to operate VCOs or PLL synthesizers in the actual equipment under real-operating conditions. So, you will need to evaluate two characteristics in advance: the VCO operating using a low-noise DC power supply like E5052B's and the actual DC power supply that will be used in the actual equipment. Then you can compare VCO's performance both under the current operating conditions and under the potentially better conditions in regards to DC source noise.

2-6. Load-pulling characteristics

The change of oscillator output signal frequency that occurs due to a change in load impedance is usually referred to as “load pulling” or “oscillator frequency pulling”. If the load impedance change is dynamic (i.e. time-variant), load pulling leads to direct frequency modulation of the oscillator[1].

If the load impedance change is static, then load pulling causes some fluctuation in the sensitivity of a free-running VCO. This sensitivity change can cause a loop gain change in total PLL performance.

A typical recommended configuration for load pulling measurement is shown in Figure 16. If the output power of the VCO is relatively small (less than 0 dBm) an additional pre-amplifier may be needed in front of the RF input port since the coupler gain is normally –20 dB.

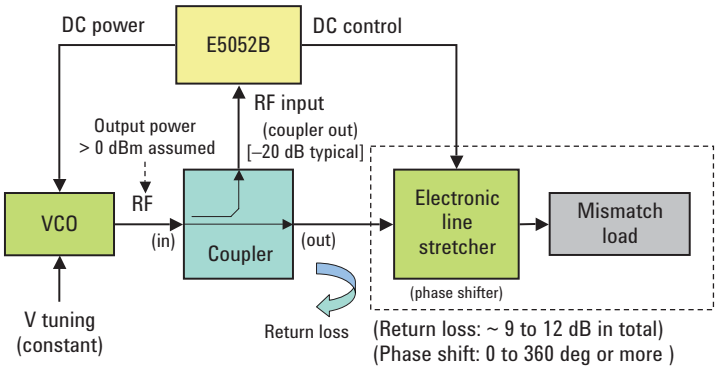


Figure 16. Load pulling characteristic measurement (1)

The phase shifter has to be able to change the phase of reflection signal from 0 to 360 degrees at least, and the total return loss is usually set at 9 to 12 dB. To avoid changing the phase manually, it has become popular to use an electric line stretcher for simplified automated test. Figure 17 shows an example of electric line stretcher (phase shifter) characteristics at 1 GHz.

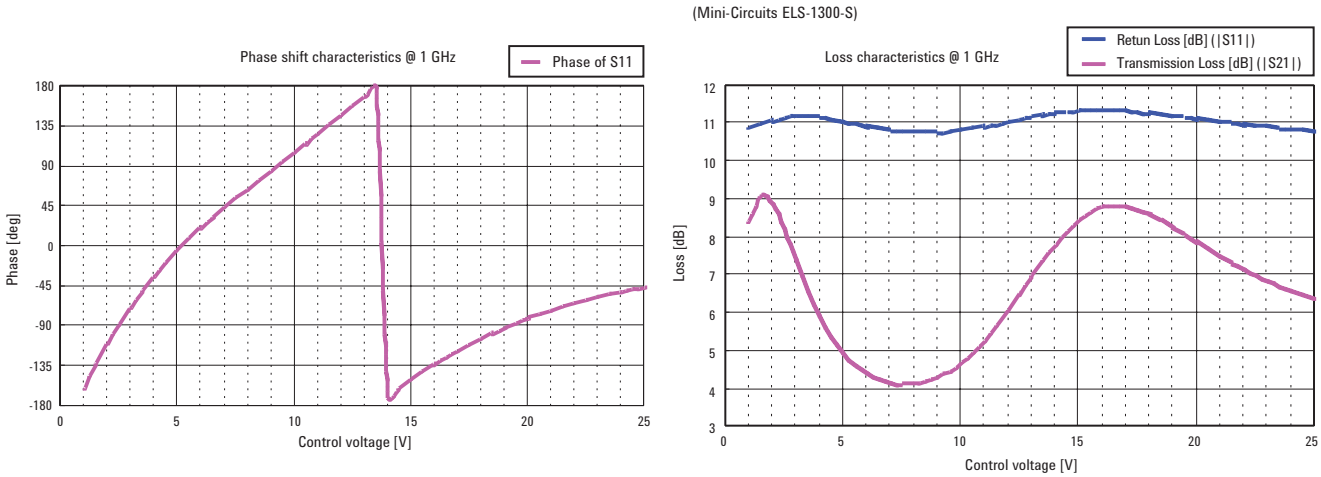


Figure 17. Example of electronic line stretcher characteristics

Figure 18 shows changes in frequency, power level and DC supply consumption current due to the phase shift of the output load at 1 GHz. About a 13.7 MHz peak-to-peak frequency change occurred in this example which used the line stretcher shown in Figure 17.

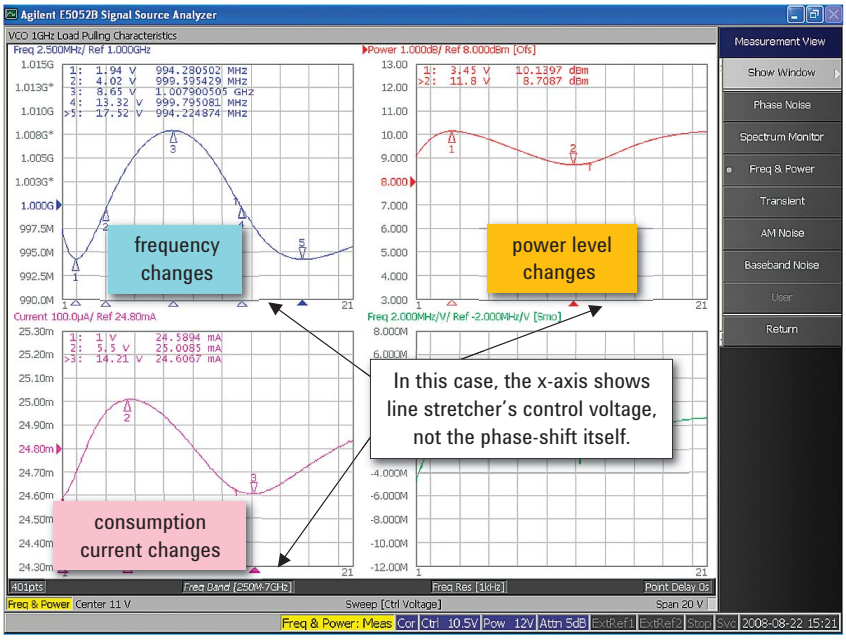


Figure 18. Load pulling characteristics

Another simple method for testing load pulling without a coupler is shown in Figure 19. The results are similar except for the power level changes (shown in Figure 20). The power level characteristic should be corrected by using the line stretcher's transfer response (|S21|) to compensate.

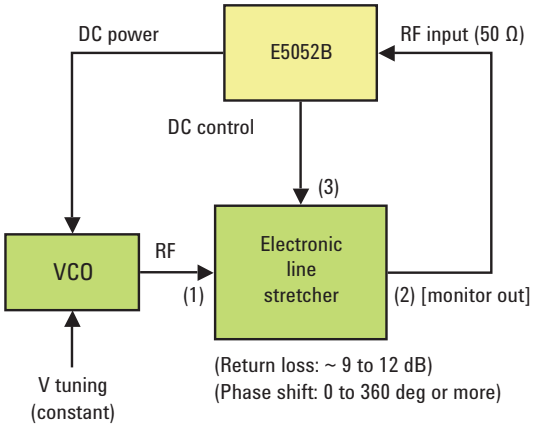


Figure 19. Load pulling characteristics measurement (2)

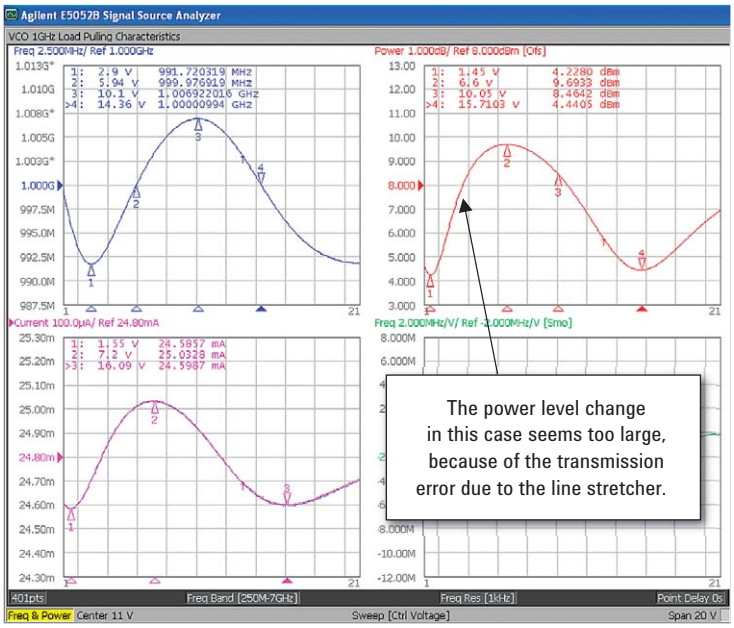


Figure 20. Measured results using the method shown in Figure 19.

An easy way to calibrate the line-stretcher's transfer response is as follows: (shown in Figure 21)

1. Connect a known level signal at the desired measurement frequency directly to the analyzer's input. This is a reference level (A_1 [dBm]).
2. Connect the same known constant level signal to the line stretcher's input. The result includes line stretcher's response (A_2 [dBm]).
3. Memorize $Ac = (A_1-A_2)$ [dB]. This is the amount of transfer response compensation needed.
4. Once the actual measured result of the power level (Ax [dBm]) is obtained, then use the transfer response compensation to determine the correction needed. (Ax+Ac)[dBm] is the compensated result. This simple compensation works well practically, although it does not provide the most accurate correction method.

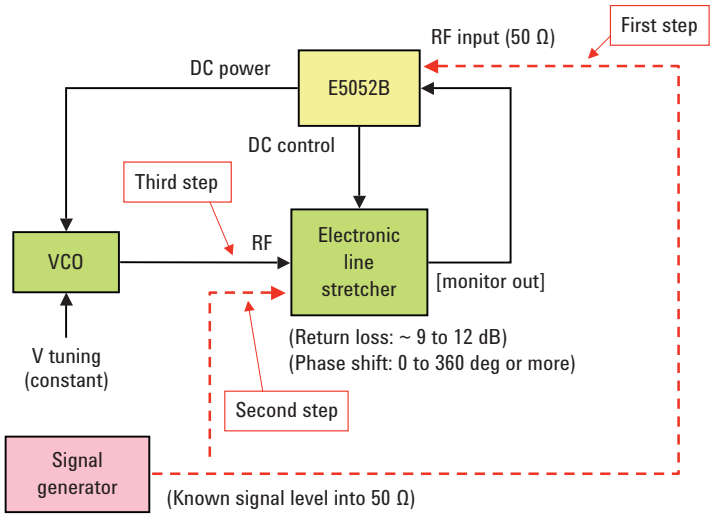


Figure 21. Simple transmission-loss calibration

Figure 22 shows the signal source analyzer's automatic compensation for the same measured data that was used in Figure 20. In this case, E5052B's user equation provides "PS=data+(8-mem)", where "PS" is the user-defined function (to be displayed), "data" is the measured data (Ax), "8" is the reference power level [dBm] (A1) from the signal generator, and "mem" is the line stretcher's response (A2).

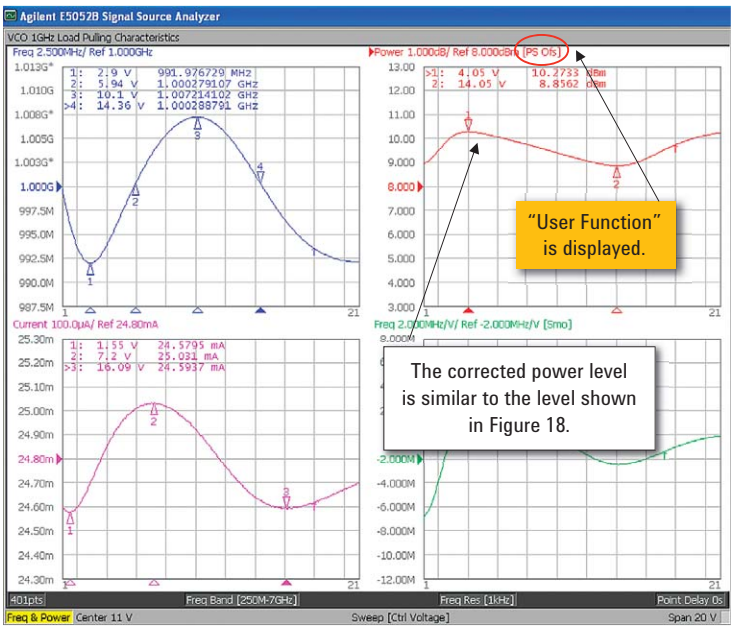


Figure 22. Corrected results using the same data as Figure 20

2-7. Harmonics and spurs

Harmonics and non-harmonic spurs in the VCO output signal are usually measured by a spectrum analyzer. The Spectrum Monitor mode of the E5052B can also work as a spectrum analyzer with maximum 15 MHz frequency span range around a carrier signal (such as shown in Figure 4).

It is simple to measure harmonics by selecting the Carrier To mode under the Spectrum Monitor menu. In the Carrier To mode, **Carrier [x1/x2/x3/x# (#:harmonic number)] to Center** and **Frequency Band** can be set up to find the harmonics easily.

Although the maximum span of the Spectrum Monitor is limited to 15 MHz due to the single conversion structure of the heterodyne receiver; the E5052B can identify –80 dBc spurs (typically) except at certain known frequency points.

2-8. Tuning delay and frequency settling time

A VCO cannot change its output frequency instantly even when the tuning voltage is changed abruptly. The time constant of the VCO frequency response for a step change in tuning voltage can be measured using the Transient mode in the sub-micro second range with about 10 ns resolution minimum. This is sufficient for evaluating ordinary VCO's having 100 ns or more response time.

Figure 23 shows a typical configuration for a time response measurement. The External Trigger mode is used to minimize timing errors. An example of the transient response of a VCO at 850 MHz is shown in Figure 24. Frequency response, power (amplitude) response, and phase response can be observed simultaneously. In this case, the rise time of the control pulse is less than 50 ns without overshoot, and a 25.6 MHz ("narrow") frequency band is used. The tuning delay time constant is less than 1 µs and the frequency settling time is about 5 µs in this case.

The settling time measurement of the output signal frequency or phase is described in the section "Total PLL Performance Test" on page 21. Power-on settling time of output amplitude is usually observed with an oscilloscope. The E5052B also can measure the power level transient response in the time range from sub-micro seconds to 100 seconds.

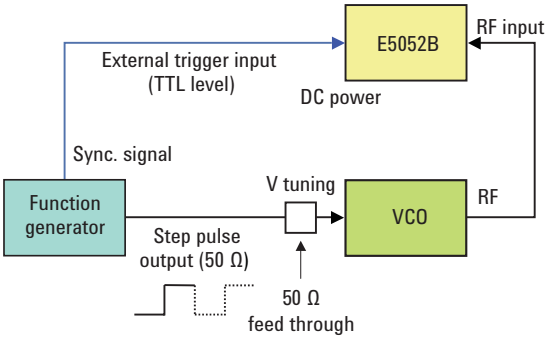


Figure 23. Tuning delay measurement configuration

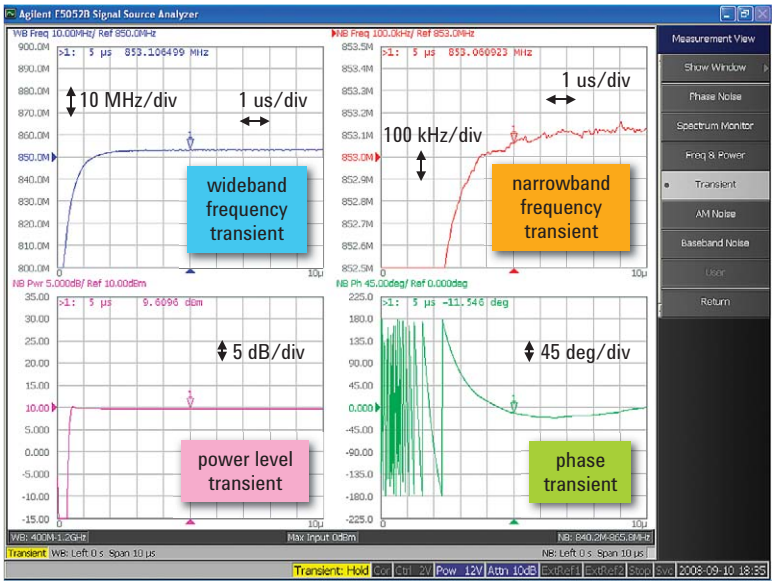


Figure 24. Example of a tuning delay measurement of an 850 MHz VCO

3. Frequency Divider Evaluation

Theoretically, the primary function of a frequency divider (÷N, where N is an integer) is very simple. The output frequency is equal to 1/N of the input frequency, and the phase noise of the output signal is also equal to 1/N of that of the input signal.

However, it may not be so simple, to measure the residual phase noise generated by a frequency divider. The residual noise can be understood conceptually as the excess noise generated and added to the inside of a device (a frequency divider or a prescaler). See Figure 25.

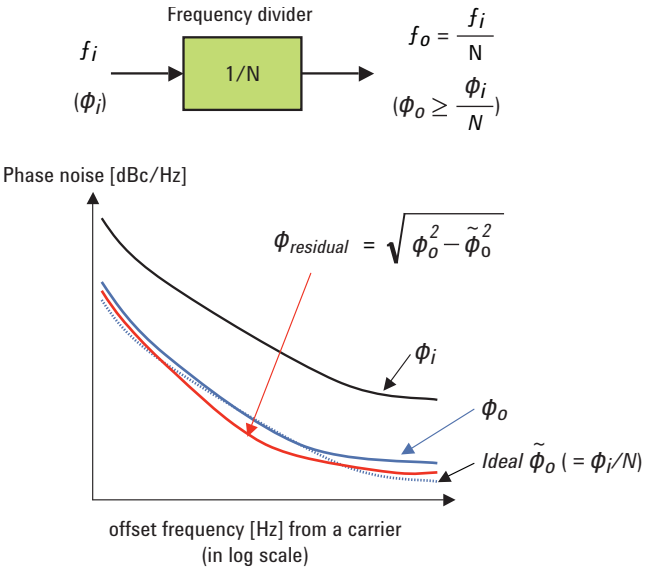


Figure 25. Residual phase noise in a frequency divider

The following factors make a frequency divider's residual phase noise measurement somewhat difficult.

(1) The noise floor of a frequency divider is generally as low as –150 dBc/Hz or –160 dBc/Hz.
(2) The phase noise of the input signal tends to mask the residual phase noise of a frequency divider at low offset frequencies particularly below 100 kHz.
(3) The instrument's internal noise floor has a practical limit even when an ideal input signal source is available.

However, in practice, you often need to know divider's phase noise only at higher offset frequencies (above 100's kHz) because the VCO's phase noise is dominant at lower offset frequencies in most cases of PLL design. Under these practical conditions, the simple residual phase noise evaluation method using a one-port analyzer, such as the E5052B, can be used.

Figure 26 shows an example of a frequency divider's residual noise measured by the E5052B. In this case (divided by 4), the ideal output phase noise above the 10 MHz offset should be 12 dB lower than the original phase noise level of a 6 GHz signal. But, the measured output phase noise floor (of a 1.5 GHz signal) at higher offset frequencies is not only much higher than –12 dB of the ideal noise level, but also a bit higher than the original one. This means that divider's residual phase noise (about –154 dBc/Hz) is added to the output and is significant above a 1 MHz offset.

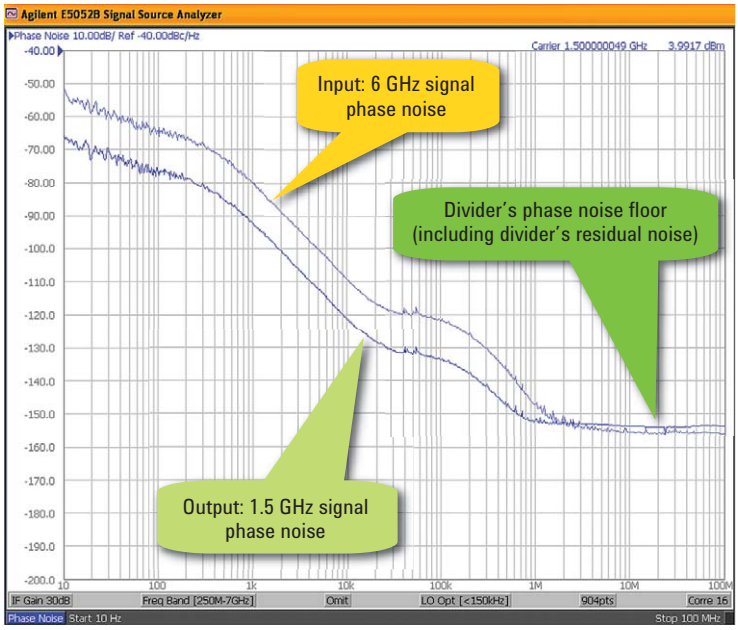


Figure 26. Phase noise example in a frequency divider (dividing by 4)

A "residual phase noise" calculation made with the measured data of Figure 26 is shown in Figure 27. Although this simple one-port analysis is only valid at higher offset frequencies, the result is accurate above 500 kHz offset the measurement area this measurement is focusing on. This is very useful information for determining total PLL noise performance. This one-port method of evaluating residual phase noise is very simple and easy to apply.

Note: The divider's noise floor ($\Phi_{residual}$) increases the reference signal's phase noise (Φ_i) equivalently.

If you want to evaluate the frequency divider's residual phase noise at wider offset frequencies with lower sensitivity and less uncertainty, a 2-port residual noise measurement method is recommended. The 2-port method is outside of the scope of this application note, please refer to Agilent E5505A phase noise measurement system and related documents for more information.[1]

1. Refer to the "Literature References" section at the end of this document, numbers 5 and 6.

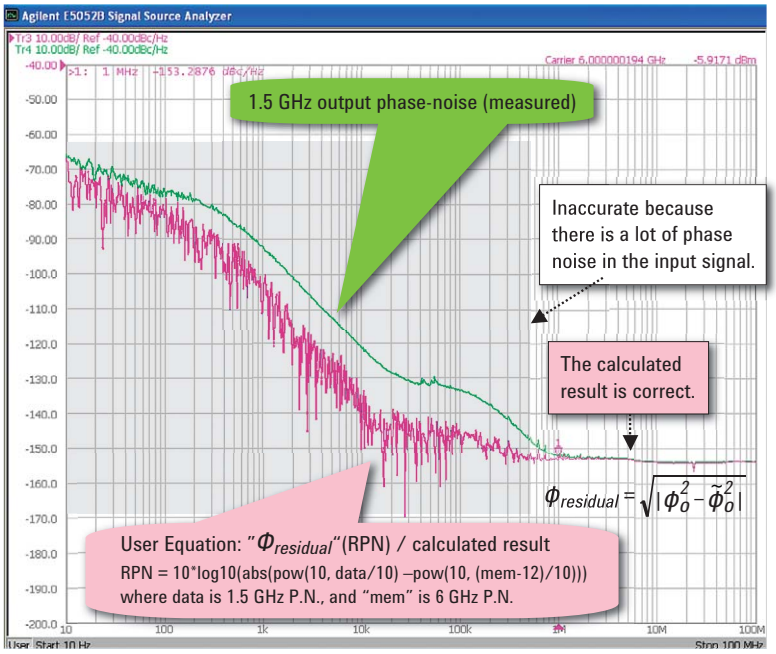


Figure 27. Calculation of residual phase noise

4. Total PLL Performance Test

4-1. General topics on PLL design

A PLL frequency synthesizer is expected to generate pure (i.e. stable and clean) signals. After characterizing designed components and/or testing purchased components in a PLL system, such as the one shown in Figure 1, you will want to estimate the total performance of the PLL system.

In the first stage of the design, you might want to consider creating an appropriate PLL model, probably a typical second-order model or a somewhat advanced third-order model. This assumes that each component works ideally as a linear small signal model with simple linear parameters. Among those components, the most flexible part of the system is a loop filter. The loop filter's transfer function G(s) should provide an optimal trade-off among lower phase noise, lower/fewer spurs, and faster frequency switching response.

An ordinary PLL system has a structure that allows for some reference frequency signal leakage (the reference leak) from the phase comparator into the VCO tuning input port. This causes the PLL output signal to be frequency-modulated, and thus it generates some spurious signals. In designing a loop filter, it is important to minimize the phase noise spectrum near the carrier frequency while, suppressing unwanted spurs at the same time.

You must also remember to shorten frequency switching time when the frequency division ratio (L) is changed. The majority of the frequency switching time is PLL lock-up time unless PLL's nonlinear behavior lasts too long. The PLL lock-up time or the phase settling time of the system is substantially affected by the loop filter's characteristics. In general, setting a higher cut-off frequency for a loop filter (i.e. a smaller time constant) results in worse spurious noise levels, even though it enables the PLL to respond faster and the phase lock-up time becomes shorter.

Please note that the dynamic characteristics (global behavior or response) of an actual PLL frequency synthesizer cannot be readily estimated with a simple linear model or brief simulations. Even though detailed analysis including some nonlinear parameters, saturated operating models, and non-ideal components (say, leaky components) is available recently in several advanced circuit simulators, the total performance evaluation of a PLL system must be executed under actual loop operating conditions.

The E5052B is a very useful tool for this purpose, because it can convert "performance estimation" to "performance verification".

4-2. Fundamental parameters of PLL frequency synthesizer performance

The following parameters are often used to specify a PLL frequency synthesizer as a clean signal source with high stability and fast response.

1) Output signal frequency [Hz] and uncertainty [±ppm]
2) Output signal power level [dBm] and uncertainty [±dB]
3) Phase noise spectrum [dBc/Hz] at specified offset frequencies from the signal (carrier)
4) Residual FM [Hz rms] at a specified band of offset frequency
5) Amplitude noise spectrum [dBc/Hz] or residual AM [%] at a specified band of offset frequency
6) Spurious noise or signals [dBc]
   – including "reference leak", "hum modulation" (due to AC ripples), and "parasitic oscillation"
7) Harmonics [dBc]
8) Frequency switching time or settling time [sec] as a specified uncertainty [±ppm]
   – other terms with a similar meaning may be: "(phase) lock-up time" or "phase settling time"
   – alternatively "loop bandwidth [Hz]" is used, particularly in an early design stage

   (Note that "settling time" and "loop bandwidth" are interchangeable only if a specified PLL model is assumed and shared.)
9) Warm-up time [second or minute]
   – mainly a reference oscillator's frequency settling time to the specified uncertainty [±ppm].
10) Power consumption [W or DC voltage x DC current]
11) Temperature characteristics of each parameter

In an early design stage,
12) Load pulling characteristics
13) Oscillator pushing characteristics

are also evaluated often for a PLL system.

However, these factors may become negligible because a buffering output amplifier and a stable DC power supply are usually provided for high-performance PLL systems.

You would need many different kinds of test instruments to evaluate all the above parameters. This includes instruments such as a very high-speed frequency counter, an RF power meter, a modulation domain analyzer, a phase-noise test system, a spectrum analyzer, an accurate DC power supply, and a controller/PC (for controlling the PLL under test as well as all the test instruments). This is not only time-consuming but also results in less repeatable measurements resulting from multiple reconnects to the many different kinds of instruments listed above. In particular, the frequency transient (settling time) measurement as it is difficult to synchronize the measurement trigger with PLL's frequency change in a sub-micro second range.

The E5052B signal source analyzer (10 MHz to 7 GHz) combines an RF power meter, two frequency counters, a (wideband) direct counter and a (narrowband) heterodyne counter; a phase noise analyzer, a baseband noise analyzer, an AM noise analyzer, a modulation domain (transient) analyzer, a narrow-span spectrum monitor, and two low-noise DC sources in one box[2].

This instrument can reduce the measurement setup and measurement time significantly, making PLL performance evaluation faster and more reliable. It also enables measurements to be made of most parameters with minimal reconnection compared to the traditional way.

4-3. Frequency/power/phase transient measurements with the E5052B

Signal acquisition time and resolution in frequency measurements are mutually exclusive in general. The conventional PLL frequency transient measurement method (with a modulation domain analyzer, for example) is based on the operating principle of a frequency counter. In this method, the data sampling interval (which must be longer than the signal acquisition/gate time) and the measurement frequency bandwidth (which is determined directly by the gate time) affect the frequency resolution. The potential problem that results from this limitation is that when you select a shorter sampling interval in order to capture faster frequency transient phenomenon the frequency resolution will be insufficient.

The E5052B combines a wideband type of counter with a narrowband type of counter, which enables it to capture fast frequency transient responses in the sub-micro second range with about 10 ns of time resolution or sub-Hz of frequency resolution. Therefore, even though the minimum time resolution and the minimum frequency resolution are not available at the same time, the E5052B offers 10 to 100 times better time and frequency resolution in transient measurements, compared to traditional instruments.

Figure 28 shows a typical configuration for PLL transient evaluation. An external trigger signal (TTL level) is strongly recommended, but if a trigger signal is not available, the video trigger function inside the E5052B can be utilized with the proper setting.

It is somewhat difficult to set an appropriate trigger mode and trigger zone at first when measuring parameter boundaries, unless you have some a priori information on the frequency transient. This is because the trigger point is a function of the time resolution (or span), frequency resolution (or span), and power level. You should set the wideband mode first, if possible, and then set the narrowband mode after viewing the whole transient response.

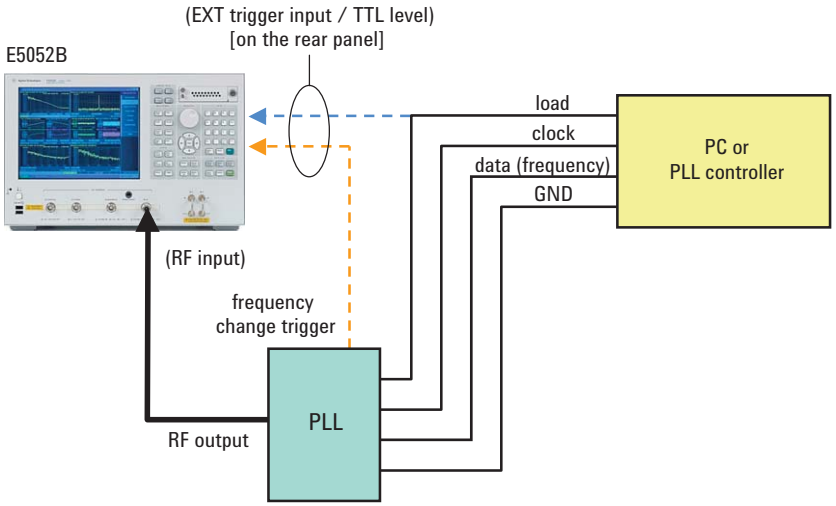


Figure 28. PLL transient measurement configuration

Figure 29 shows an example of how to set trigger modes and parameter zones. Note that the trigger point in the narrowband mode is not always synchronized with the trigger point of the wideband mode. Also, the external trigger point has about 0.2 µs uncertainty in repeatability due to the hardware (logic circuit) limitation.

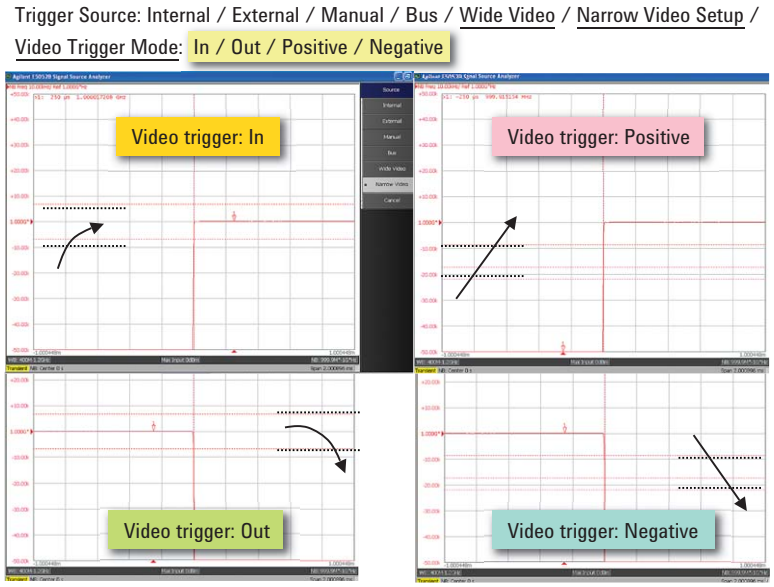


Figure 29. Trigger sources and video trigger modes

Figure 30 shows measured results of the frequency switching from 5.7 GHz to 5.8 GHz. In this case, the frequency switching looks very fast and smooth in 10 MHz order (measured by the wideband mode). However, there is a non-monotonic transient between 1 ms and 5 ms in 100 kHz order (or 10 ppm order). The power level transient and the phase transient are also observed simultaneously. As you can see, the phase settling time is about 6 ms, which you wouldn't know if you only looked at the screen in wideband mode.

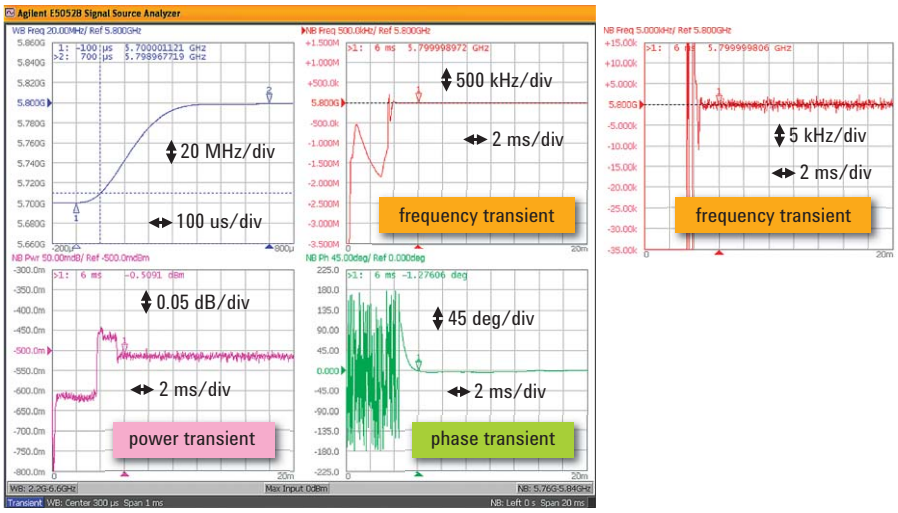


Figure 30. PLL transient measurement (1)

Figure 31 shows another example of PLL transient characteristics. The frequency switching time of this PLL synthesizer is relatively fast, though a frequency glitch appears at about 100 us. The output frequency reaches 1 ppm uncertainty at less than 200 us. Pass/Fail criterion of the phase settling time (within ±6 degrees at 5.8 GHz) has been set 300 us, and, in this case (shown in Figure 32), the transient response of the phase fell outside of the red limit lines and failed the criterion.

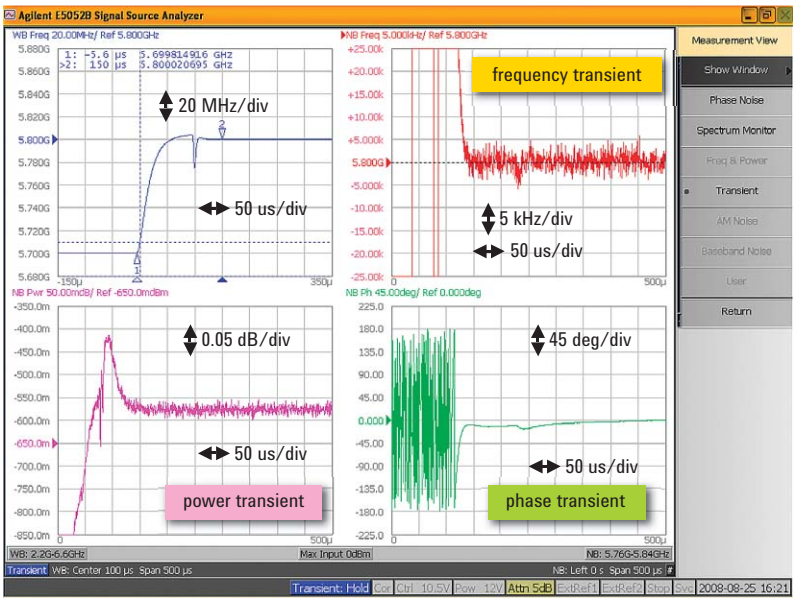


Figure 31. PLL transient measurement (2)

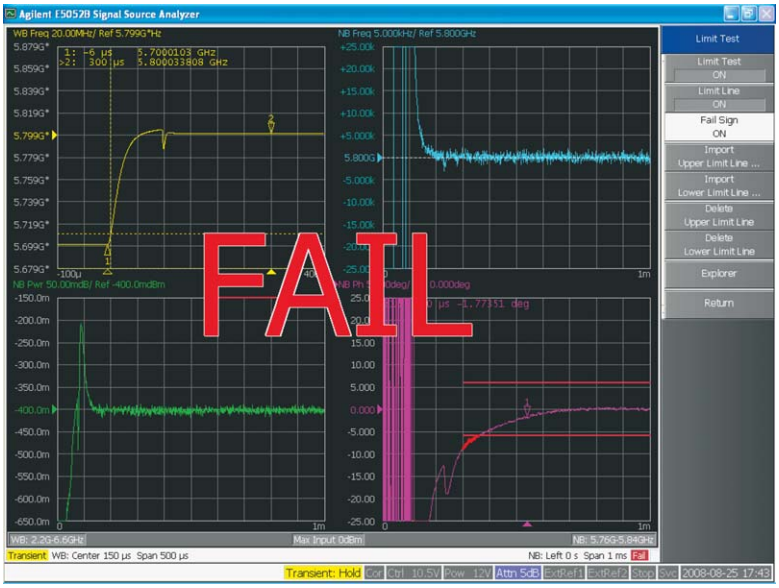


Figure 32. Pass/Fail test of phase settling time

E5052B's fast transient measurement capability can be useful for evaluating the step response of a wideband FM modulator of a PLL frequency synthesizer. Figure 33 is a typical example of a FM modulator response test configuration; a measured example is shown in Figure 34. Some overshoot response is observed in this case even though the input square-wave is almost ideal (with no overshoot at the leading edge and the trailing edge).

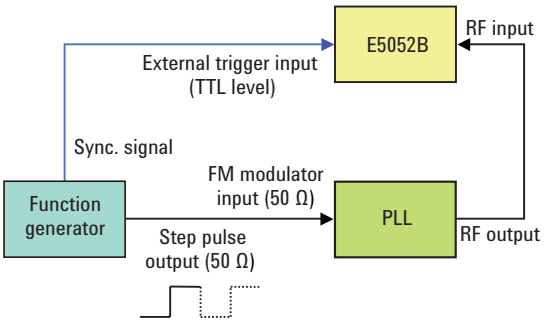


Figure 33. FM modulator response measurement configuration

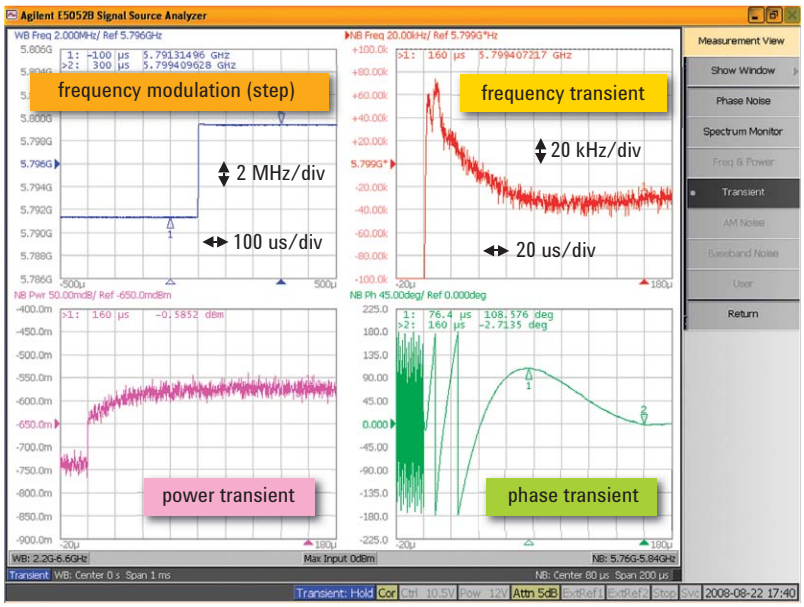


Figure 34. FM modulator response measurement

4-4. "Cut & Try" optimization for loop filter design

Currently, almost all the work done to improve the response and spurious level of the PLL loop filter design is done with a circuit simulator. Once you know the phase noise characteristics of the free-running VCO, frequency divider, and stable reference oscillator, then the total phase noise characteristic of a PLL system can be easily estimated with a model[1],[3] and [4].

In addition to this kind of simulation or estimation, the E5052B provides an innovative way to optimize the "cut-and-try" process in loop-filter design; this is based on measured data. Using a full set of the E5052B's capability (many of the measurement functions previously discussed in this application note) with intuitive screen operation, designers can easily measure the desired parameters back and forth, as shown in Figure 35. As a result, the E5052B enables designers to make their cut & try process the fastest possible for total signal source design and verification.

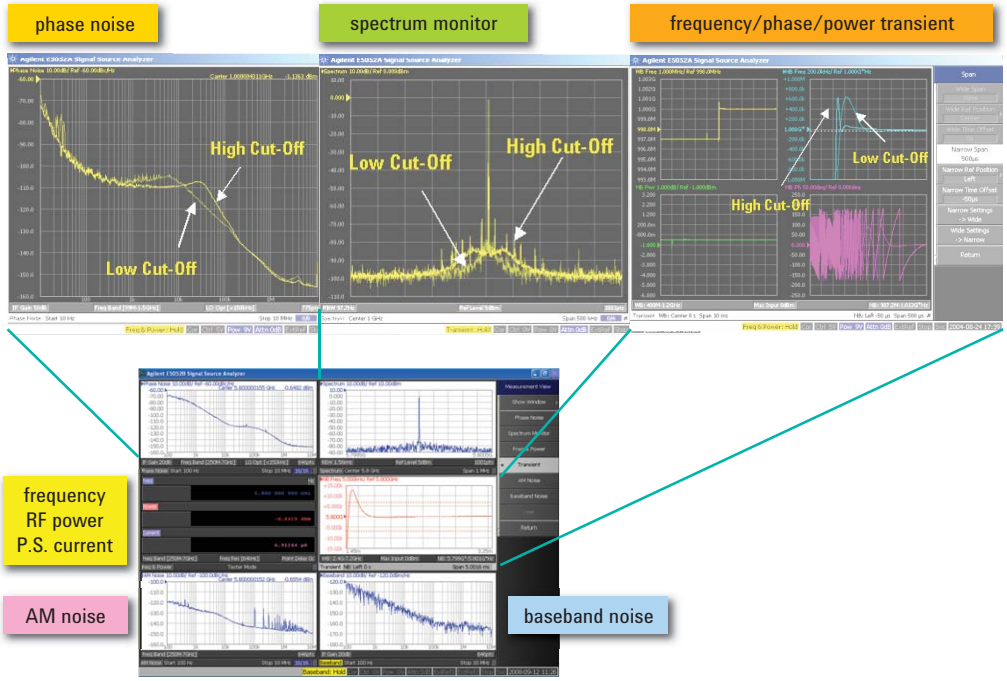


Figure 35. "Cut & Try" optimization for loop-filter design

Summary

This application note introduces practical solutions for VCO/PLL performance evaluation and actual examples of parameter measurements using the E5052B signal source analyzer.

Although, some of the topics discussed in this document are very basic, these important points are not always implemented in actual measurement situations causing possible device degradation. The advanced topics in this note will give VCO/PLL designers some good insight into making their design process more efficient.

The E5052B provides fast and accurate measurements for VCO/PLL design and manufacturing, and contributes to producing high-quality profitable products with a shorter lead time.

Literature References

1. *Advanced Phase Noise and Transient Measurement Techniques Application Note*, 5989-7273EN
2. *Fast, Easy, and Accurate Microwave Phase Noise Measurements using the Agilent E5052B SSA with the E5053A Application Note*, 5989-8373EN
3. *Fast and Simple Phase Noise Measurements in mmW Technical Overview*, 5989-8372EN
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5. *Agilent E5500 Series Product Overview*, 5989-0851EN
6. *Agilent E5505A Phase Noise Measurement System User's Guide*, pp 201-225, E5505-90003

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[1] *Advanced Phase-lock Techniques*, James A. Crawford, Artech House, 2008.
[2] *E5052B Brochure*, 5989-6389EN, Agilent Technologies, 2007 and *E5052B Product Data Sheet*, 5989-6388EN, Agilent Technologies, 2008.
[3] *Phase-Locked Loop Engineering Handbook for Integrated Circuits*, Stanley Goldman, Artech House, 2007.
[4] *Phase-Locked Loops – Principles and Practice*, Paul V. Brennan, McGraw-Hill, 1996.

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