DESIGNING WITH MICROWAVE CAE — A CASE STUDY

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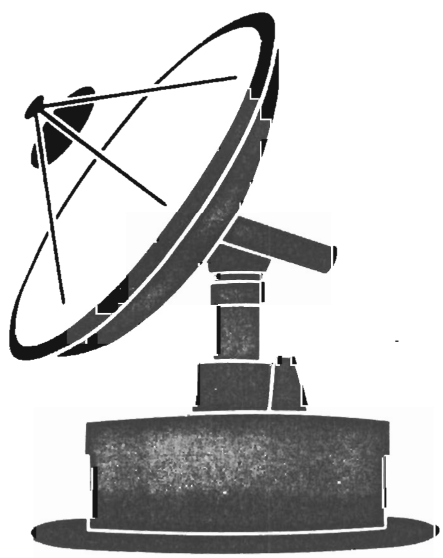
RF & Microwave
Measurement
Symposium
and
Exhibition



HEWLETT
PACKARD

This paper uses the design of a 2-to-8 GHz 3-dB power splitter to contrast the efficiencies and precision afforded by computer-aided-engineering (CAE) against the problems and shortcomings encountered when traditional manual-only design techniques are employed. Special attention is devoted to coping with subtleties not necessarily recognized by circuit theory but nonetheless existing in the real circuit. The paper demonstrates how the Touchstone (TM) design program accurately predicts the effects of these subtleties. The overall design process using CAE is analyzed, concluding with the excellent correlation between CAE-simulated and actually-measured performance.

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A COMPARISON OF MANUAL AND COMPUTER ASSISTED DESIGN TECHNIQUES FOR A 3 dB POWER SPLITTER

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2 – 8 GHz 3dB POWER SPLITTER

- Manual Design Pitfalls
- CAE Advantages
- Correlation of Simulated and Actual Data

5203

This paper highlights the design of a 2-8 GHz 3dB power splitter. It shows some pitfalls not predicted by the theory, how Touchstone accurately predicts their effects, and the excellent correlation between simulated and actual performance.

II. MANUAL DESIGN

- Theoretical Synopsis
- Problem Statement and Design
- First Pass Layout
- Potential Error Sites

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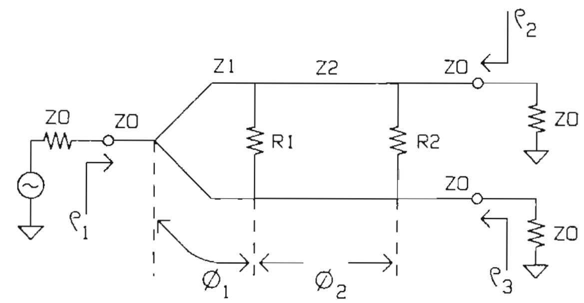
GENERAL CIRCUIT



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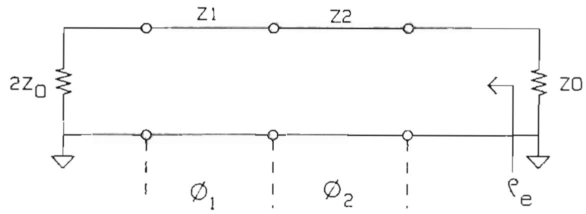
The circuit shown is the generalized representation of a two section two way 3 dB power splitter. Z_1 and Z_2 are the characteristic impedances of the transmission line with corresponding electrical lengths ϕ_1 and ϕ_2. R_1 and R_2 are the isolation resistors for each section.

The design equations are developed by analyzing the circuit under even and odd mode operation.

EVEN MODE BISECTED CIRCUIT



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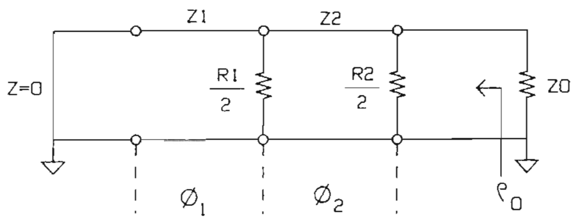
The even mode bisected circuit is generated by driving the two output ports with waves of equal amplitude and phase. The isolation resistors therefore have no net voltage across them and the resulting circuit can be bisected symmetrically with the source Zo being replaced by 2Zo.

An examination of the even mode circuit indicates that the transmission lines Z_1 and Z_2 act as a transformer between an impedance ratio of 2:1. The design of these lines therefore reduces to that of a quarter wave stepped impedance transformer.

ODD MODE BISECTED CIRCUIT



5207

The odd mode bisected circuit is generated by driving the two output ports with waves of equal amplitude and 180 degrees phase difference. The isolation resistors therefore have a non-zero net voltage across them. The midpoint of the resistors and the line junction at port 1 are a virtual ground.

Design equations for R_1 and R_2 can be developed based on this equivalent circuit.

DESIGN EQUATIONS

$$\alpha = 90° \left[1 - \frac{1}{\sqrt{2}}\left(\frac{f_2/f_1 - 1}{f_2/f_1 + 1}\right)\right]$$

$$R_2 = \frac{2Z_1 Z_2}{\left[(Z_1 + Z_2)\ (Z_2 - Z_1 \mathrm{COT}^2\alpha)\right]^{1/2}}$$

$$R_1 = \frac{2R_2(Z_1 + Z_2)}{R_2(Z_1 + Z_2) - 2Z_2}$$

5208

The equations presented here are derived (for the two stage case) by formulating an expression for

$$\rho_O = \frac{1 - Y_{IN,O}}{1 + Y_{IN,O}}$$

and then equating the real and imaginary parts of the numerator to zero.

f_1 = Start Frequency

f_2 = Stop Frequency

See Reference 1 for more details.

PROBLEM STATEMENT

Frequency	2 - 8 GHz
Bandwidth	120%
S11	−15dB Max
S21	−3.5dB Min
S22	−20dB Max
S32	−12dB Max

5209

The performance requirements for this component are as indicated. Size and cost are also important so a two stage (N=2) design has been selected.

DESIGN STEPS

* • Table Look-Up for Z_1 and Z_2
  • Transmission Line Synthesis
* • Transmission Line Length

  Calculation: $L = \dfrac{\lambda_1 \lambda_2}{2(\lambda_1 + \lambda_2)}$

  • Isolation Resistance Calculation

* See Ref 2

5210

The manual design of a power splitter using the aforementioned technique reduces to looking up the transmission line impedances and then synthesizing the line width and effective dielectric constant. The line lengths and isolation resistances can then be calculated from the previous equations.

For each transmission line:

λ_1 = Start Frequency Wavelength

λ_2 = Stop Frequency Wavelength

DESIGN DATA

Section 1	Section 2
$Z_1 = 77.19\Omega$	$Z_2 = 64.77\Omega$
$W_1 = 85\mu m$	$W_2 = 139\mu m$
$e_{R(eff)_1} = 5.84$	$e_{R(eff)_2} = 6.01$
$L_1 = 6200\mu m$	$L_2 = 6103\mu m$
$R_1 = 67.3\Omega$	$R_2 = 520.8\Omega$

5211

Applying the problem statement to the design algorithm yields the following data.

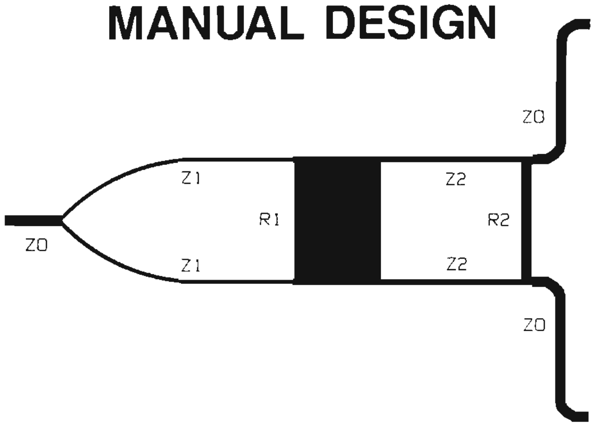
For each transmission line:

W_x = Line Width

L_x = Line Length

$e_{R(eff)x}$ = Effective Dielectric Constant

MANUAL DESIGN



5212

Based on the data generated in the manual design, this layout seems to meet all the criteria for good (close to theoretical) performance.

POTENTIAL ERROR SITES

- Microstrip Discontinuities
- Thin Film Resistor Form Factor
- Arm to Arm Coupling

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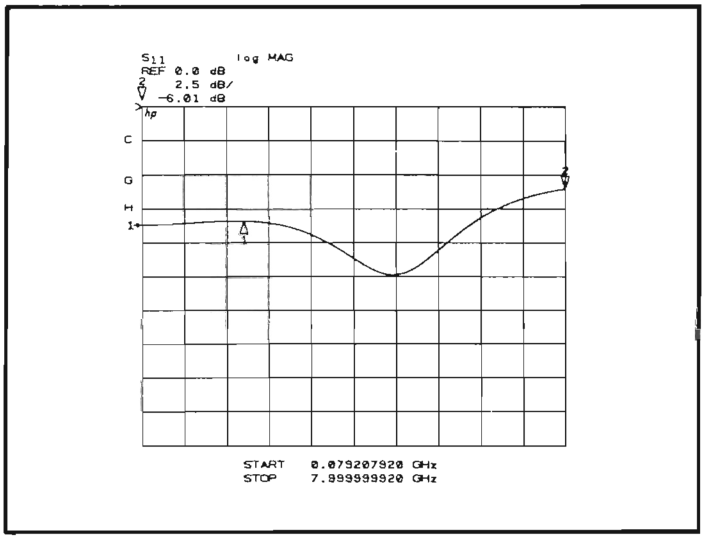
Some potential error sites in this layout that are not taken into account in the theoretical derivation are, the microstrip discontinuities, the electrical length of the isolation resistors and the coupling between the two arms.



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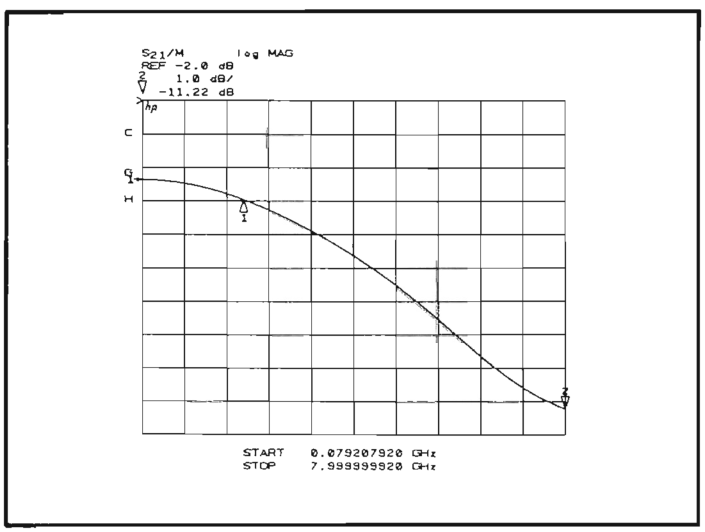
The performance of the manually designed splitter is very poor.

There must be some aspect of the physical layout, not accounted for theoretically, that is degrading the performance.

Marker 1 = 2 GHz

Marker 2 = 8 GHz



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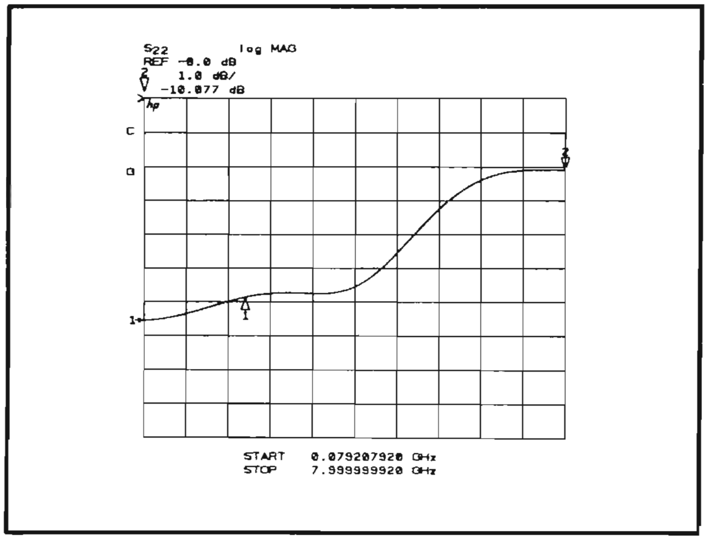
The steep roll off of the transmission response is indicative of a severely mis-tuned circuit.



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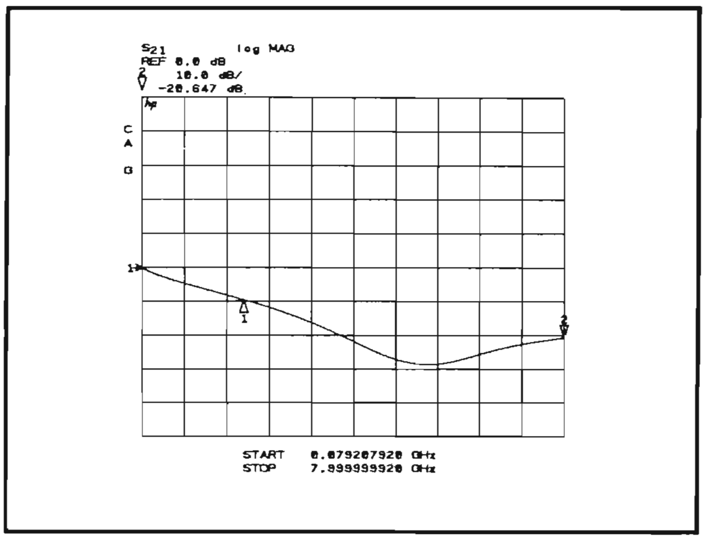
Note how the frequency response of the port matches have no particular shape. Based on the theoretical derivation, we would expect an equal ripple type response.



5217

This is a plot of the isolation response (S32). Since the network analyzer is only a two port the graph shows S21.

CONCLUSIONS

- **The Existing Theory is Incomplete.**
- **A Better Understanding of the Interaction Between the Physical Layout and the Design Parameters is Necessary.**
- **A CAE Workstation Allows an Actual Model of the Layout to be Analyzed. This Should Result in an Improved Design.**

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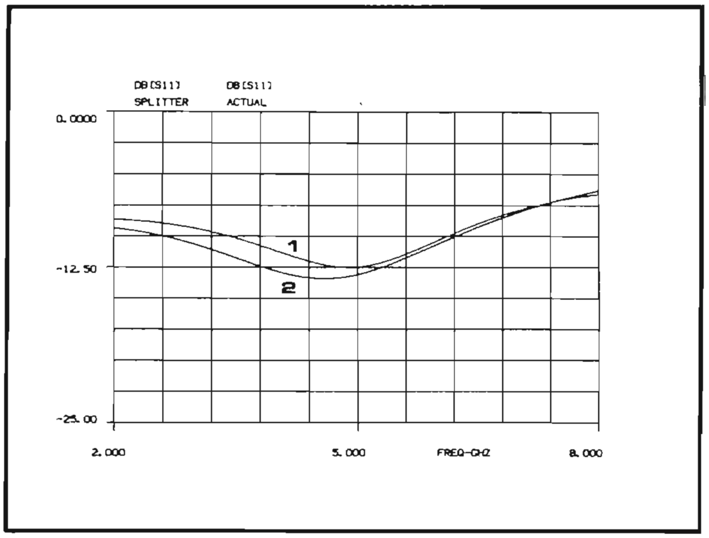
III. CAE APPROACH

- **Correlate Simulated and First Pass Design**
- **Use of the Tune Mode to Isolate Sensitive Areas**
- **Revise Layout and Present Simulated Results**
- **Optimize Second Pass Design**
- **Correlate Simulated and Second Pass Design**

5219

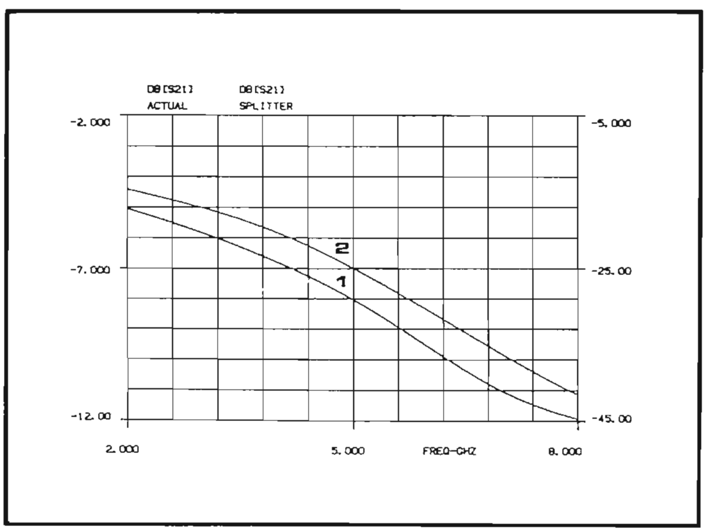


5221

The correlation between the empirical and simulated data is very good.

Trace 1 = Actual Performance

Trace 2 = Simulated Performance



5222

The difference between the insertion loss plots is approximately 1 dB. This represents the loss of the prototype package that was not taken into account in the simulation.

```
!   This file describes a 2 - 8 Ghz splitter for use as an example of the
!   advantages of Computer Aided Design.  This example is of the first pass
!   design and models the isolation conductances as thin film resistors and
!   includes all the microstrip discontinuities.
!
DIM
    lng    um

CKT
    msub    er=9.4    h=254    t=3.0    rho=1.31    rgh=0
    mlin     1         2    w=254     l=2538
   mtee2     3    4    2    w1=85     w2=85     w3=254
    mlin     3         5    w=85      l=6201
    mlin     4        16    w=85      l=6201
   mstep     5         6    w1=85     w2=139
   mstep    16        17    w1=85     w2=139
    mlin     6         7    w=139     l=25
    mlin    17        18    w=139     l=25
   mtee2     7    8    9    w1=139    w2=139    w3=2229
   mtee2    18   19   20    w1=139    w2=139    w3=2229
     tfr     9        20    w=2229    l=3000    rs=50    f=0
    mlin     8        10    w=139     l=3547
    mlin    19        21    w=139     l=3547
   mtee2    10   11   12    w1=139    w2=139    w3=277
   mtee2    21   22   23    w1=139    w2=139    w3=277
     tfr    12        23    w=277     l=2885    rs=50    f=0
    mlin    11        13    w=139     l=25
    mlin    22        24    w=139     l=25
   mstep    13        14    w1=139    w2=254
   mstep    24        25    w1=139    w2=254
    mlin    14        15    w=254     l=2538
    mlin    25        26    w=254     l=2538
DEF3P        1   15   26    spliter3

FREQ
    sweep    2    8    .06

OUT
    spliter3  db[s11]   gr1
    spliter3  db[s21]   gr2
    spliter3  db[s32]   gr2a
    spliter3  db[s22]   gr3

GRID
    range      2      8     0.6
    gr1      -25      0     2.5
    gr2      -12     -2     1.0
    gr2a     -45     -5     4.0
    gr3      -20    -10     1.0
```

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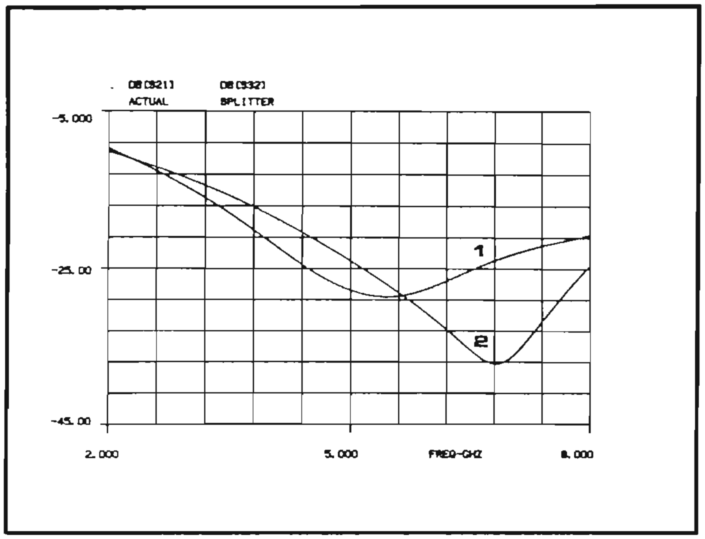


5223

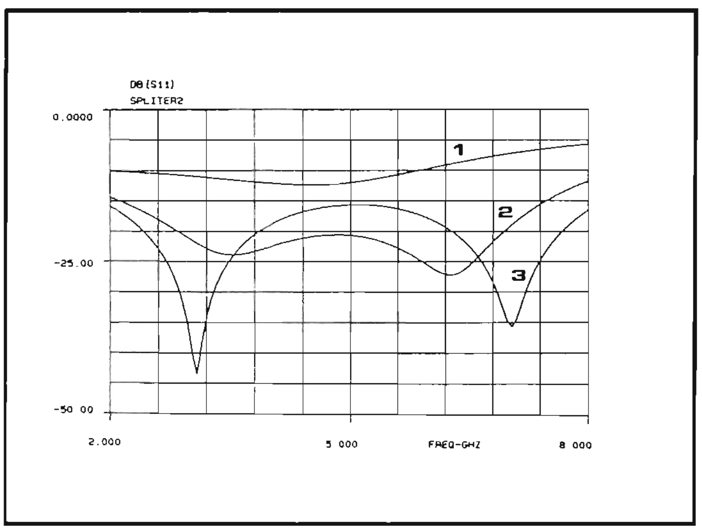
The difference between the simulated (trace 2) and actual data (trace 1) is due to the fact that the arm to arm coupling was not modeled.

TUNE MODE

- **Allows Varying One or More Parameters.**
- **Plots Successive Responses on the Screen and/or Plotter.**
- **This is an Efficient Way to Evaluate Circuit Sensitivities.**

5224

The tune mode was used to examine the circuits sensitivities to changes in several aspects of the layout. The form factor of the isolation resistors and the gap between the microstrip impedance steps and isolation resistors were studied.



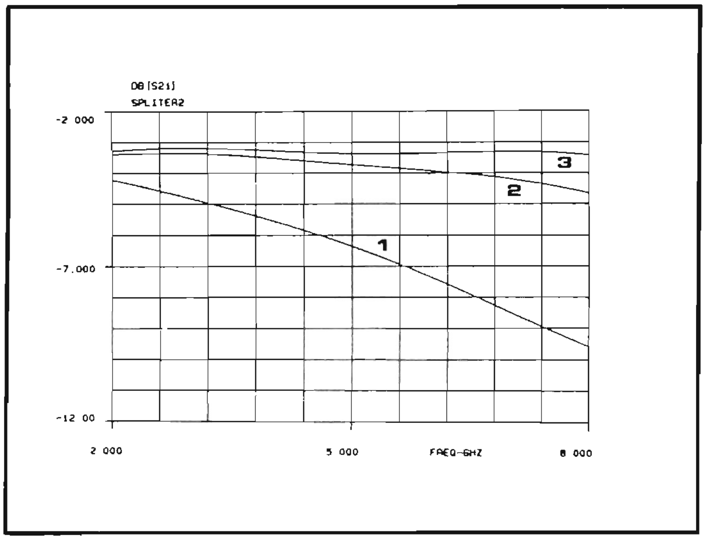
5225

These three traces represent the change in the circuits response as the isolation resistances are made physically smaller and the gap between the resistor and the microstrip step is reduced to zero.

Trace 1 = Original Design

Trace 2 = Smaller Resistors
Zero Gap

Trace 3 = Optimal Design



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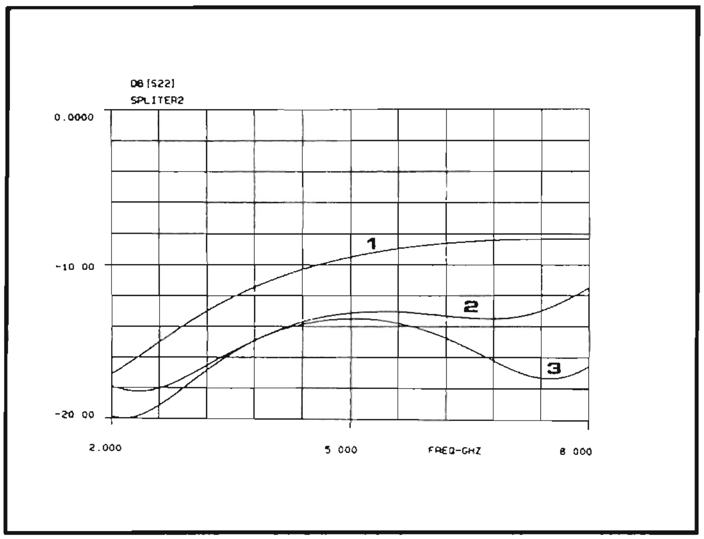

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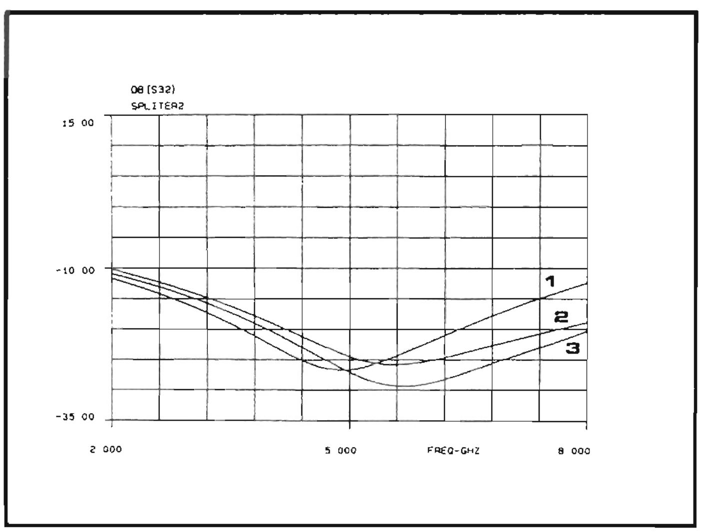


5228

As the characteristics of the layout approach the optimal design, note how the transmission characteristics flatten out and the port matches take on an equal-ripple response.

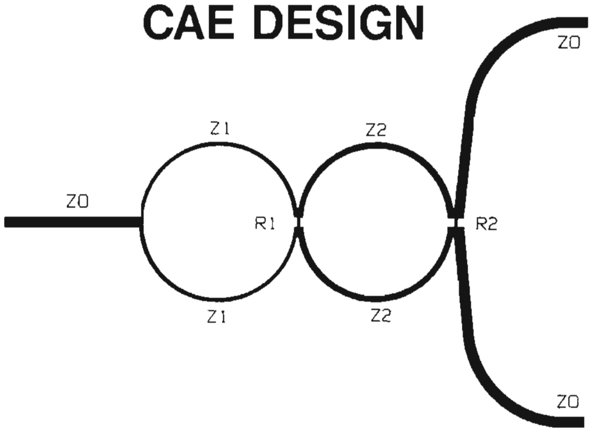
DESIGN CONCLUSIONS BASED ON TOUCHSTONE MODEL

- **Isolation Resistor Electrical Length Should be Less than λ/10.**
- **The Distance Between the Microstrip Step and the Isolation Resistor Should be as Small as Possible, Preferably Zero.**

5229

Based on data generated using Touchstone's tune mode, it was deduced that the thin film resistors electrical length should be less than λ/10 so that they appear as lumped resistors and not lossy transmission lines. The distance between the impedance steps and the thin film resistors also affects the circuit's performance. They need to be as close as possible.

CAE DESIGN



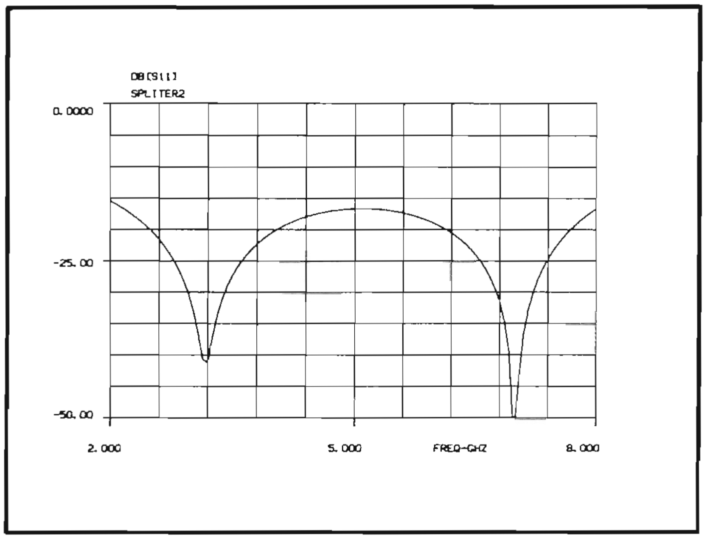
5230

A revised layout is proposed using the information generated with Touchstone's tune mode. It incorporates electrically shorter resistors and no gap between the impedance step and isolation resistor.

```
!   This file describes a 2 - 8 Ghz splitter for use as an example of the
!   advantages of Computer Aided Design.  This example is of the second pass
!   design and incorporates all the layout improvements discovered using
!   Touchstone's tuner mode.
!
DIM
    lng    um
VAR
    width1  #     25     85     200
    width2  #     25    139     300
    length1 #   1000   6201   10000
    length2 #   1000   5913   10000
    reslen1 #     50    256     500
    reslen2 #     50    520     750
    reswit1 #     50    190     500
    reswit2 #     10     50     500
CKT
    msub    er=9.4    h=254    t=3.0    rho=1.31    rgh=0
    mlin     1          2   w=254           l=2538
   mtee2     3    4     2   w1^width1       w2^width1    w3=254
    mlin     3          5   w^width1        l^length1
    mlin     4         12   w^width1        l^length1
   mtee2     5    6     7   w1^width1       w2^width2    w3^reswit1
   mtee2    12   13    14   w1^width1       w2^width2    w3^reswit1
     tfr     7         14   w^reswit1       l^reslen1    rs=50   f=0
    mlin     6          8   w^width2        l^length2
    mlin    13         15   w^width2        l^length2
   mtee2     8   10     9   w1^width2       w2=254       w3^reswit2
   mtee2    15   16    17   w1^width2       w2=254       w3^reswit2
     tfr     9         17   w^reswit2       l^reslen2    rs=50   f=0
    mlin    10         11   w=254           l=2538
    mlin    16         18   w=254           l=2538
DEF3P        1   11    18   spliter2
FREQ
    sweep    2    8    .06
OUT
    spliter2  db[s11]   gr1
    spliter2  db[s21]   gr2
    spliter2  db[s32]   gr2a
    spliter2  db[s22]   gr3
GRID
    range      2      8    .6
    gr1      -50      0     5
    gr2      -12     -2     1
    gr2a     -35     15     5
    gr3      -20      0     2
OPT
    spliter2   db[s11] < -20
    spliter2   db[s21] < -3.3
    spliter2   db[s22] < -20
    spliter2   db[s32] < -15
```

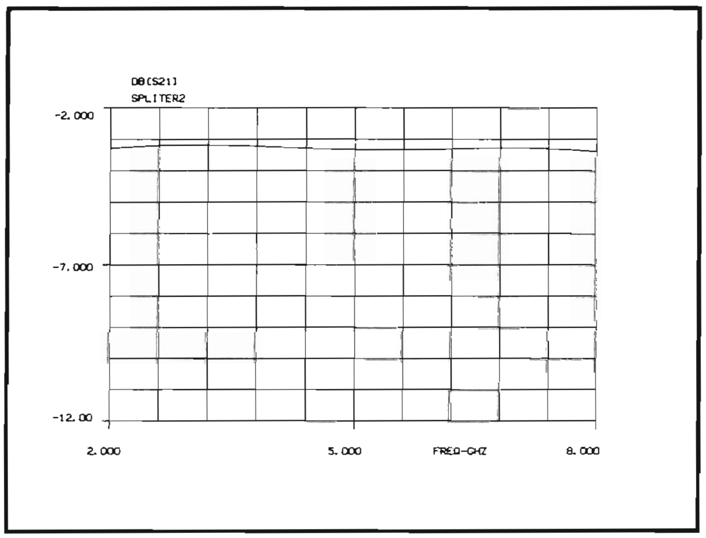
5231

This is the simulated data of the revised design. Note the equal ripple response of the port matches, and the flat insertion loss response.



5232

The symmetry of all these responses about the center frequency confirms the validity of our second pass layout.



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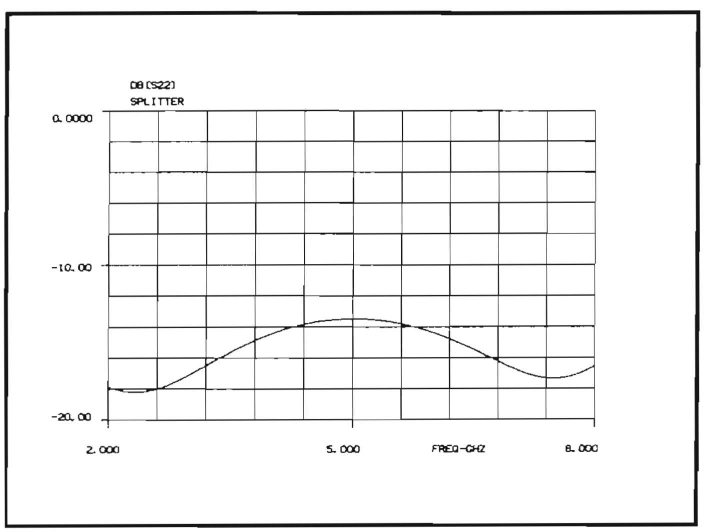

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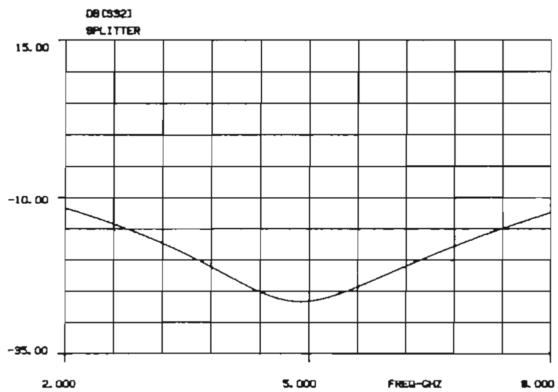

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The optimizer was used to fine tune the layout for improved output port match.

TOUCHSTONE'S OPTIMIZER

- Random or Gradient Optimization Available.
- Automatic Update of Circuit File with Improved Values.
- Continuous Monitoring of Progress Via Graphics Display.

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SPLITTER OPTIMIZATION

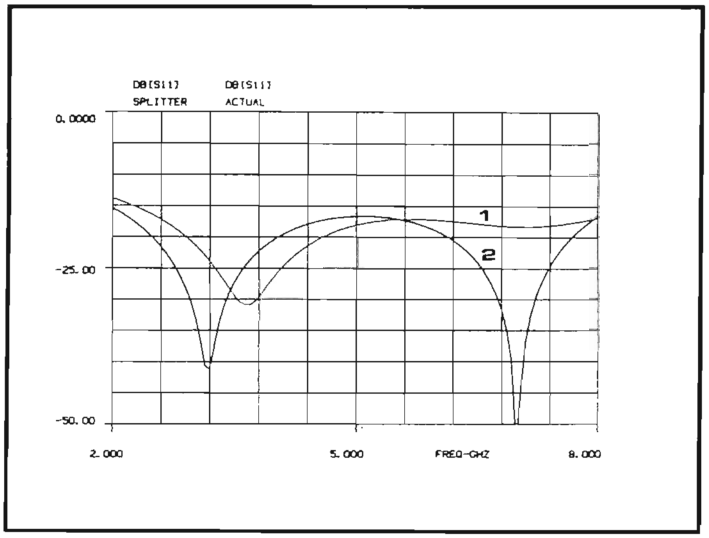
- Random Optimization was Used First to Get Close to the Required Performance.
- Gradient Optimization Was Then Employed to Determine the Best Values.
- Total Optimization Time Was Approximately 20 Minutes.
- Optimization Ranges for the Circuit Elements Were Set Based on the Manufacturing Limits of Thin Film Circuits.

5237

These plots correlate the actual performance of the optimized design with the simulated data.

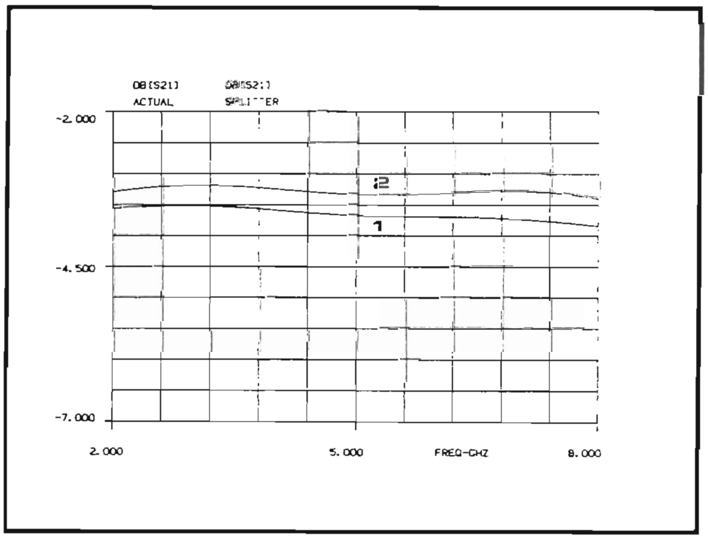
Trace 1 = Actual Performance

Trace 2 = Simulated Performance



5238

The difference between the insertion loss plots is approximately 1 dB. This represents the loss of the prototype package that was not taken into account in the simulation.



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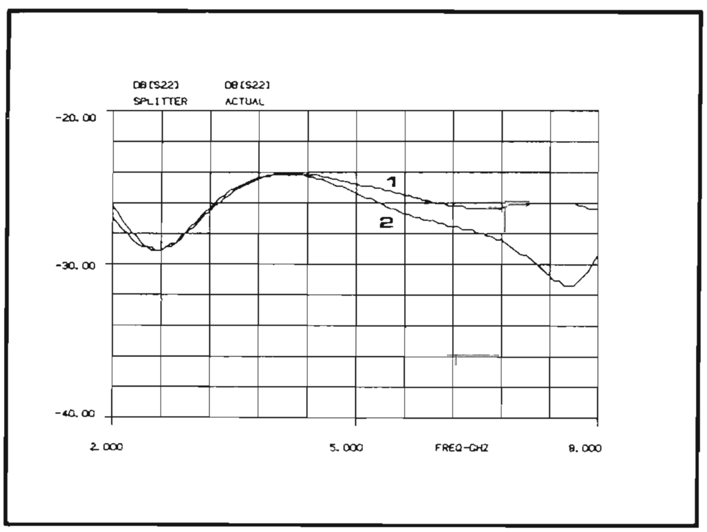

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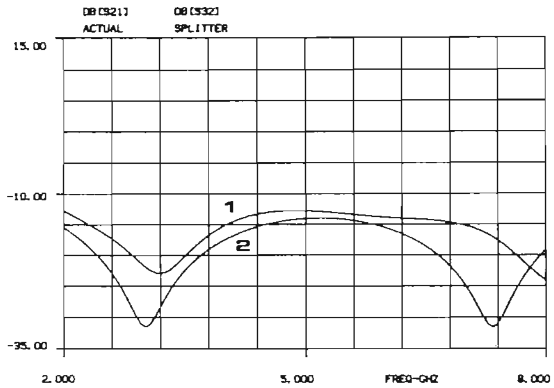

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IV. SUMMARY

- Your Data is Only Good IF Your Model is Complete and Accurate.
- Package Parasitics, Especially Fringing Capacitances and the Coax to Micro-strip Transitions, Will Degrade Performance.
- Computer Aided Engineering Offers Improved Accuracy and Reduced Design Time.

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ACKNOWLEDGMENTS

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Daren McClearnon

Joe Barnhart

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