

A Guideline for Designing External DC Bias Circuits

- For the HP 4192A, HP 4194A, HP 4274A, HP 4275A, HP 4276A, HP 4277A -

1. External DC Bias Circuit

If you need to apply up to approximately 10A DC bias to a device (ex. inductors) and measure impedance - DC bias characteristics, this can be done by inserting an external DC bias circuit between the LCR meter and the sample device. This A/N describes how to design the circuit.

2. Specific parameters for the circuit

Before designing the circuit, you should decide on the following parameters before determining the circuit's elements.

- 1) DC current bias which will be applied: I [A]
- 2) Minimum measurement frequency : f [Hz]
- 3) Inductance of the sample device : Lx [H]
- 4) Oscillator output level : Vac [V]

The external DC bias circuit diagram is shown in Figure 1.

3. Chokes (L₁, L₂)

L₁ and L₂ in Figure 1 should satisfy the following conditions;

- $|2\pi fL_1| \geq |2\pi fL_2| \geq |2\pi fL_x|$
- $|2\pi fL_2| \geq R_r$
(R_r: Range Resistance [Ω] See Table 1.)
- When the maximum DC current is applied, the cores of L₁ and L₂ must not be saturated.

- $P_{max} \geq I^2 \cdot R_{dc}$

P_{max}: Max. allowable power of L₁ and L₂

I: Max. DC current

R_{dc}: DC series resistance of L₁ and L₂

You should select chokes for L₁ and L₂ which have a large P_{max} and small R_{dc}. R_{dc} will influence the selection of the Zener diodes (see section 5).

4. Blocking Capacitors (C₁, C₂, C₃, C₄)

- The capacitance of C₁, C₃ and C₄ in Figure 1 should be

$$C \geq \frac{1}{10\pi f}$$

In case of the HP 4276A,

$$C \geq \frac{1}{2\pi f}$$

- The capacitance of C₂ should be as follows. Because of the high impedance of the Hp terminal, a small capacitance may be used.

$$C_2 \geq \frac{1}{10^3 \pi f}$$

- Withstanding voltage, Vdc, of C₁ and C₂ depends on DC resistance of L₁, the output voltage of DC power supply, and the DC bias current. It should be determined as follows.

$$V_{dc} > V - I \cdot R_{dc1}$$

Vdc: Withstanding voltage of C₁, C₂
 V: Output voltage of DC power supply
 I: DC bias current
 Rdc₁: DC resistance of L₁

However the following equation is recommended for a safety margin.

$$V_{dc} > V$$

- Withstanding voltage of C₃ and C₄ should be determined as follows.

$$V_{dc} > I \cdot R_{dc2}$$

Vdc: Withstanding voltage of C₃, C₄
 I: DC bias current
 Rdc₂: DC resistance of L₂

5. Diodes (CR₁₁, CR₁₂, CR₁₃, CR₁₄)

If the circuit is opened when a bias current is applied, a large counter electromotive force will be generated by the choking inductor and could damage the LCR meter and the operator. The circuit shown in Figure 1 includes a protection circuit to block this counter electromotive force. The diodes used in this protection circuit, CR₁₁, CR₁₂, CR₁₃, and CR₁₄, should be determined as follows.

- Diodes must be able to withstand the following power for τ [sec].

$$P_d = 1/2 \cdot (L_1 + L_2) \cdot I^2 \cdot 1/\tau \quad [W]$$

$$\tau = \frac{(L_1 + L_2)}{Z_{zt} + (R_{dc1} + R_{dc2})}$$

L₁, L₂: Inductance of L₁, L₂
 I: DC bias current
 Zzt: Zener impedance
 Rdc₁, Rdc₂: DC resistance of L₁, L₂

- Zener voltage of CR₁₁ and CR₁₂ should be determined as follows.

$$V_z > V - I \times R_{dc1} + \sqrt{2} \text{ Vac}$$

V: Output voltage of DC power supply
 I: DC bias current
 Rdc₁: DC resistance of L₁
 Vac: Oscillator level

Zener voltage of CR₁₃, CR₁₄ should be determined as follows.

$$V_z > I \cdot R_{dc2}$$

I: DC bias current
 Rdc₂: DC resistance of L₂

Considering operator safety, the zener voltage should be determined as:

$$V_z \leq 40 [V]$$

(Safe voltage is less than 42 [V]p-p according to IEC-348/UL-1244.)

6. Diodes (CR₁, CR₂, CR₄, CR₅)

Are diodes to protect the LCR meter from high DC voltages.

- Zener voltage of CR₁, CR₂, CR₄ and CR₅ should be determined as follows.

HP 4192A:	V _Z ≐	2 [V]
HP 4194A:	V _Z ≐	2 [V]
HP 4274A:	V _Z ≐	10 [V]
HP 4275A:	V _Z ≐	2 [V]
HP 4276A:	V _Z ≐	2 [V]
HP 4277A:	V _Z ≐	2 [V]

V_Z: Zener Voltage

These values depend on the maximum input voltage of the LCR meters and the maximum oscillator levels. The rating zener voltage should be greater than the maximum oscillator output level, less than the maximum input voltages and should not distort the test signal. Therefore, the zener voltage should be approximately twice the maximum oscillator output level.

7. Diode (CR₃, CR₆)

CR₃ and CR₆ are to cancel the parasitic capacitance of zener diodes CR₄ and CR₅.

- Withstanding voltage and maximum forward current of CR₃ and CR₆ are the same as or greater than CR₄ and CR₅.

8. Diodes (CR₇, CR₈, CR₉, CR₁₀)

- CR₇, CR₈, CR₉ and CR₁₀ are the same as CR₃ and CR₆. One additional diode in series with CR₇, CR₈, CR₉ and CR₁₀ will decrease the total parasitic capacitance.

9. Stray Impedance and Circuit Parasitics

When a measurement is performed using this circuit, an additional error will be caused by the circuit. When you design the circuit, keep the signal lines as short as possible to minimize stray impedance. (Refer to Figure 1.) Before making a measurement, you should determine the stray impedance as follows.

- 1) Measure a test device (inductor) using a direct-coupled test fixture such as the HP 16047A/C/D.
- 2) Connect the external DC bias circuit to a LCR meter, and measure the test device without DC bias.
- 3) Compare the results of both 1) and 2). (Refer to Figure 2.)
- 4) If the difference between 1) and 2) is small, the LCR meter's zero adjustment function will be able to compensate the circuit's stray impedance. Perform a zero adjustments at measurement terminals of the circuit.
- 5) If the stray impedance is too great to compensate for with the zero adjustment function, it will necessary to use the three point compensation method (0ohm/0S/Standard calibration). For the HP 4194A, perform 0ohm/0S/Standard calibration at measurement terminals of the circuit. For other LCR meters, perform a three point compensation using an external computer. (Refer to Instrument News/July, 1984.)

10. Procedure

- 1) Perform a stray impedance compensation of the circuit using LCR meter's built-in compensation function or using an external computer (refer to section 9).
- 2) Connect a test device (inductor) to measurement terminals of the circuit.
- 3) Set the voltage level of the DC power supply to 0V, then turn it on. Slowly increase the voltage to appropriate level. Do not turn the DC power supply on or off while its output level is not 0V.
- 4) Measure the DC current bias characteristics of the test device (inductor).
- 5) Slowly decrease the voltage level to 0V.
- 6) Remove the test device.

Do not connect or remove the test device while a DC current bias is applied.

11. Sample Circuit Design

This describes a sample circuit design using the following specifications.

- A. Instrument: HP 4194A Impedance/Gain-Phase Analyzer
- B. DC current bias: $I = 0 - 3$ [A]
- C. Inductance of a test device: $L_x = 25$ [μ H]
- D. Measurement frequency: 200 - 300 [kHz]
Minimum frequency: $f = 200$ [kHz]
- E. Oscillator level: $V_{ac} = 0.5$ [V]

(1) Chokes (L_1 , L_2)

- $|2\pi f L_1| \geq |2\pi f L_2| \geq |2\pi f L_x|$

$$L_1 \geq L_2 \geq 25 \text{ } [\mu\text{H}]$$

- $|2\pi f L_2| \geq R_r$

$$L_2 \geq \frac{50 \text{ } [\Omega]}{2\pi \times 200 \text{ } [\text{kHz}]}$$

$$L_2 \geq 39.8 \text{ } [\mu\text{H}]$$

- $P_{\max} \geq I^2 \cdot R_{dc}$

$$P_{\max} \geq 9 \cdot R_{dc}$$

Therefore select as follows.

$$L_1 = L_2 = 52 \text{ } [\mu\text{H}]$$

$$R_{dc} = 0.2 \text{ } [\Omega]$$

(2) Blocking capacitor

- Capacitance of C_1 , C_3 and C_4

$$C \geq \frac{1}{10\pi f}$$

$$C \geq \frac{1}{10\pi \cdot 200} \text{ [kHz]}$$

$$C \geq 0.16 \text{ [\mu F]}$$

- Capacitance of C_2

$$C \geq \frac{1}{10^3 \pi f}$$

$$C \geq \frac{1}{10^3 \pi \cdot 200} \text{ [kHz]}$$

$$C \geq 1.6 \text{ [nF]}$$

- Withstanding voltage of C_1 and C_2

$$V_{dc} > V$$

$$V_{dc} > 10 \text{ [V]}$$

- Withstanding voltage of C_3 and C_4

$$V_{dc} > I \times R_{dc2}$$

$$V_{dc} > 3 \text{ [A]} \times 0.2 \text{ [\Omega]}$$

$$V_{dc} > 0.6 \text{ [V]}$$

Therefore, select as follows.

$$C_1 = C_3 = C_4 = 3300 \text{ [\mu F]} \quad (V_{dc} = 25 \text{ [V]})$$

$$C_2 = 1 \text{ [\mu F]} \quad (V_{dc} = 25 \text{ [V]})$$

(3) Diodes (CR₁₁, CR₁₂, CR₁₃, CR₁₄)

- Allowable power

$$\tau = \frac{L_1 + L_2}{Z_{zt} + (R_{dc1} + R_{dc2})} = \frac{52 [\mu\text{H}] + 52 [\mu\text{H}]}{Z_{zt} + 0.2 [\Omega] + 0.2 [\Omega]}$$
$$= \frac{104}{Z_{zt} + 0.4} \times 10^{-6} [\text{sec}]$$

$$P_d = 1/2 \cdot (L_1 + L_2) \cdot I^2 \cdot 1/\tau = 1/2 \cdot 104 [\mu\text{H}] \cdot 3^2 [\text{A}] \cdot \frac{Z_{zt} + 0.4}{104 \times 10^{-6}}$$
$$= 4.5 Z_{zt} + 18 [\text{W}]$$

- Zener voltage of CR₁₁, CR₁₂

$$V_z > V - I \times R_{dc1} + \sqrt{2} \text{ Vac}$$

$$V_z > 10 [\text{V}] - 3 [\text{A}] \times 0.2 [\Omega] + \sqrt{2} \times 0.5 [\text{V}]$$

$$V_z > 8.7 [\text{V}]$$

- Zener Voltage of CR₁₃, CR₁₄

$$V_z > I \times R_{dc2}$$

$$V_z > 3 [\text{A}] \times 0.2 [\Omega]$$

$$V_z > 0.6 [\text{V}]$$

Therefore select as follows.

$$\text{CR}_{11}, \text{CR}_{12}: V_z = 20 [\text{V}], Z_{zt} = 22 [\Omega]$$

(Motrola 1N 4747 .. HP P/N 1902-0556)

$$\text{CR}_{13}, \text{CR}_{14}: V_z = 10 [\text{V}], Z_{zt} = 7 [\Omega]$$

(Motrola 1N 4740 .. HP P/N 1902-0554)

(4) Diodes (CR₁, CR₂, CR₄, CR₅)

- Zener Voltage

$$V_z \approx 2 [\text{V}]$$

Therefore select as follows.

$$\text{CR}_1, \text{CR}_2, \text{CR}_4, \text{CR}_5: V_z = 10 [\text{V}]$$

(Motrola 1N 4740 .. HP P/N 1902-0554)

(5) Diodes (CR₃, CR₆)

- Withstanding voltage

Same as CR₄, CR₅

Therefore select as follows.

CR₃, CR₆: Fast recovery: 1A
(Motorola 1N 4936 .. HP P/N 1901-1065)

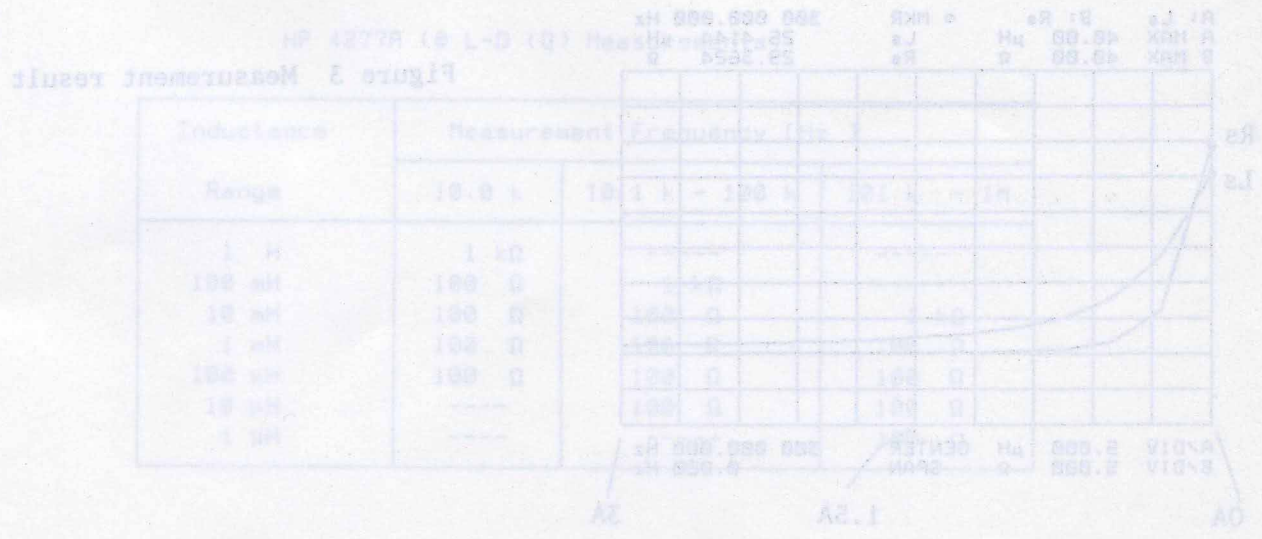
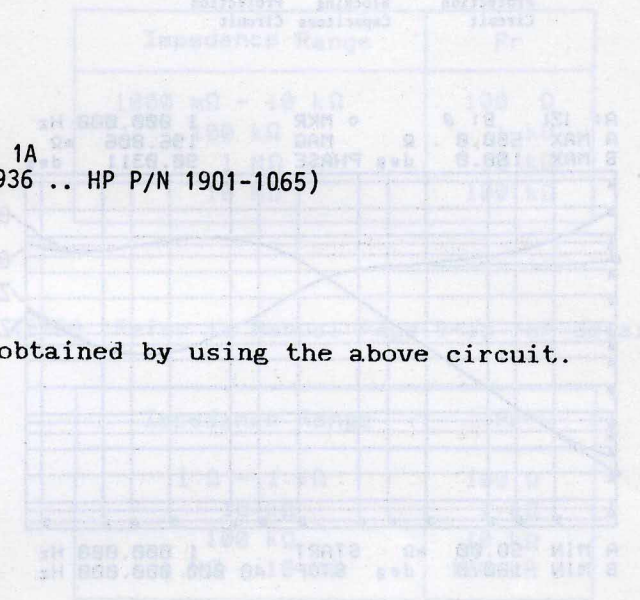
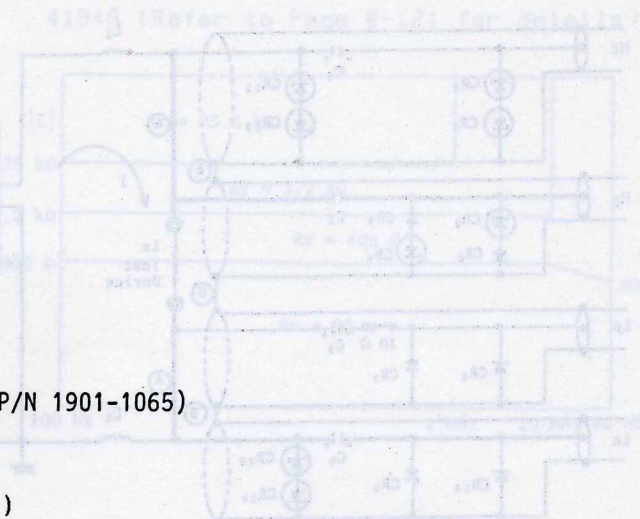
(6) Diodes (CR₇, CR₈, CR₉, CR₁₀)

- Same as CR₃, CR₆

Therefore select as follows.

CR₇, CR₈, CR₉, CR₁₀: Fast recovery: 1A
(Motorola 1N 4936 .. HP P/N 1901-1065)

Figure 3 is the measurement result obtained by using the above circuit.



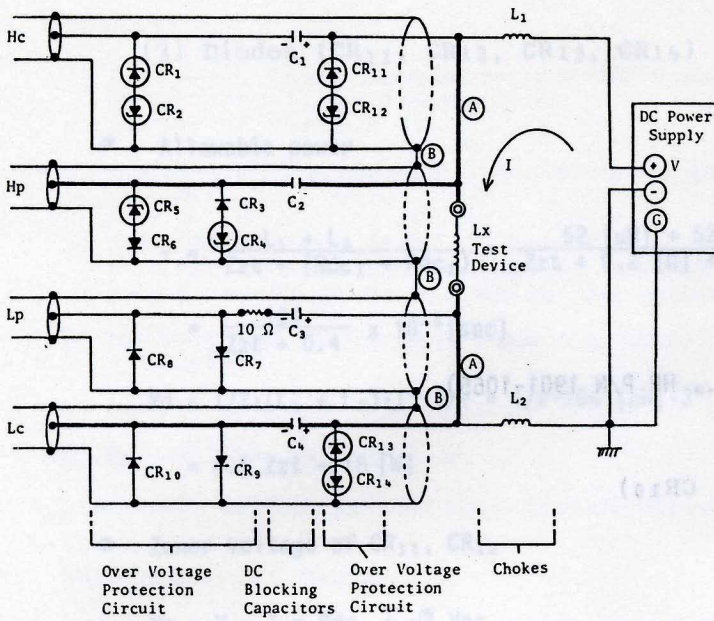
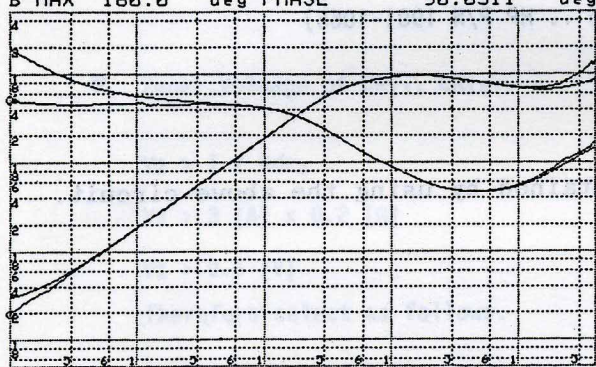


Figure 1 External DC bias circuit

- Ⓐ: Signal lines of Hp and Lc (the thick lines in the figure to the left) should be kept as short as possible.
- Ⓑ: Each signal line, especially the Hp and Lc lines, should be shielded, and the shield conductors should be connected with a heavy wire at a point as near as possible to the test device (point Ⓑ).

A: |Z| B: θ \circ MKR 1 000.000 Hz
 A MAX 500.0 Ω MAG 196.806 m Ω
 B MAX 180.0 deg PHASE 90.0311 deg

Figure 2 Comparison between the HP 16047C and the circuit

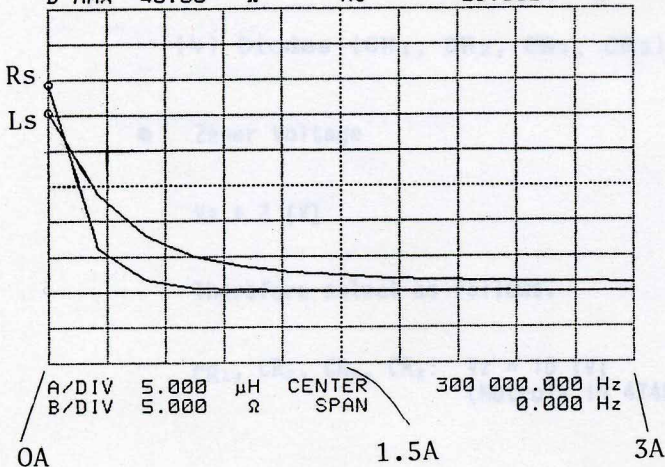


- θ : The Circuit
- θ : HP 16047C
- Z: HP 16047C
- Z: The Circuit

A MIN 50.00 m Ω START 1 000.000 Hz
 B MIN -180.0 deg STOP 40 000 000.000 Hz

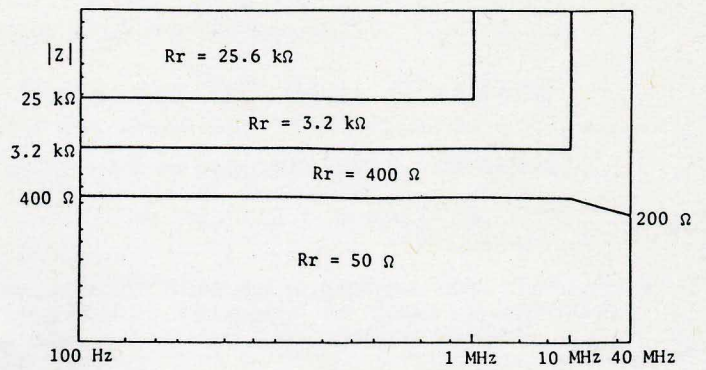
A: Ls B: Rs \circ MKR 300 000.000 Hz
 A MAX 40.00 μ H Ls 25.4144 μ H
 B MAX 40.00 Ω Rs 29.3624 Ω

Figure 3 Measurement result



A/DIV 5.000 μ H CENTER 300 000.000 Hz
 B/DIV 5.000 Ω SPAN 0.000 Hz

Impedance Range	Test Level	
	< 70 mV	> 70 mV
1 Ω - 1 kΩ	1 kΩ	100 Ω
10 kΩ	10 kΩ	1 kΩ
100 kΩ - 1 MΩ	10 kΩ	10 kΩ



4274A (Refer to Manual Page 8-11 for details) 4275A (Refer to Manual Page 8-13 for details)

Impedance Range	OSC Level Multiplier	
	x 1 x 0.1 x 0.01	x 5
100 mΩ - 10 Ω	10 Ω	10 Ω
100 Ω - 1 kΩ	100 Ω	10 Ω
10 kΩ	1 kΩ	100 Ω
100 kΩ	10 kΩ	1 kΩ
1000 kΩ	100 kΩ	10 kΩ
10 MΩ	100 kΩ	100 kΩ

Impedance Range	Rr
1000 mΩ - 10 kΩ	100 Ω
100 kΩ	1 kΩ
1 MΩ	10 kΩ
10 MΩ	100 kΩ

4276A (Refer to Manual Page 8-15 for details)

Impedance Range	Rr
1 Ω - 1 kΩ	100 Ω
10 kΩ	1 kΩ
100 kΩ	10 kΩ
1 MΩ - 10 MΩ	100 kΩ

HP 4277A (@ L-D (Q) Measurements)

Inductance Range	Measurement Frequency [Hz]		
	10.0 k	10.1 k - 100 k	101 k - 1M
1 H	1 kΩ	-----	-----
100 mH	100 Ω	1 kΩ	-----
10 mH	100 Ω	100 Ω	1 kΩ
1 mH	100 Ω	100 Ω	100 Ω
100 μH	100 Ω	100 Ω	100 Ω
10 μH	-----	100 Ω	100 Ω
1 μH	-----	-----	100 Ω



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