

### FEATURES

- 150 MSPS CONVERSION RATE
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Typical Power Dissipation < 2.2 Watts

### APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Medical Electronics: Ultrasound, CAT Instrumentation

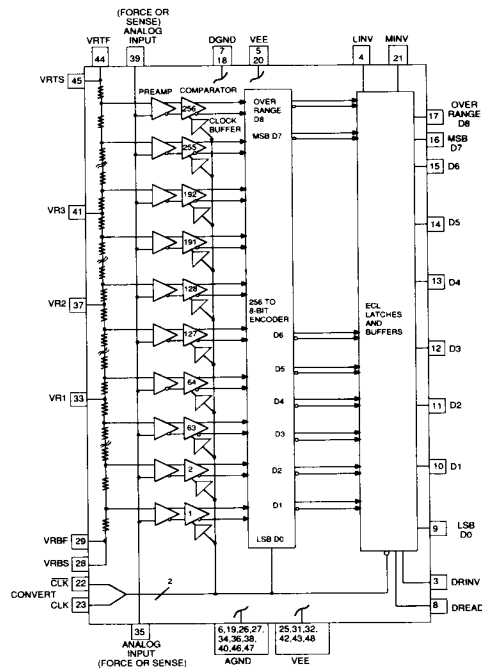
### GENERAL DESCRIPTION

The HADC77200 is a monolithic flash A/D converter capable of digitizing a 2 volt analog input signal with full scale frequency components to 50 MHz into 8-bit digital words at a 150 MSPS (TYP) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth. A single standard -5.2 volt power supply is required for operation of HADC77200, with nominal power dissipation of 2.2 watts.

The part is packaged in a 48 lead ceramic sidebraced DIP. The HADC77200 includes five external reference ladder TAPS to gain better control over linearity; an overrange bit for use in higher resolution systems; and a data ready output pin for ease in interfacing to high-speed memory. Careful attention to design and layout has provided a device with a low noise floor, stable input characteristics, and low data error rate. The HADC77200 is available in industrial and military temperature ranges.

### BLOCK DIAGRAM





**ELECTRICAL SPECIFICATIONS**

$T_C = T_{CASE} = +125\text{ }^\circ\text{C}$ ,  $T_A = T_{AMBIENT}$ ,  $V_{EE} = -5.2\text{ V}$ ,  $R_{SOURCE} = 10\text{ }\Omega$ ,  $VRB = -2.00\text{ V}$ ,  $VRT = 0.00\text{ V}$ ,  $f_{clk} = 100\text{ MHz}$ , Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	LEVEL	ROOM +25 °C			HOT T <sub>MAX</sub>		COLD T <sub>MIN</sub>		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Output High Voltage	50 $\Omega$ to -2 V T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	II I	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	Volts
			-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	Volts
Output Low Voltage	50 $\Omega$ to -2 V T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	II I	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	Volts
			-1.95	-1.80	-1.65	-1.95	-1.65	-2.00	-1.70	Volts
Input High Voltage (MINV, LINV)	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	II I	-1.13		-0.81	-1.07	-0.67	-1.19	-0.87	Volts
			-1.13		-0.81	-1.07	-0.67	-1.22	-0.87	Volts
Input Low Voltage (MINV, LINV)	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	II I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
			-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts

**AC ELECTRICAL CHARACTERISTICS**

Maximum Sample Rate	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	IV I	125	150		125		125		MSPS
			100	150		100		100		MSPS
Clock Low Width, TPW0	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	I I	5	3						ns
			5	3		5		5		ns
Clock High Width, TPW1	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	I I	5	3						ns
			5	3		5		5		ns
Output Delay, TD Differential Clock	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	I I	3	4.2	5					ns
			3	4.2	5	4	7	3	4.5	ns
Output Delay Tempco Differential Clock		V		15						ps/°C
Data Ready Delay Differential Clock	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	I I	3	4						ns
			3	4	5	3.8	7	3.5	4.5	ns
Output Rise Time 10 to 90% 50 $\Omega$ to -2 V	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	I I	1.3	1.9	2.4					ns
			1.3	1.9	2.4	1.3	4	.5	2.2	ns
Output Fall Time 10 to 90% 50 $\Omega$ to -2 V	T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	I I	1.1	1.5	2.2					ns
			1.1	1.5	2.2	1.1	4	.5	2.2	ns
Large Signal Bandwidth	Vin = F.S.	V		100						MHz
Small Signal Bandwidth	Vin=500 mV PP	V		175						MHz
Aperture Jitter		V		12						ps
Aperture Delay	Differential Clock T <sub>A</sub> = -25 to +85 °C T <sub>A</sub> = -55 to T <sub>C</sub>	I I	0.3	1.8	2.3					ns
			0.3	1.8	2.3	0.3	2.8	0.3	2.0	ns
Aperture Delay Tempco	Differential Clock	V		4						ps/°C
Aperture Time		V		<100						ps
Acquisition Time	F.S. to $\pm 1/2$ LSB	V		5						ns
Input Slew Rate		V		800						V/ $\mu$ s

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**ELECTRICAL SPECIFICATIONS**

$T_C = T_{CASE} = +125\text{ }^\circ\text{C}$ ,  $T_A = T_{AMBIENT}$ ,  $V_{EE} = -5.2\text{ V}$ ,  $R_{SOURCE} = 10\text{ }\Omega$ ,  $VRB = -2.00\text{ V}$ ,  $VRT = 0.00\text{ V}$ ,  $f_{clk} = 100\text{ MHz}$ , Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25 °C			HOT T <sub>MAX</sub>		COLD T <sub>MIN</sub>		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>AC ELECTRICAL CHARACTERISTICS</b>										
Total Dynamic Error	$V_{in} = FS @ 1\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	45	48		44.2		44.2		dB dB
Total Dynamic Error	$V_{in} = FS @ 25\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	36.7	38		36.2		36.2		dB dB
Total Dynamic Error, 77200A	$V_{in} = FS @ 50\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	29.5	33		29.2		29.2		dB dB
Signal to Noise Ratio	$V_{in} = FS @ 1\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	46.5	49		45		45		dB dB
Signal to Noise Ratio	$V_{in} = FS @ 25\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	42.5	46		41		41		dB dB
Signal to Noise Ratio, 77200A	$V_{in} = FS @ 50\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	33	38		32.5		32.5		dB dB
Total Harmonic Distortion	$V_{in} = FS @ 1\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	52	56		50.5		52		dB dB
Total Harmonic Distortion	$V_{in} = FS @ 25\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	38	39		36.5		38		dB dB
Total Harmonic Dist, 77200A	$V_{in} = FS @ 50\text{ MHz}$ $T_A = -25\text{ to }+85\text{ }^\circ\text{C}$ $T_A = -55\text{ to }T_C$	I I	32	34		30.5		32		dB dB

**TEST LEVEL CODES**

All electrical characteristics are subject to the following conditions:

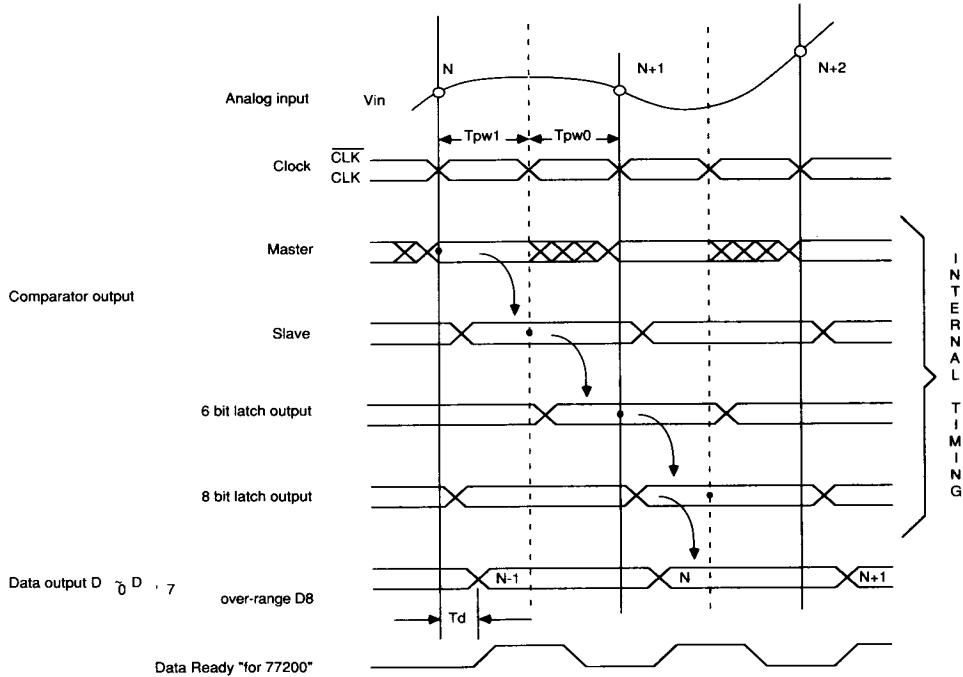
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are performed after die reaches operating temperature.

**TEST LEVEL****TEST PROCEDURE**

- |     |  |
|-----|--|
| I   | 100% production tested at the specified temperature.   |
| II  | 100% production tested at $T_A = 25\text{ }^\circ\text{C}$ , and sample tested at the specified temperatures. QA sample tested only at the specified temperatures. |
| III | Parameter is guaranteed (but not tested) by design and characterization data.  |
| IV  | Parameter is a typical value for information purposes only.  |
| V   |  |

**Timing Diagram**



Dots (+) in the chart denote respective latch timings.

**DEFINITION OF TERMS**

**A/D CONVERTER ERROR SUMMARY**

SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 1B) while a static DC input level may appear close to the ideal (Figure 1A). That is why we are including many dynamic tests as well as the industry standard DC specifications.

tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These errors are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from the measured RMS error for the ideal sinewave and the measured actual RMS error as follows:

**TOTAL DYNAMIC ERROR (EFFECTIVE BITS)**

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual RMS error}}{\text{ideal RMS error}}$$

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is

Furthermore, total dynamic error (TDE) can be related to effective bits by the following formula:

$$\text{TDE (dB)} = 1.8 + 6.02 \times N \text{ (eff bits)}$$



**QUANTIZATION ERROR**

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in  $2^8$  (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is  $Q = FSR/2^N$  where FSR = full scale range and  $N = 8$ . Nonideal quantization bands represent differential nonlinearity errors see Figures 1A and 1B.

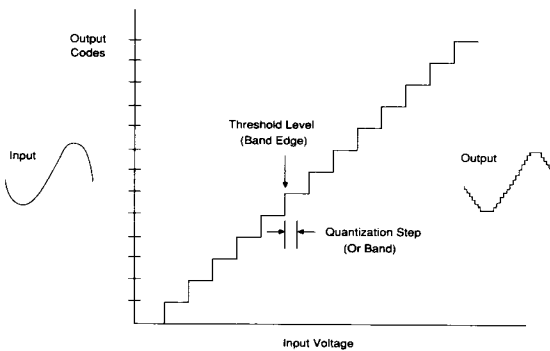
**DIFFERENTIAL NONLINEARITY**

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 1B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77200's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

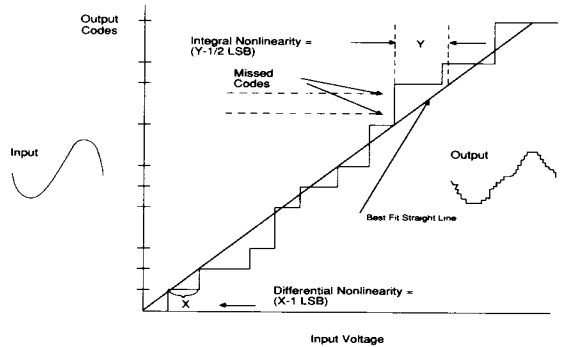
**MISSING CODES**

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 1B points out two missed codes in the transfer function.

**Figure 1A - Static Input Conditions**



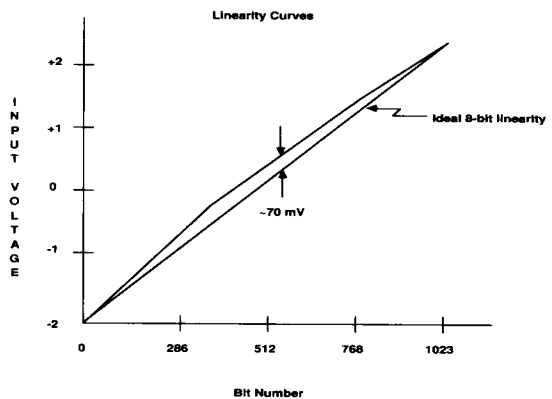
**Figure 1B - Dynamic Conditions**



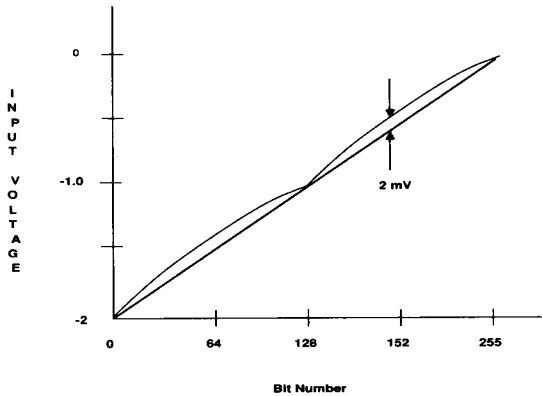
**INTEGRAL NONLINEARITY**

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 2A). Integral nonlinearity does not include any gain or offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 1B shows an integral nonlinearity error of 2 LSBs. The HADC77200's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 5. The resulting effect on the linearity is shown in Figure 2B.

**Figure 2A - Linearity Curve with no TAP adjustment**



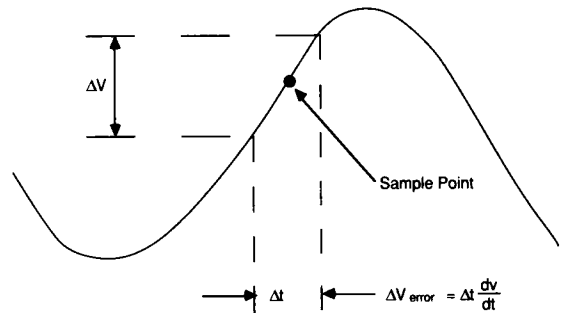
**Figure 2B - Linearity Curve with TAP Forced to Within .5 mV of Ideal**



aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70 ps.

Aperture time and delay are very difficult to measure. However, these values are needed to make intelligent design decisions. SPT supplies these values for the HADC77200 based on both computer design simulations and verified by characterization of samples.

**Figure 2C - Aperture Uncertainty**



**APERTURE UNCERTAINTY**

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point see Figure 2C.

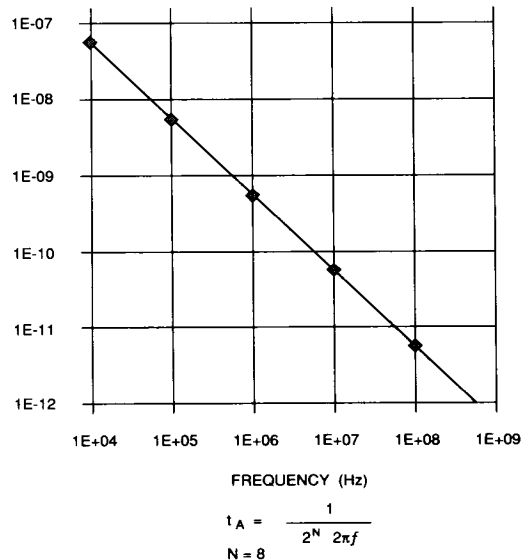
As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sine wave can be calculated for time or voltage by the equation:

$$dV/V = 2 \pi f t_A$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 3 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10 MHz, then from Figure 3 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70 ps. Most data sheets do not state

**Figure 3 - Aperture Time - Sinewaves**



## CHARACTERISTIC TESTING

### TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table I.

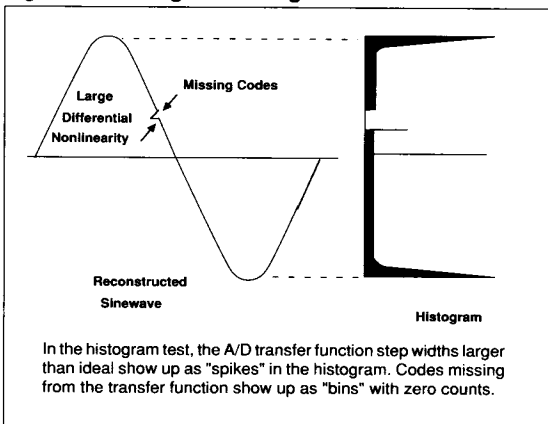
### HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77200. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurrence along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurrence at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts see Figure 4.

Figure 4 - Histogram Testing



### FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Imple-

mented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table I.

### SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77200. Using least squared error minimization techniques, an idealized sinewave fit to the data is calculated by software. The sinewave is in the form:

$$A \sin(2 \pi f t + \theta) + DC$$

where A, f,  $\theta$ , DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave,

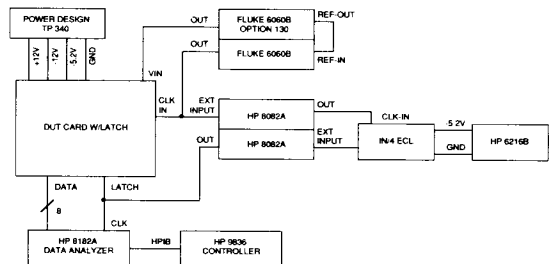
$$A_0 \sin(2 \pi f_0 t + \theta_0) + DC_0$$

is then subtracted from the digitized time record. The rms errors are then calculated and the effective bits specification is found.

### BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77200. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converter's sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency,  $\Delta f$ , is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

### DYNAMIC EVALUATION





**Table I - Tests**

The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

(Table from H.P. Product Note 5180A-2)

ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes.	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts.	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform).	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperture Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

### GENERAL DESCRIPTION

The HADC77200 is the fastest monolithic 8-bit parallel flash A/D converter available today. The minimum conversion rate is 150 MSPS and the analog bandwidth is in excess of 100 MHz. A major advance over previous flash converters is the enclosed 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This reduces clock transient kickback to the input and reference ladder. The preamplifiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range of "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

An additional advantage of the HADC77200 over similar devices is a better integral linearity specification over the

parts entire usable range. The center reference ladder taps are optional as needed to further improve this specification.

The HADC77200 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

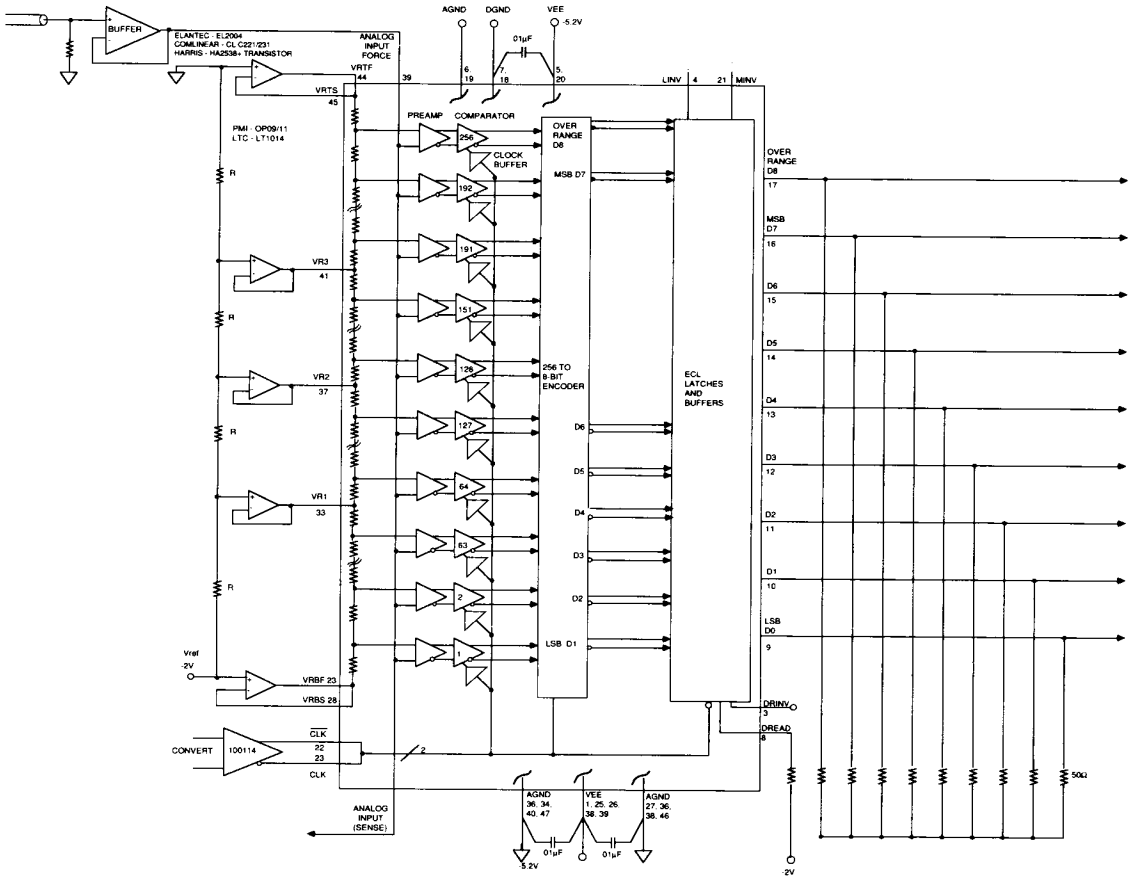
Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77200 has an on board power supply bypass of 1500 pF to reduce external component needs. The output drive capability of the device can provide full ECL swings into 50  $\Omega$  loads.

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**FIGURE 5 - HAD77200 Typical Interface Circuit**



**TYPICAL INTERFACE CIRCUIT**

The HAD77200 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 5 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

**V<sub>EE</sub>, AGND, DGND**

V<sub>EE</sub> is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01  $\mu$ F ceramic capacitor. A 1  $\mu$ F tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 5.

**VIN (ANALOG INPUT)**

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force." This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77200 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

**CLK, CLK (CLOCK INPUTS)**

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since CLK is internally biased to -1.3 V. (See clock input circuit.) It may be left open but a .01  $\mu$ F bypass capacitor from CLK to AGND is recommended. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

**MINV, LINV (OUTPUT LOGIC CONTROL)**

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table II. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to AGND1 through a diode or 3.9 k $\Omega$  resistor.

**D0 TO D7 (DIGITAL OUTPUTS)**

The digital outputs can drive 50  $\Omega$  to ECL levels when pulled down to -2V. When pulled down to -5.2 V the outputs can drive 130  $\Omega$  to 1 k $\Omega$  loads.

**Table II - Output Coding**

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
V <sub>IN</sub>	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V<sub>IH</sub>, V<sub>OH</sub>0: V<sub>IL</sub>, V<sub>OL</sub>**VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (REFERENCE INPUTS)**

These are five external reference voltage taps from -2V (VRB) to AGND (VRT) which can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in Figure 5. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

**DREAD (DATA READY), DRINV (DATA READY INVERSE)**

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the HADC77200's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin (see Timing Diagram).

**D8 (Overrange)**

This is an overrange function. When the HADC77200 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the HADC77200 into higher resolution systems.

**N/C**

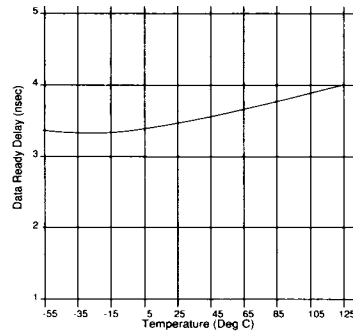
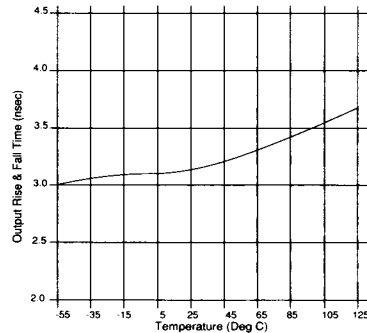
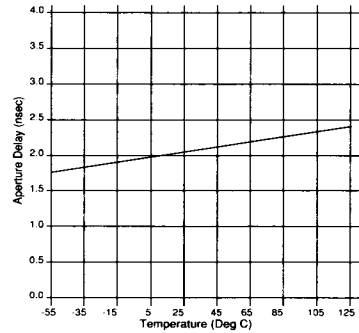
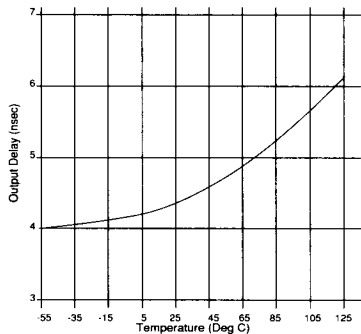
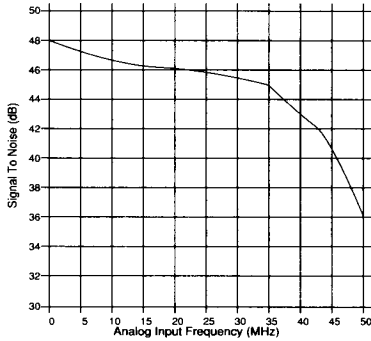
All "Not Connected" pins should be tied to AGND.

**OPERATION**

The HADC77200 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit

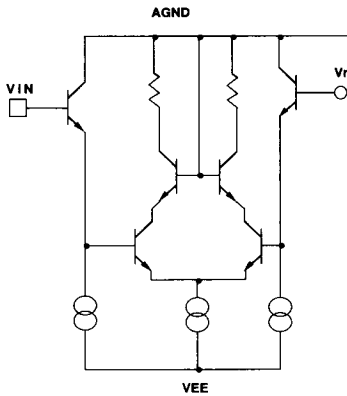
latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

**CHARACTERIZATION GRAPHS**

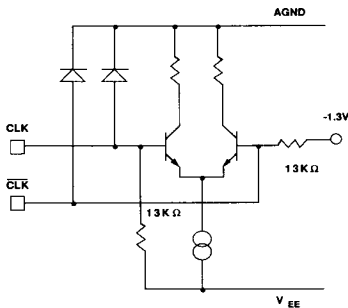


# SUBCIRCUIT SCHEMATICS

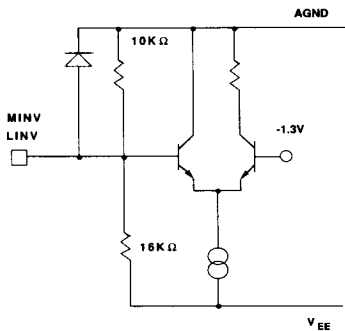
## INPUT CIRCUIT



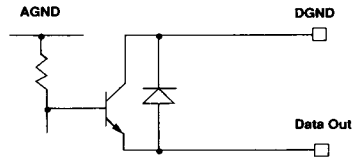
## CLOCK INPUT



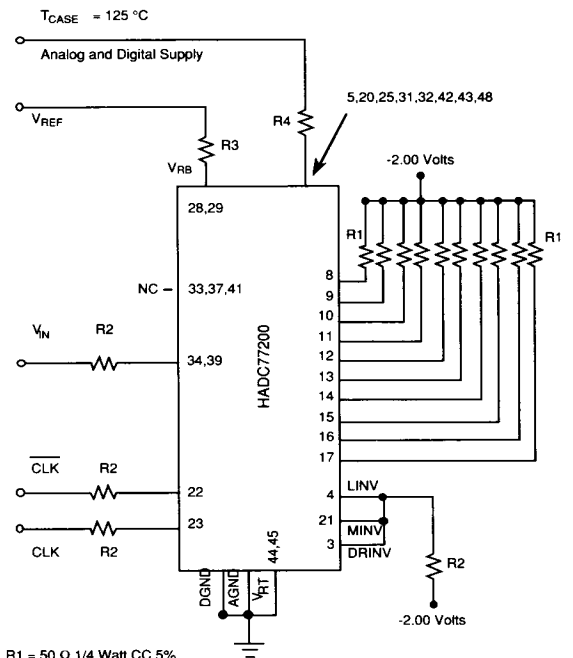
## DRINV, MINV, LINV INPUT CIRCUIT



## OUTPUT CIRCUIT



## BURN-IN CIRCUIT



R1 = 50  $\Omega$  1/4 Watt CC 5%  
 R2 = 1k $\Omega$  1/4 Watt CC 5%  
 R3 = 6.5  $\Omega$  1/4 Watt CC 5%  
 R4 = 3.25  $\Omega$  1/2 Watt CC 5%  
 VREF = -2.00 Volts  
 VEE = -6.6 Volts

**PIN ASSIGNMENT HADC77200**

**TOP VIEW**

1	N/C	VEE	48
2	N/C	AGND	47
3	DRINV	AGND	46
4	LINV	VRTS	45
5	VEE	VRTF	44
6	AGND	VEE	43
7	DGND	VEE	42
8	DREAD	VR3	41
9	D0 (LSB)	AGND	40
10	D1	VIN	39
11	D2	AGND	38
12	D3	VR2	37
13	D4	AGND	36
14	D5	VIN	35
15	D6	AGND	34
16	D7 (MSB)	VR1	33
17	D8 (OVERRANGE)	VEE	32
18	DGND	VEE	31
19	AGND	N/C	30
20	VEE	VRBF	29
21	MINV	VRBS	28
22	CLK	AGND	27
23	CLK	AGND	26
24	N/C	VEE	25

**PIN FUNCTIONS HADC77200**

NAME	FUNCTION
VEE	Negative Supply Nominally -5.2 V
LINV	D0 through D6 Output Inversion Control Pin
DREAD	Data Ready Output
DGND	Digital Ground
AGND	Analog Ground
D0	Digital Data Output Pin 1 (LSB)
D1-D6	Digital Data Output Pin 7
D8	Ovrrange Output
MINV	D7 Output Inversion Control Pin
CLK	ECL Clock Input Pin
CLK	ECL Clock Input Pin
DRINV	Data Ready Inverse
VRBS	Reference Voltage Bottom, Sense Nominally -2.0 V
VRBF	Reference Voltage Bottom, Force, Nominally-2.0 V
VIN	Analog Input, connected to the input signal or used as Sense
VR1	Reference Voltage Tap 1
VR2	Reference Voltage Tap 2
VR3	Reference Voltage Tap 3
VRTS	Reference Voltage Top, Sense, Nominally -2.0 V
VRTS	Reference Voltage Top, Force, Nominally -2.0 V