AMPLIFIER

DESCRIPTION

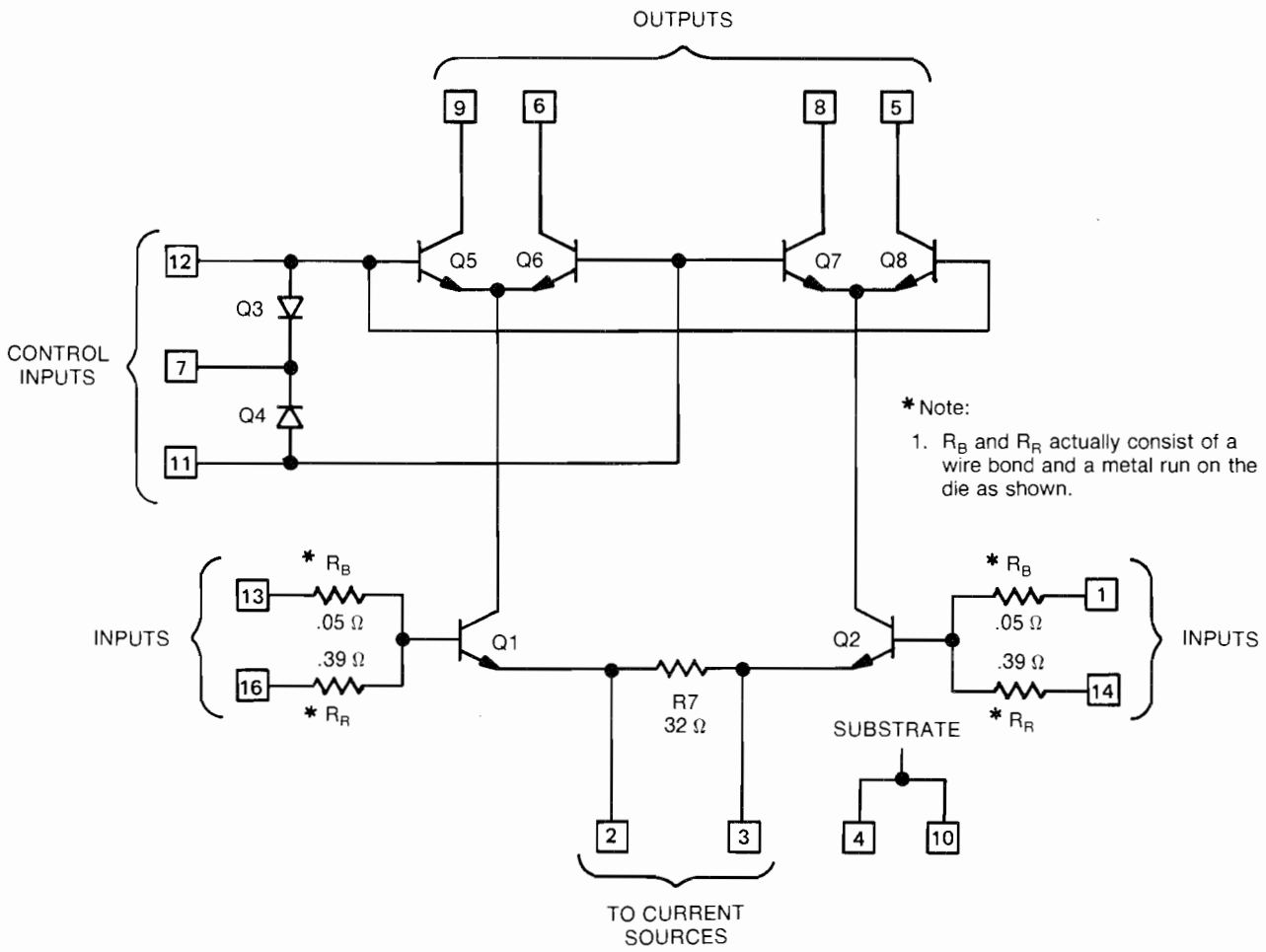
The 155-0078-10 is a monolithic integrated circuit originally designed as an Oscilloscope Vertical Amplifier.

The circuit is a differential in, differential out amplifier with variable gain capabilities. By cross-coupling the output collectors, the circuit is basically a multiplier. DC voltages applied to the control inputs can be used to vary gain from the nominal (maximum) gain through zero to the negative nominal gain. Diodes are provided on the control inputs to linearize the gain characteristics.

FEATURES

- Nominal voltage gain 2.82 (50 Ω source and loads). Set primarily by an on-chip nichrome resistor.
- Gain variable from nominal (either polarity) to zero.
- Nominal bandwidth 1.05 GHz.
- Package leads and etched circuit board can be used to obtain T-coil peaking.
- Available in three versions:
  155-0078-10 (Minipak)
  155-0273-00 (14-pin DIP w/o nichrome resistors)
  155-0274-00 (14-pin DIP) (slower)

SCHEMATIC



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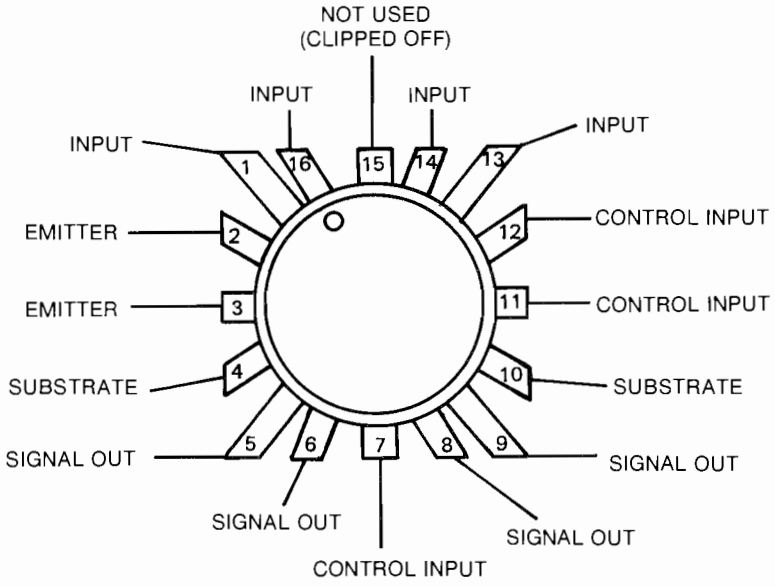
ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	NOTES	VALUES	UNITS
$V_{out\text{-}sub\ MAX}$	Maximum voltage of the outputs (pins 5, 6, 8, 9) relative to the substrate (pin 4).	Prevents collector-substrate breakdown of Q5, Q6, Q7, Q8.	19	V
$V_{out\text{-}cont\ MAX}$	Maximum voltage of the outputs (pins 5, 6, 8, 9) relative to the control inputs (pins 11, 12).	Prevents collector-base breakdown of Q5, Q6, Q7, Q8.	7	V
$V_{cont\text{-}input\ MAX}$	Maximum voltage at the control inputs (pins 11, 12) relative to inputs (pins 1, 13, 14, 16).	Prevents collector-base breakdown of Q1 and Q2.	8	V
$V_{sub\text{-}input\ MAX}$	Maximum voltage of the substrate (pin 4) relative to the inputs (pins 1, 13, 14, 16).	Substrate voltage must be held more negative than any collector in circuit.	0	V
$V_{RQ3\ MAX}$	Maximum voltage from pin 7 to pin 11 or 12.	Maximum steering diode reverse voltage to avoid degradation.	2.5	V
$V_{R11\text{-}R12\ MAX}$	Maximum voltage from pin 11 to 12 or from pin 12 to pin 11.	Maximum steering diode reverse voltage to avoid degradation.	2.5	V
$V_{EB\ MAX}$	Maximum voltage from pin 2 to pin 13 or 16; or from pin 3 to pins 1 or 14.	Maximum base-emitter reverse voltage to avoid degradation.	2	V
I_{MAX}	Maximum current, pins 2 or 3.	40 mA total.	20*	mA
P_{MAX}	Maximum power dissipation.	75°C ambient.	270	mV
$T_{OPERATING}$	Operating temperature range.		0 to 80	°C
$T_{STORAGE}$	Storage temperature range.		−55 to +125	°C
$T_{j\ MAX}$	Maximum junction temperature.		125	°C

*** Contact Applications Engineering, IC Manufacturing, if 20 mA is to be exceeded.**

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	MIN	MAX	UNITS
BV_{CEO} Q1, Q2, at 200 μA	4.4		V
BV_{CEO} Q5, Q6, Q7, Q8 at 200 μA	4.4		V
$BV_{CEO\ SUS}$ Q1, Q2 at 10 mA	4.9		V
$BV_{CEO\ SUS}$ Q5, Q6, Q7, Q8 at 10 mA	4.9		V
SUBSTRATE VOLTAGE in operating configuration		−15	V
INPUT BIAS CURRENT Q1 or Q2 (16 mA emitter current)	64	225	μA
NORMAL OFFSET (OUTPUT)	−14	+14	mV
INVERT OFFSET (OUTPUT)	−14	+14	mV
NORMAL GAIN	2.68	2.96	
INVERT GAIN	2.68	2.96	
NORMAL-INVERT GAIN MATCH	−0.5	+0.5	%
NULL OFFSET (Output offset in null condition)	−10	+10	mV
NULL GAIN	−.14	+.14	
50% GAIN TOLERANCE	.49	.51	$X(AV_{NORM})$
OFF FEEDTHRU (Q5 & Q8 leakage)	−200	+200	μV
MEASURED RISETIME Measurement system risetime less than 100 ps		355	ps

PARAMETRIC DEFINITIONS

The 0078 is specified in three different operating conditions: NORMAL, INVERT and NULL.

In the NORMAL condition, Q5 and Q8 are conducting and Q6 and Q7 are not.

In the INVERT condition, Q6 and Q7 are conducting and Q5 and Q8 are not.

In the NULL condition, Q5, Q6, Q7 and Q8 are all conducting equally.

APPLICATIONS INFORMATION

Output Stage Considerations

Pin 11 and 12 can be voltage driven and pin 7 left open (Figure 1) if gain linearity as a function of control voltage is not critical. The voltage applied on pins 11 or 12 should be 1.2 to 3.7 volts above the quiescent voltage on pins 1, 13, 14, or 16 for conducting output transistors. For nonconducting output transistors pin 11 or 12 can be at a lower potential than this. Absolute maximum ratings must be observed, however. For the case of pin 11 and 12 voltage driven and pin 7 open, gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{\exp\left(\frac{qV_{12}}{kT}\right) - \exp\left(\frac{qV_{11}}{kT}\right)}{\exp\left(\frac{qV_{12}}{kT}\right) + \exp\left(\frac{qV_{11}}{kT}\right)}\right]$$

where $A_{V\,NORM}$ = Normal Gain
V_{11} = voltage applied on pin 11
V_{12} = voltage applied on pin 12
$\frac{kT}{q}$ = 26 mV at room temperature

If gain linearity as a function of control voltage is critical, pin 11 and 12 should be current driven and pin 7 returned to a voltage so as to set pin 11 and 12 voltage to the proper level as mentioned above. Figure 2 shows this type hookup. Current driving these inputs linearizes the gain by making use of the exponential current-voltage relationship of the diodes Q3 and Q4 to cancel that of the output transistors. The gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{I_{12} - I_{11}}{I_{12} + I_{11}}\right]$$

where I_{11} = current into pin 11
I_{12} = current into pin 12

If variable gain of only a single polarity is desired, one pair of outputs can be used and the other pair connected to separate unused leads as in Figure 3.

If fixed maximum gain is desired, one pair of outputs can be left open as in Figure 4.

In applications where the output is to be switched from one output pair to another, the difference in offset voltage between the two outputs should not be specified any tighter than 28 mV (the sum of normal and invert offset specs).

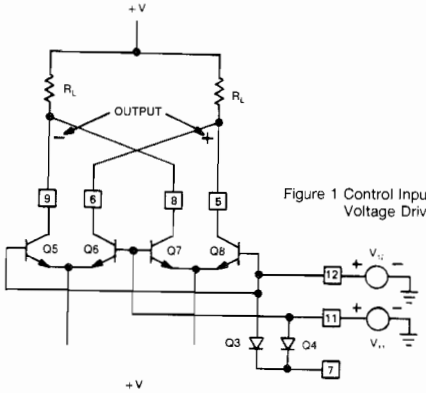


Figure 1 Control Inputs Voltage Driven

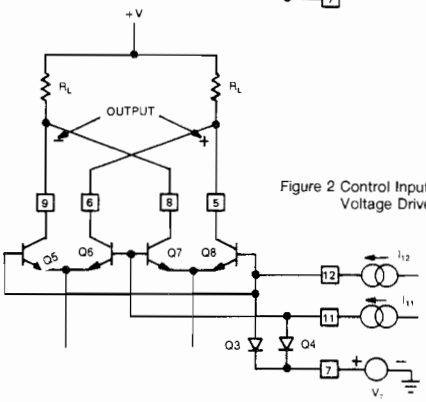
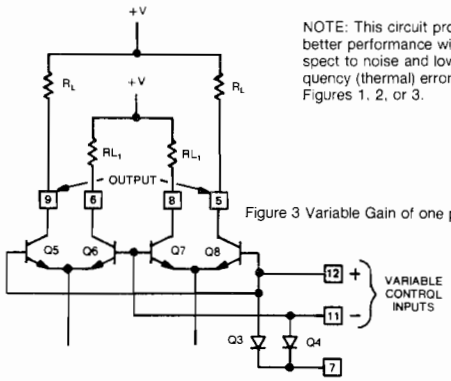
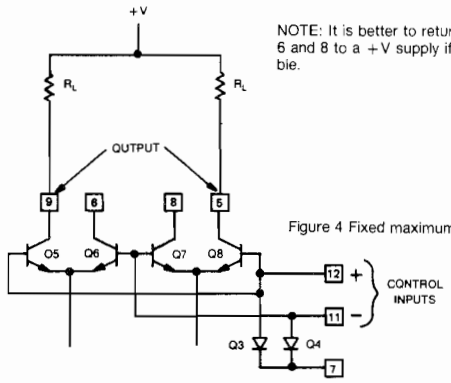


Figure 2 Control Inputs Voltage Driven



NOTE: This circuit provides better performance with respect to noise and low frequency (thermal) errors than Figures 1, 2, or 3.

Figure 3 Variable Gain of one polarity only



NOTE: It is better to return 6 and 8 to a +V supply if possible.

Figure 4 Fixed maximum gain

Input Stage Considerations

The bias current (pin 2 and 3 current) should not exceed 20 mA per side or a decrease in the life of the part may result.

For full bandwidth, T-coil peaking must be used. Package and etched circuit board inductances can be used in the realization of this bridged T circuit[1].

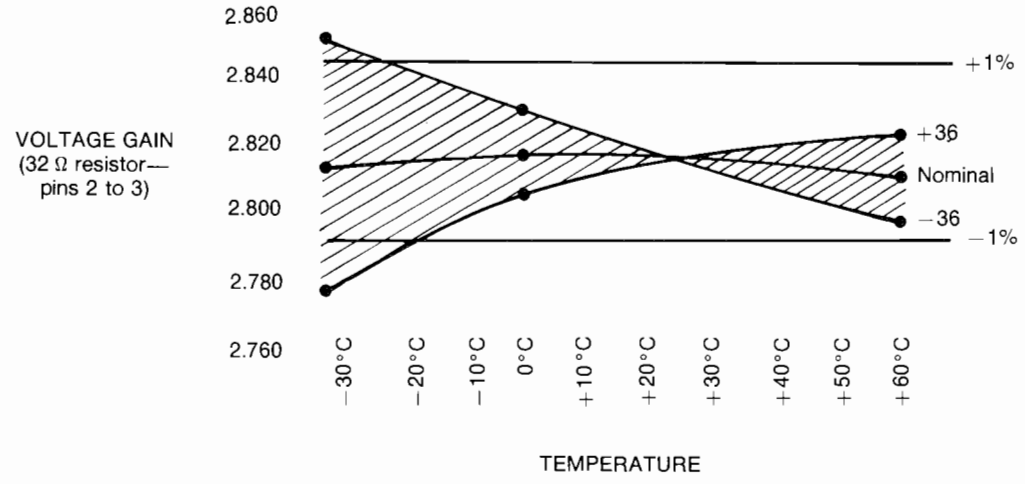
Standing current through pin 16 to 13 and pin 1 to 14 will cause a DC drop due to the run and bond wire resistance in their leads. This resistance provides some intentional improvement in gain vs. temperature and may need to be considered in biasing calculations.

Thermal effects due to signal dependent power dissipation changes in Q_1 and Q_2 cause the low frequency gain to exceed mid band gain by $\approx$1% with Q_1, Q_2 at 15 mA, 2.4 V.

[1]See John Addis' article in *Electronics Magazine* June 5, 1972.

Typical Performance Graph
(not a specification, for information only)

155-0078 GAIN Vs TEMPERATURE



PRODUCT PRECAUTIONS

Input Protection

Input base-emitter voltages should not exceed 2 volts in the negative direction and 1 volt in the positive direction.

Output Loading

Outputs should be limited to less than those listed in Absolute Maximum Ratings.

Power Supply Turn-On/Turn-Off Sequence

Substrate voltage should be turned on coincident with or before the other voltages.

Handling Procedures

Static sensitive handling procedures should be implemented for this part.

RELIABILITY

λ. failure rate $\leq$ .02%/1K hours at 75°C Tj.

$\Theta jc = 87°C/W$.

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