SECTION IV
OPERATION INSTRUCTIONS

4-1. THEORY OF OPERATION. The following discussion describes the operation of the oscilloscope circuitry. First a general description of the overall relationship between the basic circuits is given. Then each circuit is described in detail.

4-2. BASIC CIRCUIT FUNCTIONS. The overall relationship between the basic circuits is described below. Refer to the basic block diagram shown in Figure 4-1 to aid in understanding the discussion.

a. Vertical Module. The Vertical Module contains the CH 1 and CH 2 Input, CH 1 and CH 2 Preamplifier and Vertical Switching Hybrid Integrated Circuit, Vertical Switching Control Circuit, Delay Line Driver and Delay Line, and the Vertical Amplifier (see Figure 4-1).

(1) CH 1 and CH 2 Input. The Input circuits provide input coupling and attenuation for the signals connected to the CH 1 and CH 2 input connectors. AC, DC, and GND coupling modes are provided. Two attenuators in each channel provides attenuation factors of 10:1, 100:1, or when switched in series 1000:1.

(2) CH 1 and CH 2 Preamplifier and Vertical Switching. U4160 is a hybrid integrated circuit which contains the Vertical Switching circuitry and both the CH 1 and CH 2 Preamplifiers.

(a) The signal from the vertical input attenuators is applied to U4160, amplified, and supplied to the Delay Line Driver. In conjunction with the input attenuators, the gain of the preamplifiers is changed to provide the deflection factors indicated by the VOLTS/DIV switches. A sample of the signals present in the amplifiers is supplied to the Trigger Switching and Trigger Input Amplifiers in the Horizontal Module.

(b) The Vertical Switching circuitry selects which preamplifier will supply the signal to the Delay Line Driver.

(3). Vertical Switching Control. Inputs to this circuit are from the VERT MODE switch and from the Sweep Control circuit (alternate sync pulse). The output is supplied to U4160 to control Vertical Switching.

(4) Delay Line Driver and Delay Line. The vertical signal from the CH 1 and CH 2 Preamplifiers is amplified by the Delay Line Driver and supplied to the Delay Line. The Delay Line delays the vertical signal enough so the portion of the vertical signal initiating the sweep can be viewed.

(5) Vertical Amplifier. This circuit amplifies the signal from the Delay Line. The amplified signal is used to drive the vertical deflection plates of the crt.

b. Horizontal Module. The Horizontal Module contains Trigger Input Amplifiers and Trigger Switching, A Trigger Generator, B Trigger Generator, A Sweep Generator, B Sweep Generator, Horizontal Preamplifier, +A GATE OUT Amplifier, +B GATE Buffer, and Sweep Control (see Figure 4-1).

(1) Trigger Input Amplifiers and Trigger Switching. The Trigger Input Amplifiers are buffer amplifiers between the Trigger Generators and the source of the trigger signal. Trigger Switching selects the source of the signal used to trigger the Sweep Generator(s) and selects the method of coupling this signal to the Trigger Generator(s).

(2) A Trigger Generator. Using a signal selected by the A Trigger SOURCE switch, the A Trigger Generator produces a pulse which causes the A Sweep Generator to produce an A sweep ramp.

(3) B Trigger Generator. Using a signal selected by the B Trigger SOURCE switch, the B Trigger Generator produces a pulse which causes the B Sweep Generator to produce a B sweep ramp.

(4) A Sweep Generator. The A Sweep Generator, when initiated by the A Trigger Generator, produces a linear sawtooth output signal. The slope of the sawtooth is controlled by the A TIME/DIV switch.

(5) B Sweep Generator. The B Sweep Generator is basically the same as the A Sweep Generator. However, it produces a sawtooth output signal only after a delay time selected by the A TIME/DIV switch and the DELAY TIME POS control. When the B Trigger SOURCE switch is in the STARTS AFTER DELAY position, the B Sweep Generator begins to produce a sawtooth immediately following the selected delay time. In the other positions of the B Trigger SOURCE switch, the B Sweep Generator does not produce a sawtooth until it receives a trigger pulse occuring after the selected delay time.

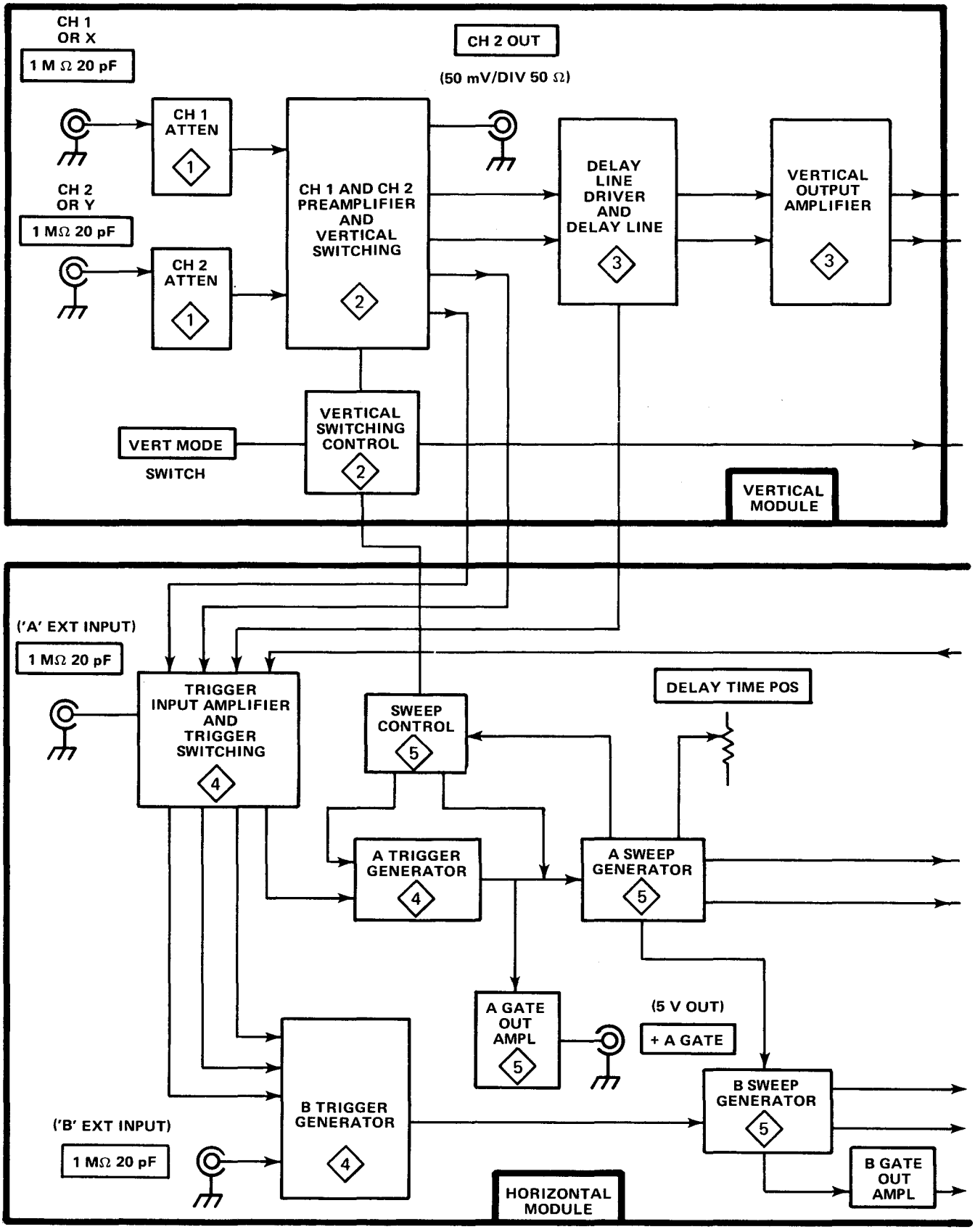

Figure 4-1. Overall block diagram (sheet 1 of 2).

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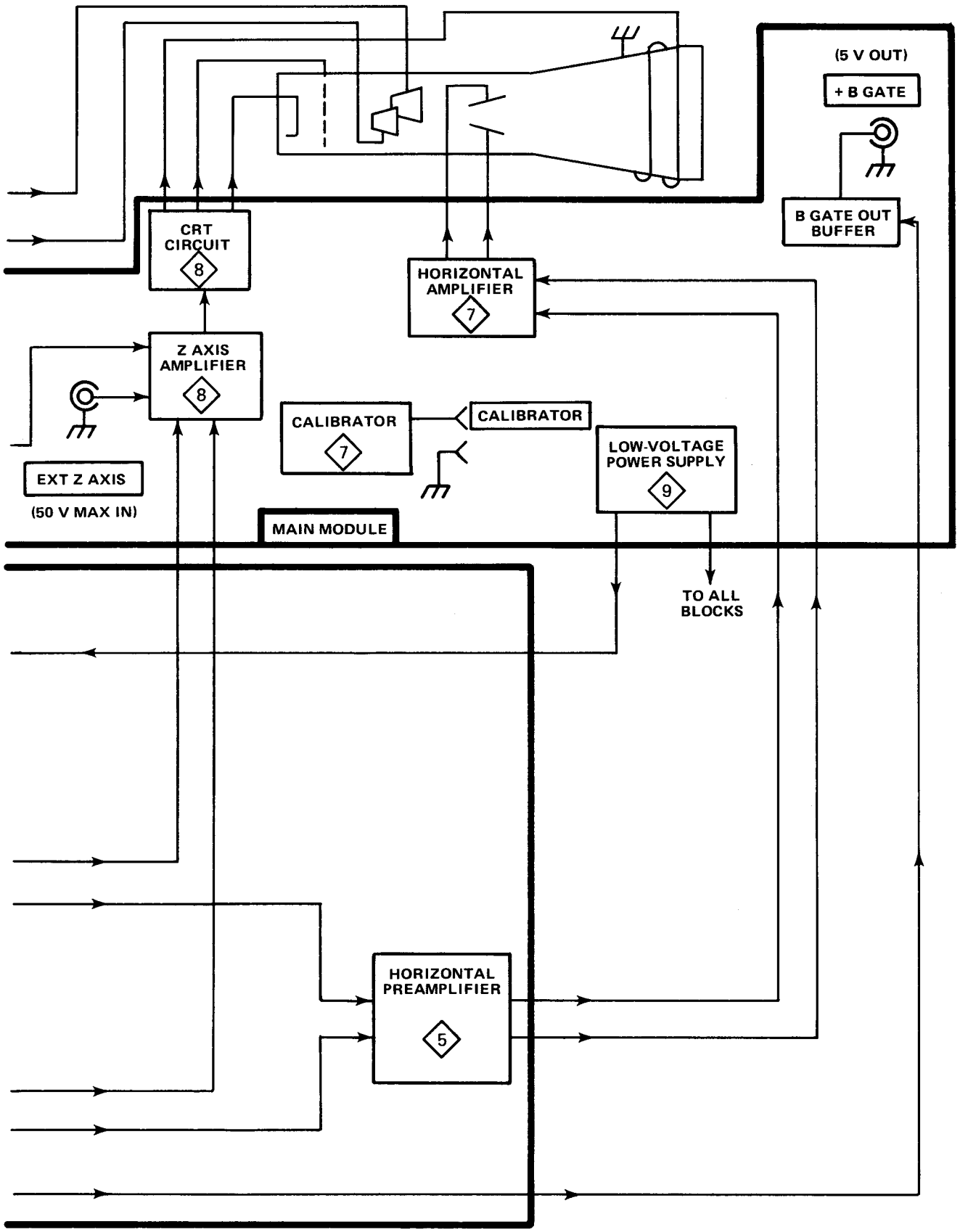


Figure 4-1. Overall block diagram (sheet 2 of 2).

(6) Horizontal Preamplifier. This circuit amplifies the output of the A or B Sweep Generator. The amplified sweep ramp is supplied to the Horizontal Amplifier in the Horizontal Module. In the X10 position of the X10 MAG switch, the gain of the Horizontal Preamplifier is increased by a factor of ten which increases the displayed sweep rate by a factor of ten. In the X-Y position of the TIME/DIV switches, the signal from the CH 1 Preamplifier is connected to the Horizontal Preamplifier and provides horizontal deflection.

(7) +A GATE OUT Amplifier. This circuit samples the A sweep start gate and produces a positive-going rectangular pulse coincident with A sweep time.

(8) +B GATE OUT Buffer. This circuit sums the B sweep holdoff signal from U2690, the delayed gate, and the B sweep gate, and produces an output signal coincident with B sweep time. This output is supplied to the +B GATE OUT Amplifier in the Main Module.

(9) Sweep Control. The Sweep Control circuitry is contained in an integrated circuit. This circuitry controls A Sweep holdoff time and A Trigger mode, and supplies the alternate sync pulse to the Vertical Switching Control circuit.

c. Main Module. The Main Module contains the Z Axis Amplifier, Crt Circuit, Horizontal Amplifier, Calibrator, and Low Voltage Power Supply.

(1) Z-Axis Amplifier. This circuit amplifies the unblanking signals supplied by the Vertical Switching Control circuit, the A Sweep Generator, and the B Sweep Generator. The output controls the brightness of the display through the Crt Circuit.

(2) Crt Circuit. This circuit provides the high voltages needed for operation of the crt.

(3) Horizontal Amplifier. This circuit amplifies the sweep ramp signal supplied by the Horizontal Preamplifier in the Horizontal Module. The output of the Horizontal Amplifier drives the horizontal deflection plates of the crt.

(4) +B GATE OUT Amplifier. This circuit amplifies the signal from the +B GATE OUT Buffer in the Horizontal Module. The amplified signal is supplied to an externally accessable BNC connector. The output signal is a positive-going rectangular pulse coincident with B Sweep time.

(5) Calibrator. The Calibrator provides an externally accessable square-wave output with an accurate voltage amplitude. This signal is used for checking vertical deflection accuracy and probe compensation.

(6) Low Voltage Power Supply. The Low Voltage Power Supply provides the low voltages needed to operate the oscilloscope. The high voltages are supplied by the Crt Circuit.

4-3. DETAILED CIRCUIT OPERATION.

The following detailed circuit description is subdivided according to the overall block diagram shown in Figure 4-1. Simplified diagrams are used, where needed, for clarity. Complete schematic diagrams are located in Section VI.

a. Vertical Module.

(1) CH 1 and CH 2 Input. The CH 1 and CH 2 Input circuits are shown in Diagram 1 (FO-3). These circuits contain the input coupling switches, the vertical attenuators, and input source followers. Both circuits are the same so only the CH 1 circuit will be discussed.

(a) Input Coupling Switches. S4100A selects the method of coupling the input signal to the attenuators.

1 In the DC position of S4100A, the input signal is connected directly to the attenuators.

2 In the AC position of S4100A, the input signal passes through C4102 and then to the attenuators. This blocks the dc component of the input signal.

3 In the GND position of S4100A, the gate of the input source follower (Q4124A) is connected to ground through R4103. Since the resistance of R4103 is so small compared to that of R4102, the percentage of the input signal passed to the gate of Q4124A is negligible. This essentially disconnects the input signal from Q4124A and provides a 0 volt reference display. Also, in the GND position of S4100A, C4102 charges to the average dc level of the input signal through R4102 and R4103. This prevents coupling a high-amplitude transient to Q4124A when S4100A is switched from GND to AC.

(b) Vertical Attenuators. To obtain the vertical deflection factors indicated by the VOLTS/DIV control, the input signal is attenuated and the gain of the Vertical Preamplifier is reduced (see 4-3. a. (2) (a) 1). The attenuators are frequency-compensated voltage dividers. The attenuators provided are a divide by ten and a divide by one hundred. To obtain divide by 1000, the two attenuators are connected in series. Table 4-1 shows the VOLTS/DIV settings and the attenuation and gain switching required to obtain them.

Table 4-1. Attenuation and Gain Switching Sequence

VOLTS/DIV SETTING	ATTENUATION	GAIN REDUCTION
5 mV	1X	1X
10 mV	1X	2X
20 mV	1X	4X
50 mV	10X	1X
100 mV	10X	2X
200 mV	10X	4X
500 mV	100X	1X
1V	100X	2X
2 V	100X	4X
5 V	1000X	1X

(c) Input Source Followers. The signal from the CH 1 attenuator is connected to the gate of Q4124A. The one megohm input impedance seen at J4100 is determined by R4122. To prevent damage to Q4124A in the presence of high-amplitude positive-going input signals, R4123 limits gate current. In the presence of high-amplitude negative-going input signals, CR4124 clamps the gate of Q4124A to about −5.7 volts and R4123 limits the current through CR4124. FET Q4124B provides a relatively constant current source for Q4124A.

(2) CH 1 and CH 2 Preamplifier and Vertical Switching. A schematic diagram of this curcuit is shown in Diagram 2 (FO-4). The preamplifier and switching circuits are both contained in one hybrid integrated circuit (U4160). The preamplifier circuits provide the initial stages of amplification for the vertical input signals. The switching circuit determines which of the vertical input signals will be displayed on the crt.

(a) CH 1 and CH 2 Preamplifier. The single-ended signals from the input source followers are connected to terminals 1 and 32, respectively of U4160. The single-ended input signals are converted to paraphase signals and internally connected to the Vertical Switching circuit.

1 **Gain Switching.** To provide the vertical deflection factors indicated by the VOLTS/DIV control, the gains of the preamplifiers are reduced and attenuators are switched into the signal path, see 4-3. a. (1) (b). The CH 1 gain setting resistors are connected from terminals 4 and 6 to terminals 7 and 8 of U4160. The CH 2 gain setting resistors are connected from terminals 29 and 31 to terminals 26 and 27 of U4160. The VOLTS/DIV switches determine which gain setting resistors are used. Table 4-1 shows the VOLTS/DIV settings and the attenuation and gain switching needed to obtain them.

2 **CH 2 INVERT.** The CH 2 signal can be inverted as displayed on the crt. This is done by inverting the signal in the CH 2 Preamplifier. The polarity of the CH 2 signal is determined by the dc voltage on terminals 34 and 36 of U4160. With 0.8 volts on terminal 34 and 0.0 volts on terminal 36, the CH 2 signal is not inverted. To invert the signal, the INVERT switch (S4240) is pushed, which sets terminal 34 to 0.0 volts and terminal 36 to 0.8 volts.

(b) Vertical Switching. Transistor gates within U4160 allow either the CH 1 or CH 2 signal to be connected to the output of U4160 (terminals 17 and 18). The transistor gates are controlled by the Vertical Switching Control circuit. Figure 4-2 shows a simplified diagram of the transistor gates and the Vertical Switching Control circuit. Figure 4-2 shows the signal path with the VERT MODE switch set to CH 1.

(c) CH 1 and CH 2 Trigger Pickoff. U4160 supplies samples of the signals present in the CH 1 and CH 2 Preamplifiers to the trigger circuits. The CH 1 trigger signal output is at terminal 13 of U4160 and the CH 2 trigger signal output is at terminal 22 of U4160.

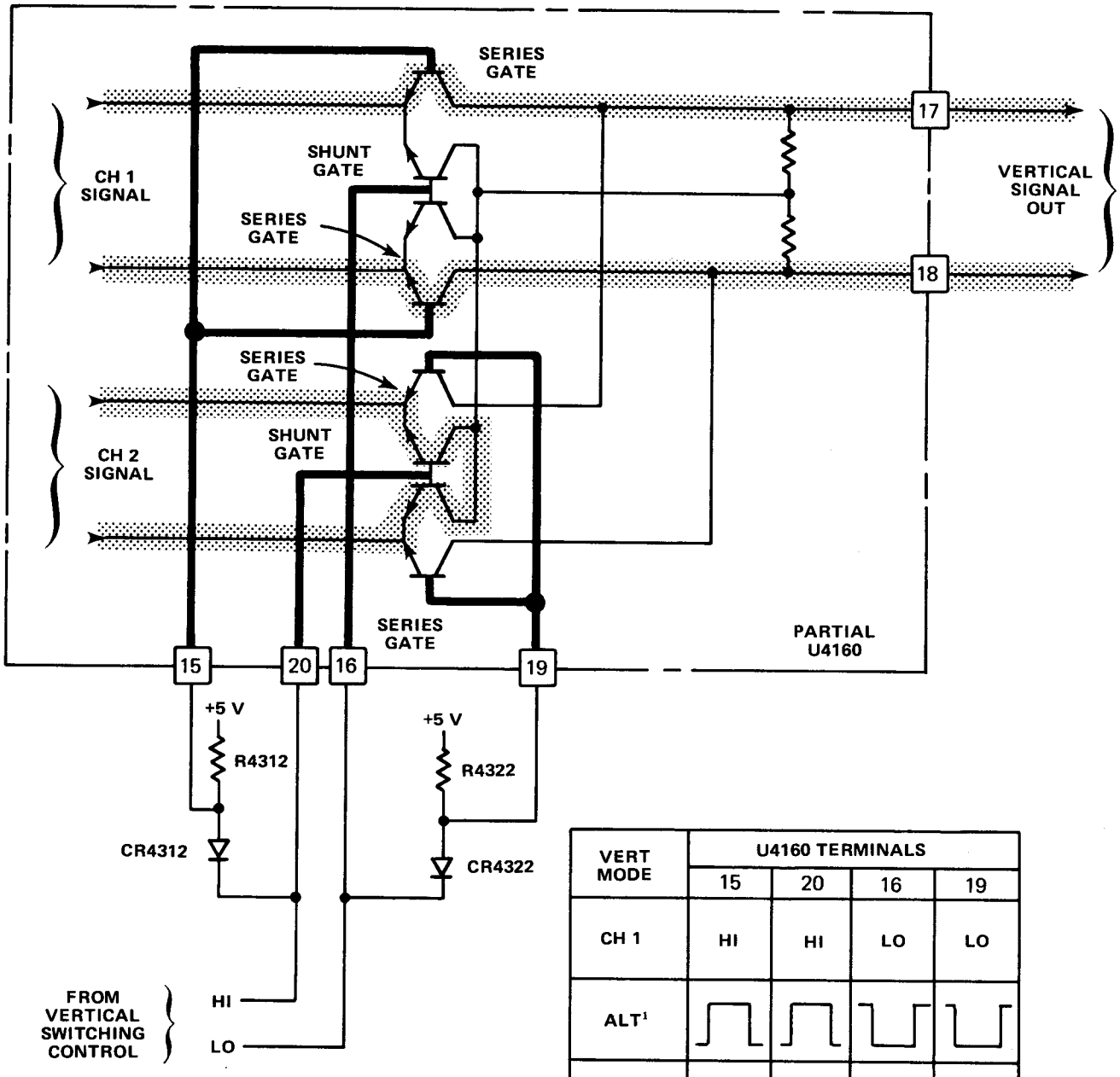
(d) CH 2 OUT Signal Pickoff. Terminal 21 of U4160 supplies a sample of the signal present in the CH 2 Preamplifier to the base of Q4282. This signal is amplified through Q4282 and Q4288, then connected to the CH 2 OUT connector (J4289).

(e) X-Axis Signal Pickoff. A sample of the signal present in the CH 1 Preamplifier is supplied to terminal 14 of U4160. In the X-Y horizontal mode, this signal is connected to the Horizontal Preamplifier in the Horizontal Module and provides horizontal deflection for the crt.

(3) Vertical Switching Control. Diagram 2 (FO-4) shows the Vertical Switching Control circuitry. Transistor gates within U4160 determine which of the signals in the CH 1 and CH 2 Preamplifiers is supplied to the output of U4160 (terminals 17 and 18). The CH 1 gate is controlled by the voltages on terminals 15 and 16 of U4160. The CH 2 gates are controlled by the voltages on terminals 19 and 20 of U4160. These voltages are controlled by the channel switching multivibrator and the VERT MODE switch.

(a) Channel Switching Multivibrator. The channel switching multivibrator consists of Q4316 and Q4326. The multivibrator operates in the CHOP and ALT settings of the VERT MODE switch. In the CHOP mode, the multivibrator is free running at about 250 kilohertz. In the ALT mode it switches states when triggered by the alternate trace sync pulse through Q4334.

(b) CH 1 Vertical Mode. When the VERT MODE switch is set to CH 1, −5 volts is connected to R4323 through the VERT MODE switch S4330. Resistors R4323 and R4322 form a divider which sets terminals 16 and 19



VERT MODE	U4160 TERMINALS			
	15	20	16	19
CH 1	HI	HI	LO	LO
ALT[1]				
ADD	HI	LO	HI	LO
CHOP[2]				
CH 2	LO	LO	HI	HI

[1] CHANGES STATES AT THE END OF EACH SWEEP.
[2] REPETITION RATE ABOUT 250 kHz.

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Figure 4-2. Channel switching gates.

of U4160 LO. Terminals 15 and 20 of R4160 are pulled HI through R4312. This turns off the CH 2 series gate and turns on the CH 1 series gate. The CH 1 signal passes to terminals 17 and 18 of U4160.

(c) CH 2 Vertical Mode. This mode works the same as the CH 1 mode except −5 volts is connected to R4313 setting terminals 15 and 20 LO and terminals 16 and 19 are pulled HI through R4322. This turns on the CH 2 series gate and allows the CH 2 signal to pass to terminals 17 and 18 of U4160.

(d) Add Vertical Mode.

1 In the ADD mode the algebraic sum of the output signals from the CH 1 and CH 2 Preamplifiers is supplied to terminals 17 and 18 of U4160.

2 When the VERT MODE switch (S4330) is set to ADD, neither R4313 nor R4323 are connected to −5 volts. This allows terminals 15 and 19 to be pulled HI through R4312 and R4322 respectively. Terminal 20 is also pulled positive through R4312 but, because of CR4312, terminal 20 is LO with respect to terminal 15. In the same way, terminal 16 is LO with respect to terminal 19 due to CR4322. This turns on both the CH 1 and CH 2 series gates and turns off both shunt gates (see Figure 4-2). Both signals pass to terminals 17 and 18 of U4160.

(e) ALT Vertical Mode. In the ALT mode the channel switching multivibrator operates as a bistable multivibrator. The state of the multivibrator is switched at the end of each sweep. The CH 1 and CH 2 signals are individually displayed on alternate sweeps.

1 When the VERT MODE switch is set to ALT, −5 volts is connected to the emitter of Q4334 through R4333. The base of Q4334 is pulled positive with respect to its emitter through R4334. This turns on Q4334 and provides the negative supply voltage for the multivibrator.

2 When Q4334 turns on, either Q4316 or Q4326 will turn on. Assume Q4316 turns on. This pulls terminals 15 and 20 of U4160 LO. Terminals 16 and 19 are pulled HI through R4322. This blocks the CH 1 signal and passes the CH 2 signal to terminals 17 and 18 of U4160.

3 While Q4316 is on, the end of C4316 connected to the emitter of Q4316 charges positive with respect to the end connected to the emitter of Q4326.

4 At the end of each sweep, the Sweep Control circuit in the Horizontal Module supplies a negative-going pulse to the base of Q4334. This momentarily turns off Q4334 removing the ngative supply voltage from the multivibrator. Neither Q4316 nor Q4326 can conduct.

5 We previously assumed Q4316 was on and had charged the end of C4316 connected to the emitter of Q4316 positive with respect to its other end. When Q4334 again turns on, the emitter of Q4326 will be more negative than the emitter of Q4316. Therefore Q4326 will turn on, reversing the previously assumed condition. Terminals 16 and 19 of U4160 will be pulled LO through Q4326 and terminals 15 and 20 will be pulled HI through R4312. The CH 2 signal will be blocked and the CH 1 signal will pass to terminals 17 and 18 of U4160.

(f) CHOP Vertical Mode. In the CHOP mode the channel switching multivibrator operates as an astable multivibrator. The CH 1 and CH 2 signals are alternately displayed during the same sweep. The switching transients are blanked and cannot be seen.

1 When the VERT MODE switch is set to CHOP, −5 volts is connected to the emitters of Q4316 and Q4326 through R4318 and R4328, respectively. This provides the negative supply voltage for the channel switching multivibrator. The multivibrator operates as an astable multivibrator with a repetition rate of about 250 kilohertz. Transistors Q4316 and Q4326 conduct alternately to switch the CH 1 and CH 2 transistor gates in the same manner as for the ALT setting of the VERT MODE switch.

2 The frequency determining components are C4316, R4318, and R4328.

3 The chop blanking amplifier (Q4338) provides an output pulse to the Z Axis Amplifier to blank the switching transients. During the time the multivibrator is switching, the current change in the primary of T4335 induces a voltage in the secondary. This induced voltage drives the base of Q4338 negative which turns it off. The resulting positive-going pulse on the collector of Q4338 is supplied to the Z Axis Amplifier in the Main Module. The length of this pulse is determined by R4335 and C4335.

(4) Delay Line Driver and Delay Line. Diagram 3 (FO-5) shows the Delay Line Driver and Delay Line circuitry. The Delay Line Driver buffers the vertical signal from terminals 17 and 18 of U4160 and supplies it to the Delay Line. The Delay Line delays the vertical signal about 120 nanoseconds. The Delay Line Driver and Delay Line circuitry also contains the NORM trigger signal pickoff, the BW LIMIT 20 MHz switch, and the TRIG VIEW switch.

(a) Delay Line Driver. The output from the channel switching gates, at terminals 17 and 18 of U4160, is applied to the Delay Line Driver (Q4342, Q4352, Q4362, and Q4372). Transistors Q4342 and Q4352 buffer the output of U4160 to provide optimum frequency response. Transistors Q4362 and Q4372 are connected as feedback

amplifiers with R4362 and R4372 providing feedback. Resistors R4365 and R4375 provide reverse termination for the Delay Line.

(b) NORM Trigger Signal Pickoff. A sample of the signal present in the Delay Line Driver is supplied to the base of emitter follower Q4384. The signal on the emitter of Q4384 is supplied to the Trigger Switching circuit in the Horizontal Module. This signal is used to trigger the sweep on the signal providing vertical deflection regardless of the setting of the VERT MODE switch.

(c) BW LIMIT 20 MHz Switch. When the BW LIMIT 20 MHz switch (S4380) is pulled, a low-pass filter is placed in the vertical path between the Delay Line Driver and the Delay Line. The filter components are C4388, C4389, L4378, and L4388. The inductors are in series with the signal path blocking high frequencies and the capacitors are in parallel with the signal path shunting high frequencies. This limits the upper −3 dB point of the vertical system to 20 megahertz.

(d) TRIG VIEW Switch. When the TRIG VIEW switch (S4380) is pushed in and held, the vertical signal is disconnected from the Delay Line input and a sample of the signal being applied to A Trigger Generator is applied in its place. This allows viewing the signal being applied to the A Trigger Generator at the time the sweep is triggered. This is useful when using an external source for triggering (in the EXT and EXT ÷ 10 positions of the A SOURCE switch).

(e) Delay Line. The Delay Line (DL4400) provides about 120 nanoseconds of signal delay. The delay allows the Trigger Generator to initiate sweep generation before the vertical signal reaches the crt. This allows viewing the portion of the vertical input signal at which the sweep is triggered.

(5) Vertical Amplifier. The Vertical Amplifier amplifies the signal from the output of the Delay Line to a level sufficient to drive the vertical deflection plates of the crt.

(a) The Vertical Amplifier is a two-stage cascode amplifier. The first stage consists of Q4421, Q4429, Q4431, and Q4439. The second stage consists of Q4447, Q4463, Q4457, and Q4473. A cascode amplifier consists of a common-emitter amplifier driving a common-base amplifier.

(b) The series RC networks between the emitters of Q4421 and Q4431 in the first stage provide high-frequency compensation. Thermistor RT4419 and varactors CR4416 and CR4417 correct for changes in high-frequency compensation as temperature changes.

(c) As temperature increases the gain of an amplifier of this type decreases. To compensate for this, the resistance of thermistor RT4416 decreases as temperature increases. This reduces the emitter resistance of Q4421 and Q4431. The decreased emitter resistance decreases the negative feedback due to the emitter resistance and holds the gain constant as temperature increases.

(d) Overall gain of the Vertical Amplifier is adjusted by R4443. Adjusting R4443 changes the collector load resistance on Q4429 and Q4439.

(e) Part of the BEAMFINDER switch (S500) is located in the Vertical Amplifier.

1 When S500 is not pushed, the junction of R4427 and R4437 is directly connected to +5 volts through S500. Resistors R4427 and R4437 supply current to Q4429 and Q4439.

2 When S500 is pushed, it removes +5 volts from the junction of R4427 and R4437. Now +5 volts is supplied to the junction of R4427 and R4437 through R4425. The increased resistance reduces the current supplied to Q4429 and R4439 reducing their dynamic range. The reduced dynamic range prevents Q4429 and Q4439 from passing any vertical signals which would cause an off-screen display. The resulting vertical display is compressed and always appears on the crt regardless of the amplitude of the input signal or the setting of the vertical POSITION control.

b. Horizontal Module.

(1) Trigger Input Amplifiers and Trigger Switching. Diagram 4 (FO-6) shows a schematic diagram of this circuit. The Trigger Input Amplifier buffers the trigger signal. The Trigger Switching circuit selects the source of the trigger signal and the method of coupling the trigger signal to the Trigger Generator.

(a) CH 1 and CH 2 Trigger Input Amplifiers. The CH 1 and CH 2 trigger signals are supplied by U4160 in the Vertical Module. The signals pass through emitter followers Q4142 and Q4122. The outputs of the emitter followers are supplied to the SOURCE switches.

(b) NORM Trigger Input Amplifier. The NORM trigger signal is picked off the Delay Line Driver circuit. Emitter follower Q4384, in the Delay Line Driver circuit, buffers the signal and supplies it to the SOURCE switches.

(c) EXT Trigger Input Amplifier.

1 The A EXT Trigger Input Amplifier consists of Q2212, Q2214, and Q2216. The B EXT Trigger Input Amplifier consists of Q2112, Q2114, and Q2116. Both amplifiers are the same so only the A EXT Trigger Input Amplifier will be discussed.

2 The A EXT trigger signal is applied to J2205. The signal passes through one of two voltage dividers. The A SOURCE switch (S2200) determines which divider is selected. In the EXT position, the A SOURCE switch selects the divider composed of R2205-C2205 and R2206-C2206. In the EXT position the selected divider attenuates the input signal by a factor of about 4. In the EXT ÷ 10 position, the A SOURCE selects the divider composed of R2203-C2203 and R2204-C2204. In the EXT ÷ 10 position the selected divider attenuates the input signal by a factor of about 40. The capacitors in parallel with the divider resistors provide correct voltage divider action at high frequencies.

3 In the AC, LF REJ, and HF REJ positions of the A COUPLING switch (S2220), the signal from the output of the selected voltage divider is coupled to the gate of Q2212 through a capacitor (C2212). In the DC position, the signal is directly connected to the gate of Q2212.

4 The EXT signal is applied to the gate of source-follower Q2212. FET Q2214 provides a relatively-constant current source for Q2212. Diode CR2214 compensates for current changes as temperature changes by slightly adjusting the bias on Q2214. The signal on the source of Q2212 is applied to the base of emitter follower Q2216. The signal on the emitter of Q2216 is supplied to the A SOURCE switch.

5 To protect Q2212 in the presence of high-amplitude positive-going input signals, R2203 or R2205 (depending on the A SOURCE setting) limits the gate current that can be drawn by Q2212. In the presence of high-amplitude negative-going signals, CR2213 becomes forward biased. The path for current flow is from −5 volts through R2229, CR2213, and R2204 or R2205. Resistor R2203 or R2205 limits the current through R2229 and CR2213 preventing the anode of CR2213 from going more negative than about −6 volts.

(d) Trigger Switching. Trigger SOURCE Switching selects the source of the signal applied to the Trigger Generators. Trigger COUPLING Switching determines the band of frequencies supplied to the Trigger Generators. The A and B Trigger Switching circuits are the same except A SOURCE has a LINE position and B SOURCE has a STARTS AFTER DELAY position. The LINE position supplies a sample of the power line voltage from the Low-Voltage Power Supply to the A Trigger Generator. The STARTS AFTER DELAY position will be discussed in the B Trigger Generator description. Since both circuits are so similiar, only the A Trigger Switching circuit will be discussed.

1 Two paths exist for the triggering signal. The high-frequency signal components connect directly to input pins of U2260. The low-frequency signal components connect to pin 19 of U2260 through the A SOURCE switch.

Figure 4-3A shows a simplified diagram of the low-frequency signal path. Figure 4-3B shows a simplified diagram of the high-frequency signal path.

2 Figure 4-4 shows a simplified diagram of signal flow with A SOURCE set to NORM and A COUPLING set to AC. Other SOURCE settings operate in a similar manner. Each of the high-frequency signal inputs to U2260 is internally connected to the base of an emitter follower. Normally these emitter followers are prevented from conducting by connecting the base to −2 volts through a pair of resistors (see Figure 4-4). To select a high-frequency input, the junction of these resistors is connected to ground through the SOURCE switch which allows the emitter in U2260 to conduct. For instance, to select the NORM trigger source, the junction of R2233 and R2238 is grounded through the A SOURCE switch (see Figure 4-4).

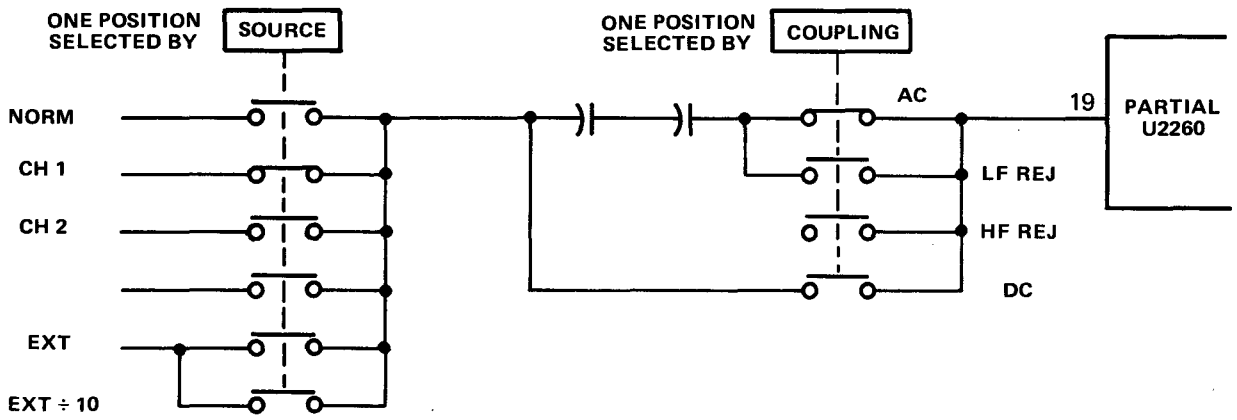
3 For all A COUPLING settings except HF REJ, the resistor junction selected is connected to ground through the A COUPLING switch (see Figure 4-3B and Figure 4-4). In the HF REJ position, the selected resistor junction is disconnected from ground and pin 4 of U2260 is selected by grounding the junction of R2243 and R2242. Pin 4 must be selected even though no signal is connected to it because one of the emitter followers within U2260 must be selected for proper operation of U2260. Since the high-frequency signal path is opened the only signal supplied to the A Trigger Generator is through the low-frequency path.

4 For the AC and HF REJ positions of the A COUPLING switch, the low-frequency signal is ac coupled through C2226 and C2227 to pin 19 of U2260. In the dc position, the low-frequency signal is dc coupled (C2226 and C2227 are bypassed). In the LF REJ position, the low-frequency signal is interrupted and only the high-frequency signal is connected to the A Trigger Generator.

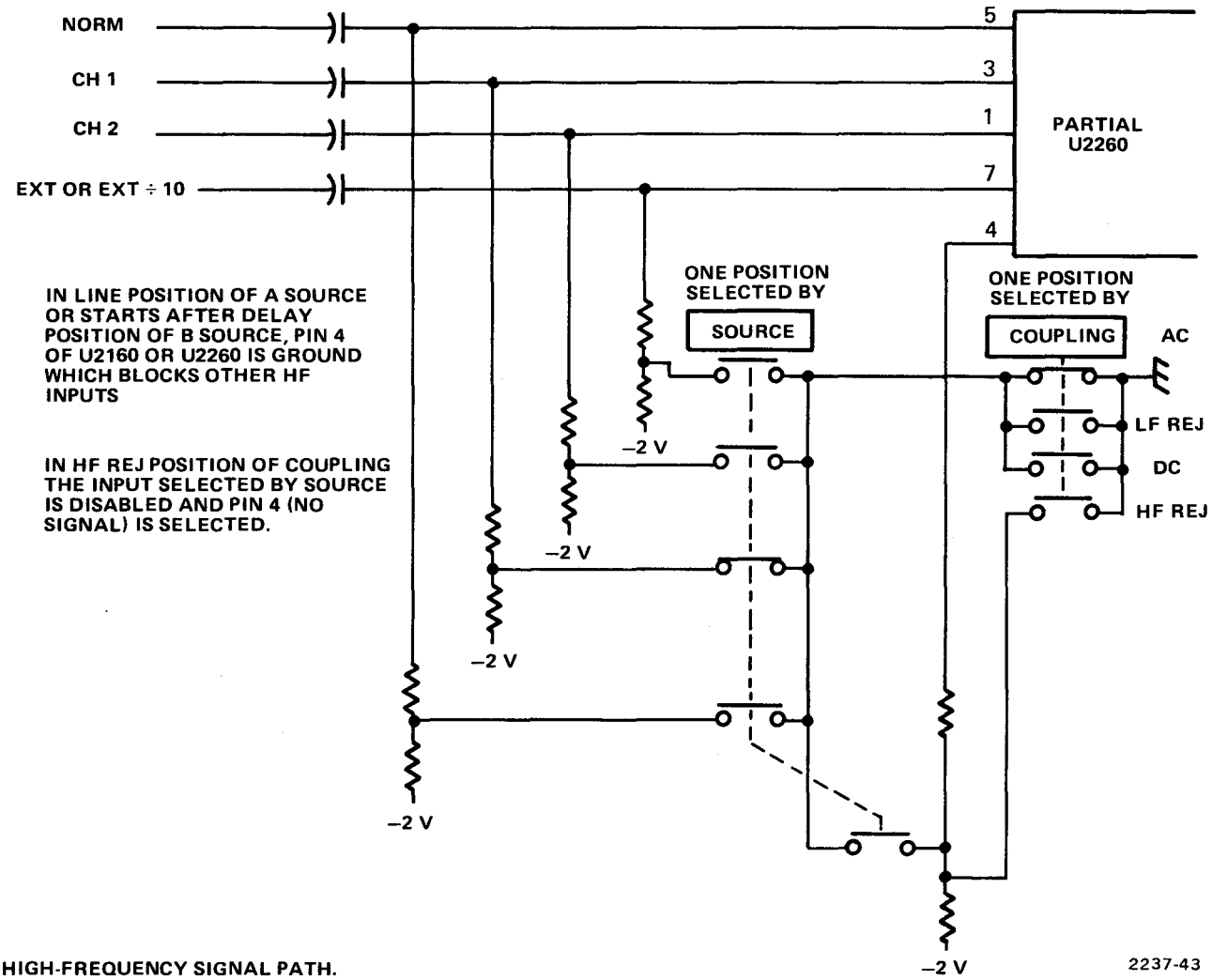
(2) A Trigger Generator. The A Trigger Generator consists of U2260 and associated circuitry. Figure 4-5 shows a simplified diagram of the A Trigger Generator.

(a) Sequence of Events During Trigger Generation. The following discussion will follow the sequence of events in the A Trigger Generator. Refer to Figure 4-5 throughout the discussion.

1 **During Holdoff.** Point E is held HI by the holdoff gate at pin 17 of U2260. Point I is held HI by the complement sweep gate output at point L causing point J to be LO. Both of the arm latch inputs are LO. The output of the arm latch (point K) has previously been reset to HI (at the beginning of holdoff by the holdoff signal applied to pin 17 of U2260). When point K is HI, pin 14 will be held LO regardless of the trigger signal input. The sweep gate latch is held off.



A. LOW-FREQUENCY TRIGGER SIGNAL PATH.



B. HIGH-FREQUENCY SIGNAL PATH.

Figure 4-3. Trigger switching.

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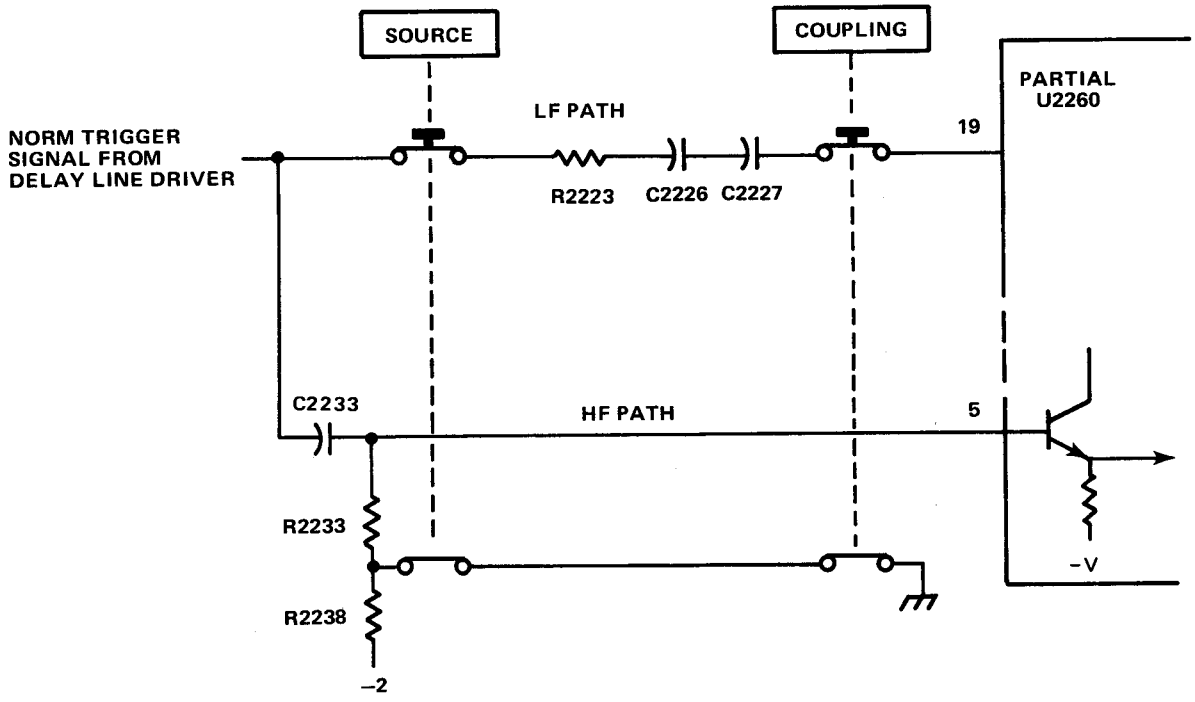


Figure 4-4. Trigger signal paths with SOURCE set to NORM and COUPLING set to AC.

2 At the End of Holdoff. At the end of holdoff, pin 17 of U2260 steps LO causing point H to step HI. There are now two possibilities depending on the state of the signal at point A. If the trigger input signal at point A is above the 3.55 volt threshold at the end of holdoff, no further changes will occur at this time. The HI at point K will continue to hold pin 14 LO. If the trigger input signal at point A is below the 3.55 volt threshold at the end of holdoff (or the first time after the end of holdoff the trigger input signal falls below the 3.55 volt threshold), point D goes LO setting point F HI. This sets the arm latch causing point K to go LO. With point K LO, the sweep gate latch will be allowed to change states.

3 After the Arm Latch Sets. After the arm latch sets, the first voltage at point A that is more positive than the 3.65 volt threshold, causes point B to go HI. This causes the output of the sweep gate latch (pin 14 of U2260) to go HI. The HI on pin 14 causes the A Sweep Generator to begin generating a sweep ramp.

4 Beginning of Holdoff. At the end of A Sweep time, the holdoff gate at pin 17 of U2260 steps HI. This causes point H to step LO. Point I is set to LO whenever the sweep gate (at pin 14) is HI. With points H and I both LO, point J momentarily steps HI. This resets the arm latch causing point K to go HI. When point K goes HI, the sweep gate goes LO and point I goes HI setting point J LO. The holdoff condition described in paragraph 4-3. b. (2) (a) 1 is restored.

(b) Slope Selection. The slope of the trigger input signal, on which a sweep gate is generated, is determined by the voltage connected to pin 8 of U2260. When the voltage is negative, the signal at point A is inverted (see Figure 4-5).

(c) LEVEL Control. The LEVEL control (R2253) shifts the dc level of the signal appearing at point A. This changes the position on the signal where the signal passes through the threshold voltage.

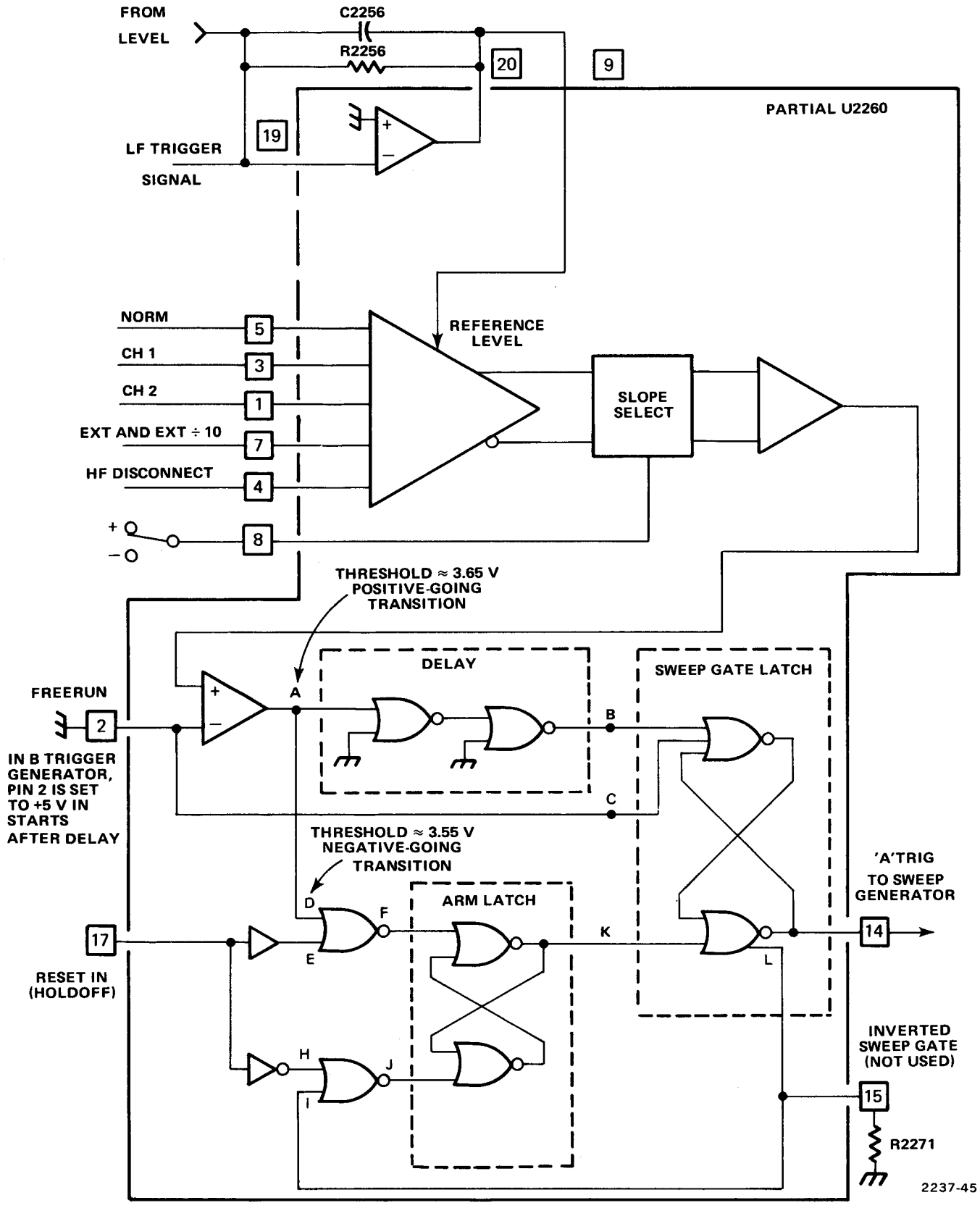


Figure 4-5. A trigger generator.

(d) Hysteresis Adjustment. The hysteresis adjustment (R2245) sets the difference in the trigger threshold and the arm threshold. The closer the levels are to each other, the more susceptible the circuit will be to triggering on noise. If the levels are too far apart, the circuit will require excessive input signal amplitude to generate a sweep gate.

(e) Trigger View Pickoff. A sample of the trigger input signal is supplied to pins 10 and 11 of U2260. This paraphase signal passes through emitter followers Q2350 and Q2356 to the TRIG VIEW switch (S4380). When the TRIG VIEW switch is pushed, the signal from the Delay Line Driver is disconnected from the Delay Line and the trigger view signal is connected in its place.

(3) B Trigger Generator. The B Trigger Generator operates in the same manner as the A Trigger Generator except in the STARTS AFTER DELAY position of the HORIZ DISPLAY switch. In the STARTS AFTER DELAY mode, +5 volts is connected to pin 2 of U2160 through S2100 and S2650 (see Figure 4-5). This disconnects the trigger signal from point B, sets point D LO, and sets point C HI. At the end of holdoff, point E goes LO causing point F to go HI. This sets point K LO and, because of the HI always present on point C, causes a sweep gate to be generated.

(4) A Sweep Generator. A sweep generator consists of U2790 and associated circuitry. Diagram 5 (FO-7) shows a complete schematic diagram of the circuit. Figure 4-6 shows a simplified diagram of the circuit. Figure 4-7 shows the waveforms produced during A sweep generation.

(a) Sweep Generator Integrated Circuits. Both the A and B Sweep Generator integrated circuits (U2790 and U2690 respectively) are the same. However, the functions of some of the pins are different. The following lists the pin numbers and their functions:

1 Pin 1 is the input for the DELAY TIME POS control. This pin is only used in the A Sweep Generator. When the A ramp on pin 2 is equal to the voltage on pin 1, a delayed gate is produced at pin 16.

2 Pin 2 is the input for the ramp voltage from the output Miller circuit. This voltage is internally connected to pin 5 when pin 7 is LO.

3 Pin 3 sets internal current levels.

4 Pin 4 sets the Miller null and retrace currents for the A Sweep Generator only. This function is performed by another circuit in the B Sweep Generator.

5 Pin 5 is the sweep ramp output. The ramp at pin 5 is connected to the Horizontal Preamplifier. Pin 5 is switched on or off by the voltage on pin 7.

6 Pin 6 sets the internal current levels which, along with R2682 or R2782, determine the sweep start voltage.

7 Pin 7 controls the sweep ramp output at pin 5. When pin 7 is LO the sweep ramp at pin 2 is internally connected to pin 5. When pin 7 is HI, the sweep ramp at pin 2 is disconnected from pin 5 and pin 5 is set to −5 volts.

8 Pin 8 is the connection for the −5 volt supply.

9 Pin 9 is the ground connection.

10 In the A sweep Generator, pin 10 produces an output which initiates holdoff. In the B Sweep Generator, pin 10 produces an output which is supplied to the +B GATE OUT Amplifier in the Main Module.

11 The voltage connected to pin 11 sets the amplitude of the unblanking signal at pin 12.

12 The signal at pin 12 is supplied to the Z Axis Amplifier in the Main Module to unblank the crt. The amplitude of this signal, and therefore the brightness of the crt display, is controlled by the voltage on pin 11.

13 Pins 13 and 14 work together. A HI on either pin prevents sweep generation. Both must be LO to start sweep generation. In the A Sweep Generator, pin 13 is held LO through a resistor to ground and only pin 14 controls sweep generation. In the B Sweep Generator pin 14 goes LO when the A Sweep Generator starts but pin 13 doesn't go LO until the B Trigger Generator produces a sweep gate. In the STARTS AFTER DELAY position of the B SOURCE switch, a B sweep gate is produced as soon as pin 16 of U2790 produces a delayed gate. In other settings, a B sweep gate is produced when the first adequate trigger signal occurs after a delayed gate is produced at pin 16 of U2790.

14 Pin 14 works with pin 13. See the pin 13 discussion.

15 Pin 15 is the connection for the +5 volt supply.

16 Pin 16 of the A Sweep Generator produces a delayed gate to remove the holdoff condition from the B Trigger Generator. This output is produced when the A ramp voltage on pin 2 reaches the dc level on pin 1.

(b) Sequence of Events During A Sweep Generation.

1 **Quiescent Condition.** The quiescent condition exists during holdoff and after holdoff but before the A Trigger Generator produces a sweep start gate. Pin 14 of U2790 is HI. This sets point A (see Figure 4-6) HI. This causes the output of the sweep start comparator to appear as a low-impedance point. The output of the sweep start comparator supplies current through pin 4 of U2790, and through R_t, to set the inverting input of the Miller op amp to the same voltage as the non-inverting input (the sweep

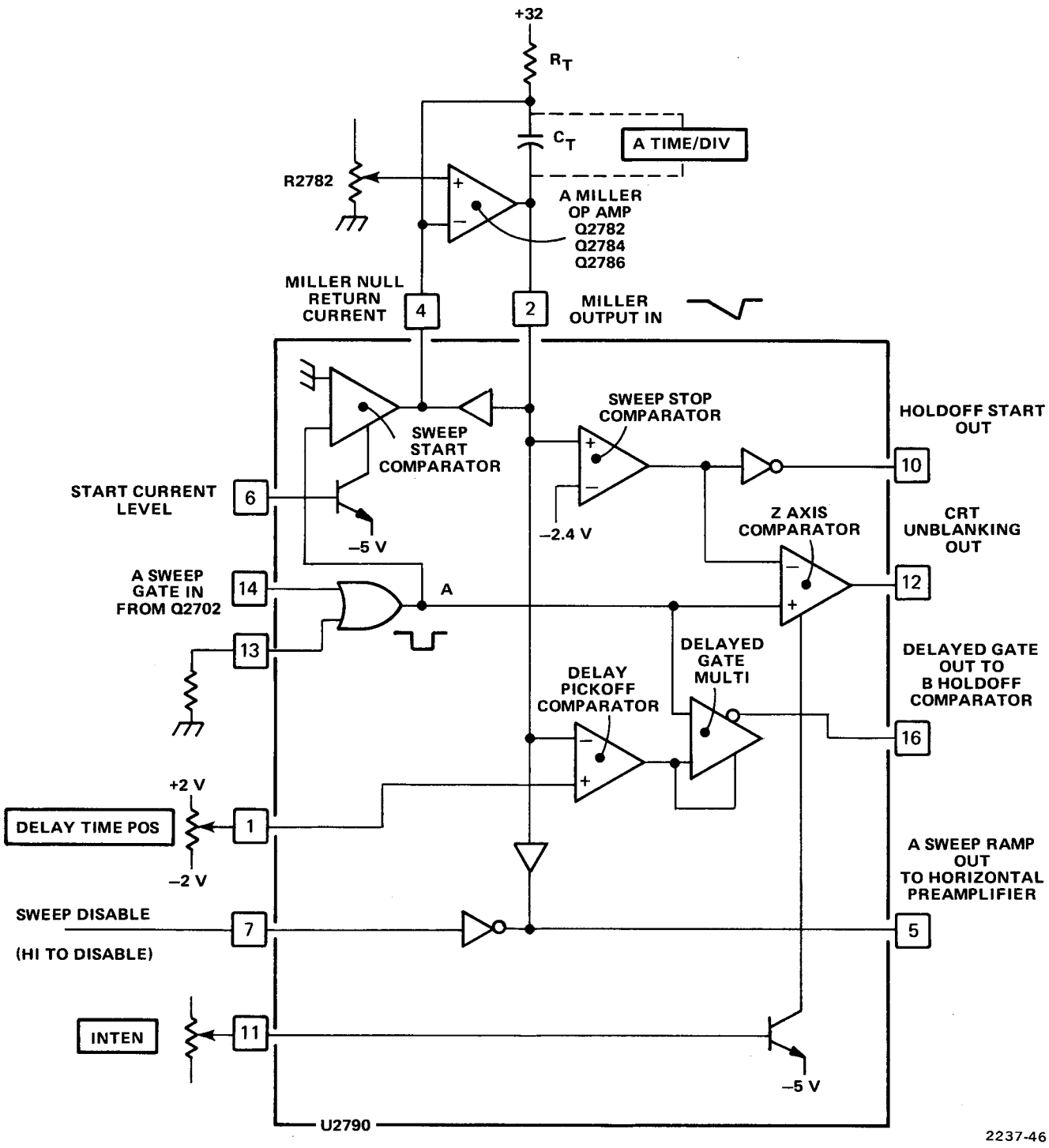


Figure 4-6. Simplified diagram of the A sweep generator.

start voltage which is set by R2782). The output of the Miller op amp sets pin 2 of U2790 to the sweep start voltage also.

2 At Triggering. Pin 13 is always LO, except in the X-Y mode. When pin 13 is HI, point A (see Figure 4-6) is HI regardless of the state of pin 14. When the sweep gate causes pin 14 to go LO, point A steps LO (see Figure 4-6). This causes the output of the sweep start comparator to become a high-impedance point. The timing capacitor (C_t) starts charging through the timing resistor (R_t).

3 During Ramp Generation. As C_t starts charging through R_t, the inverting input of the Miller op amp tries to go more positive. This causes the output of the Miller op amp to go less positive which supplies current through C_t and R_t to hold the voltage on the inverting input constant. Since the resulting voltage across R_t is constant, the current through R_t and C_t must also be constant. Charging C_t with this constant current produces a linear negative-going voltage ramp at pin 2 of U2790. The slope of the ramp is determined by the values of R_t and C_t which are selected by the A TIME/DIV switch (S3100). The ramp at pin 2 is internally connected to pin 5 of U2790 whenever pin 7 is LO. Pin 7 is HI in the MIXED and B DLY'D positions of the HORIZ DISPLAY switch and LO in the A and A INTEN positions of the HORIZ DISPLAY switch and in the X-Y mode.

4 At Delayed Gate Generaton. The negative-going ramp at pin 2 of U2790 is internally connected to a comparator. The ramp is compared to the dc voltage on pin 1 of U2790 (set by the DELAY TIME POS control). When the ramp voltage is the same as the voltage on pin 1, the comparator triggers the delayed gate multivibrator supplying a negative-going gate pulse to pin 16 of U2790. This gate is connected to the B holdoff comparator (Q2672 and Q2674) and terminates B holdoff. The negative-going gate from pin 16 of U2790 is also connected to the base of Q2622 through CR2608, CR2617, CR2618, and CR2622. This allows the B sweep gate, from the B trigger amplifier (Q2602 and Q2604), to start B sweep generation. Both signals must be LO at the same time to start B sweep.

5 Sweep End. The ramp on pin 2 of U2790 is internally connected to the sweep stop comparator. When the ramp reaches −2.4 volts, the comparator switches supplying a positive-going pulse to pin 10 of U2790. This pulse is supplied to the Sweep Control circuit and initiates A holdoff. At the beginning of holdoff, the sweep gate causes pin 14 of U2790 to step HI causing pin 4 to again appear as a low-impedance point. The current through R_t is now supplied by pin 4 of U2790. Also, when pin 14 of U2790 steps HI, it causes pin 12 to step HI and initiate B holdoff.

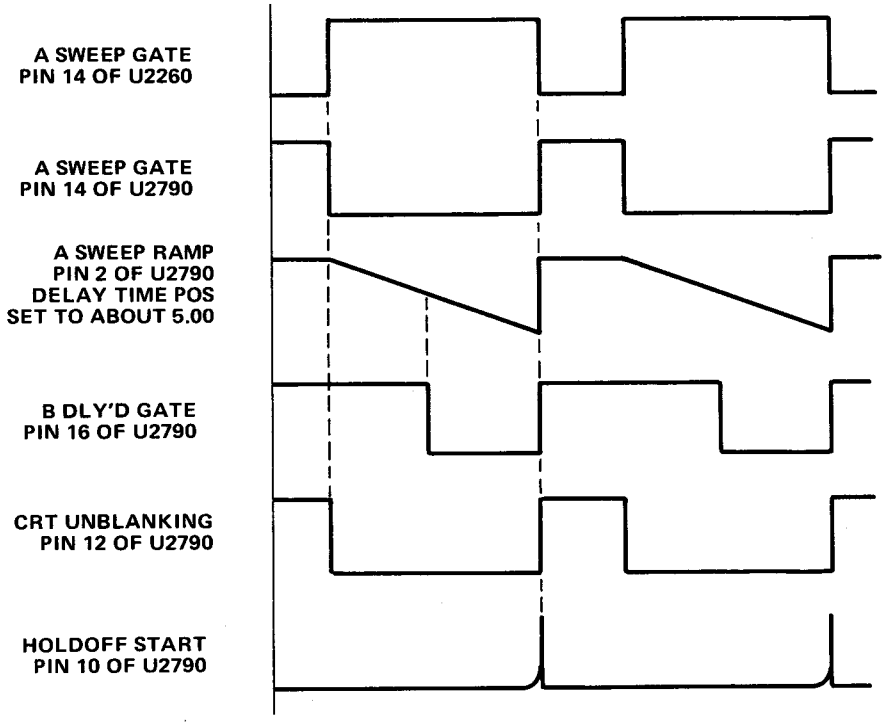


Figure 4-7. Waveforms produced during A sweep operation.

6 Retrace. At the beginning of holdoff, the output of the Miller op amp and pin 2 of U2790 are at about −2.4 volts. This voltage is supplied to the input of a non-inverting amplifier within U2790. This amplifier tries to pull pin 4 of U2780, and the inverting input of the Miller op amp, less positive. To compensate, the output of the Miller op amp rapidly goes positive discharging C_t. The resulting positive-going ramp provides retrace.

(5) B Sweep Generator. The B Sweep Generator consists of U2690 and associated circuitry. The B Sweep Generator integrated circuit (U2690) is the same as the A Sweep Generator integrated circuit (U2790). Both are discussed in paragraph 4-3. b. (4) (a). Figure 4-8 shows a simplified diagram of the B Sweep Generator. Figure 4-9 shows the waveforms produced during B sweep generation. Figure FO-6 shows a complete schematic diagram of the B Sweep Generator.

(a) Sequence of Events During B Sweep Generation in B DLY'D or A INTEN Mode. Refer to Figure 4-8 and Figure 4-9 during the following discussion. Diagram 5 (FO-7) shows a complete schematic diagram of the B Sweep Generator.

1 Before B Delayed Gate Generation. In the B DLY'D or A INTEN modes, the base of Q6236 is set to about +2 volts through the HORIZ DISPLAY switch (S2650). The following conditions exist before the generation of a B delayed gate at pin 16 of U2790. The B trigger amplifier (Q2602 and Q2604) supplies a HI to the base of Q2622 which biases off Q2622. The B sweep start voltage (about +2 volts from pin 2 of U2690) is applied to the base of Q2632. Bias resistors set the base of Q2636 to about +2 volts also. Ideally Q2632 and Q2636 Will conduct equally. The emitter of Q2624 is connected to the collector of Q2636 which forward biases Q2624. The collector of Q2624 pulls the emitter of Q2620 negative enough (through CR2621) to turn on Q2620. Transistor Q2620 supplies current through R_t to hold the inverting input of the B Miller op amp at the same voltage as its non-inverting input (set by R2682).

2 At B Delayed Gate Generation. When the A Sweep Generator generates a B delayed gate (at pin 16 of U2790), the resulting negative step on the base of Q2672, causes the B holdoff comparator (Q2672 and Q2674) to switch states and remove B holdoff from the B Trigger generator.

3 At B Sweep Gate Generation. When a B sweep gate is generated by the B Trigger Generator, the B trigger amplifier (Q2602 and Q2604) switches, which pulls the base of Q2622 negative. Transistor Q2622 turns on, pulling the emitter of Q2620 less negative. This turns off Q2620. This begins generation of a B ramp. When the B ramp (at pin 2 of U2690) begins going less positive, it turns off Q2636. The emitter of Q2624 is now connected to −5 volts through R2638. Transistor Q2624 remains on, supplying the collector current for Q2622.

4 During B Ramp Generation. When Q2620 turns off, C_t begins charging through R_t. As C_t charges, the inverting input of the B Miller op amp tries to go more positive. To compensate, the output of the B Miller op amp supplies current through C_t and R_t to hold the inverting input at the same voltage as the non-inverting input (set by R2682). Since the resulting voltage across R_t is constant, the current through R_t and C_t is constant. Charging C_t with this constant current produces a linear negative-going ramp at pin 2 of U2690. The slope of the ramp is determined by the values of R_t and C_t which are selected by the B TIME/DIV switch (S3200). The ramp at pin 2 of U2690 is internally connected to pin 5 whenever pin 7 is LO. Pin 7 is LO in the B DLY'D mode and HI in the A INTEN mode. The B Sweep Generator does not provide horizontal deflection in the A INTEN mode, it only supplies additional unblanking current to intensify the display during the time a B sweep ramp is being generated.

5 Sweep Stop. When the ramp at pin 2 of U2690 reaches about −2.4 volts, the emitter of Q2629 becomes sufficiently negative to forward bias Q2629. When Q2629 turns on its collector becomes sufficiently negative to turn on Q2620. The resulting current through Q2620 flows through R_t and holds the inverting input of the B Miller op amp at the same voltage as the non-inverting input. The B Miller op amp no longer supplies current to C_t and the voltage on pin 2 of U2690 remains at about −2.4 volts. The B Sweep Generator does not reset at this time. If it did reset, it might be possible to trigger and generate another B sweep ramp before A sweep ends. This would produce an erroneous display. The gate at pin 10 of U2690 does not initiate B holdoff, it only supplies a signal to the +B GATE OUT Amplifier in the Main Module.

6 Retrace. At the end of a sweep, the holdoff gate from the Sweep Control circuit resets both the A and B Trigger Generators. When the B Trigger Generator resets, the B trigger amplifier (Q2602 and Q2604) switches and pulls the base of Q2622 HI. This turns off Q2622. When Q2622 turns off, it allows the collector of Q2629 to pull the emitter of Q2620 more negative which increases the forward bias on Q2620. The increased forward bias on Q2620 tries to increase the current through R_t and force the inverting input of the B Miller op amp less positive. To compensate, the output of the B Miller op amp rapidly goes positive, discharging C_t. The resulting positive-going ramp on pin 2 of U2690 provides retrace.

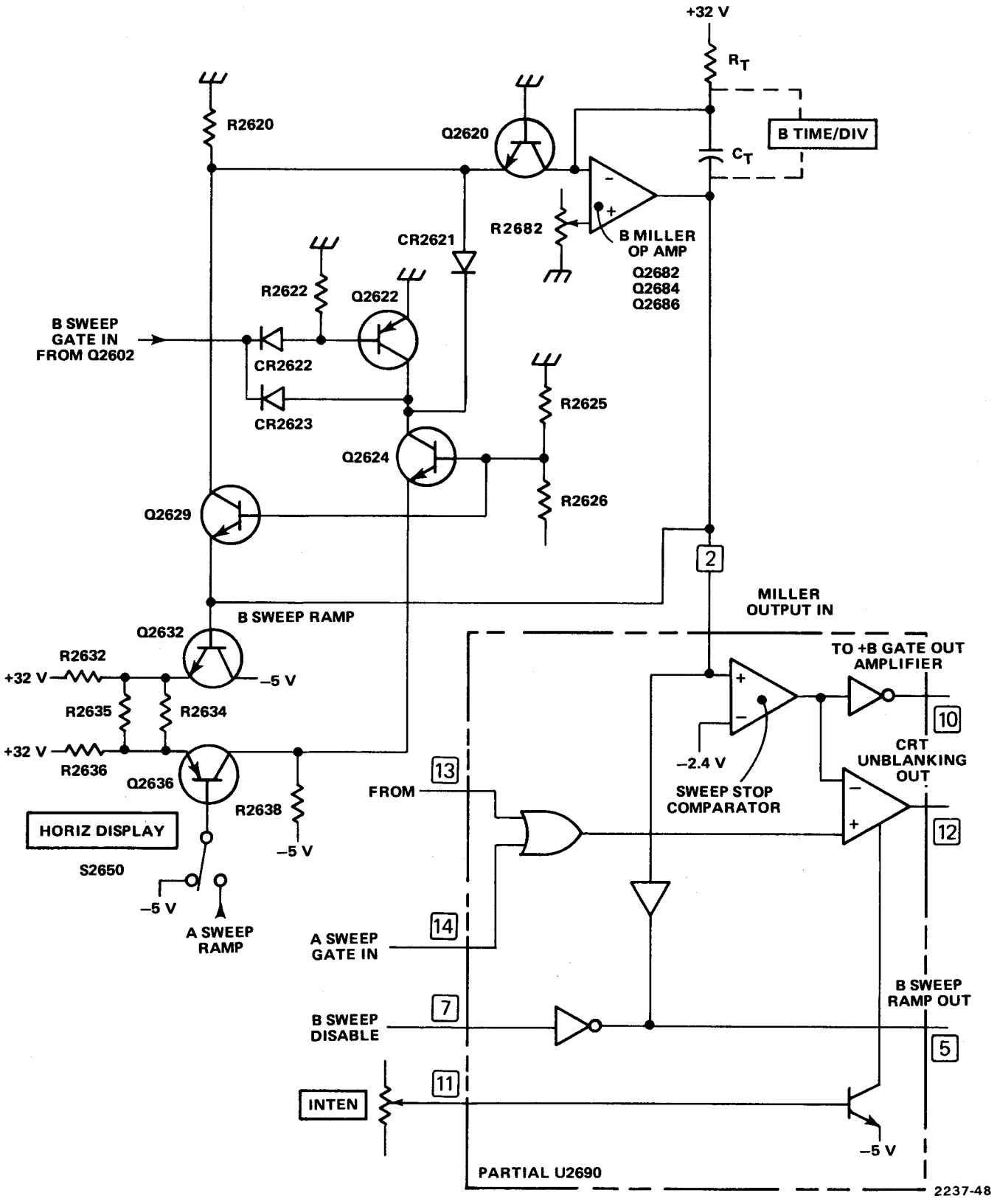


Figure 4-8. Simplified diagram of the B sweep generator.

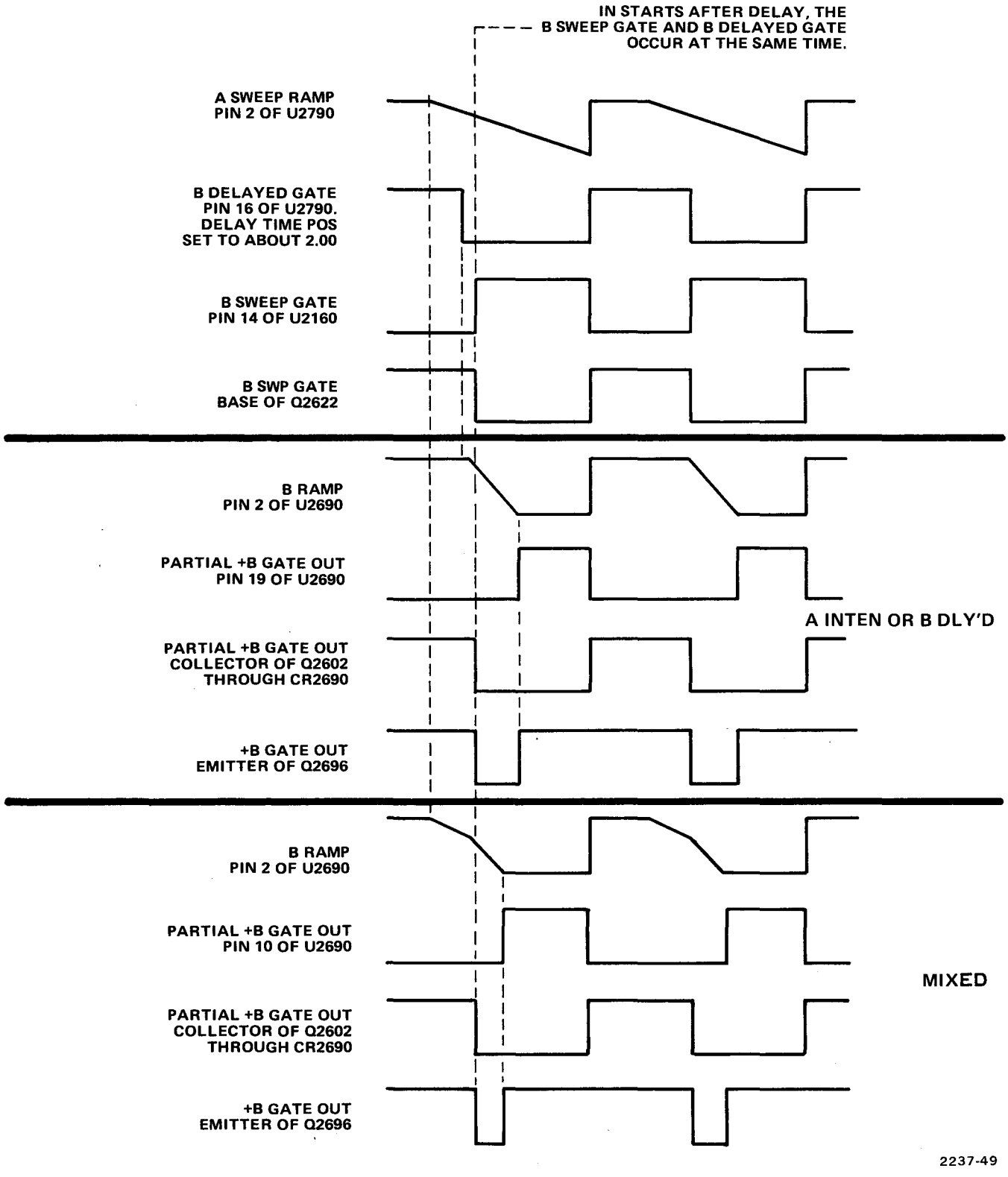


Figure 4-9. Waveforms produced during B sweep generation

7 End of Retrace. When the retrace ramp on pin 2 of U2690 reaches about +2 volts, the emitter of Q2636 (through the emitter of Q2632) is pulled sufficiently positive to forward bias Q2636. At the same time, the emitter of Q2629 becomes sufficiently positive to turn off Q2629. The initial condition (before B delayed gate generation) is restored. The collector of Q2636 goes less negative, decreasing the forward bias on Q2624. Now Q2624 supplies just enough current through Q2620 and R_t to hold the inverting and non-inverting inputs of the B Miller op amp at the same voltage.

(b) Sequence of Events During B Sweep Generation in MIXED Mode. In the MIXED mode, B sweep generation is similar to that in the A INTEN or B DLY'D modes. The main difference is that the voltage level on pin 2 of U2690 is controlled by the A sweep ramp before a B sweep gate is generated. Also, a HI is placed on pin 7 of U2790 causing pin 5 of U2790 to go LO and disconnect the A ramp from the Horizontal Preamplifier.

1 Before A Sweep Starts. When the MIXED button is pushed, the A sweep ramp is connected to the base of Q2636 through R2637 and R2781. Ideally the A and B sweep start voltages will be about the same, causing both Q2636 and Q2632 to conduct. The collector of Q2636 is connected to the emitter of Q2624, forward biasing Q2624. The collector of Q2624 pulls the emitter of Q2620 negative enough to forward bias Q2620. Transistor Q2620 supplies current through R_t to hold both inputs of the B Miller op amp at the same voltage. Also, a HI from the B trigger amplifier (Q2602 and Q2604) holds off Q2622.

2 After A Sweep Starts. When the A Sweep Generator is triggered, the negative-going A sweep ramp begins to appear at pin 2 of U2790 which is connected to the base of Q2636. As the base of Q2636 goes less positive, Q2636 turns on harder causing its collector to go less negative. The collector of Q2636 is connected to the emitter of Q2624. As the collector of Q2636 goes less negative, the forward bias on Q2624 is decreased, which decreases its collector current. Since Q2624 supplies the current through Q2620, the current through Q2620 also decreases. This causes the inverting input of the B Miller op amp to try to go more positive. To compensate, the output of the B Miller op amp supplies current through C_t and R_t to hold both inputs at the same voltage. C_t charges at a rate determined by the A sweep ramp. The resulting ramp at pin 2 of U2690 has the same slope as the A sweep ramp and is internally connected to pin 5 of U2690. This signal is connected to the Horizotal Preamplifier and provides horizontal deflection for both the A and B portions of the display.

3 When B Sweep Gate is Generated. When a B sweep gate is generated by the B Trigger Generator, the base of Q2622 steps negative, turning on Q2622 which turns off Q2620. B sweep generation continues as in the A INTEN or B DLY'D modes. See 4-3. b. (5) (a) 3 through 7.

(6) Horizontal Preamplifier.

(a) The Horizontal Preamplfier is contained within a single integrated circuit (U2900). The Horizontal Preamplifier amplifies the sweep ramp outputs from the A and B Sweep Generators and supplies the amplified signal to the Horizontal Amplifier in the Main Module. In the X-Y mode, the CH 1 Preamplifier output is supplied to the Horizontal Peramplifier to provide horizontal (X axis) deflection.

(b) The following lists the pin numbers of U2900 and their functions.

1 Pin 1, Magnifier Registration. Used in conjunction with pin 8 to adjust magnifier registration. Adjustment is correct when display does not shift horizontally when switching between normal and magnified displays.

2 Pin 2, Sweep. Output for the negative-going signal which is supplied to the Horizontal Amplifier in the Main Module.

3 Pin 3, Gain. Used in conjunction with pin 6. The resistance between pins 3 and 6 determines the amplitude of the signal at pins 2 and 7. Decreasing this resistance increases gain. The X10 Magnifier switch, when pushed, decreases this resistance by a factor of ten and therefore increases the gain by a factor of ten.

4 Pin 4, –5 Volts. Connection for the –5 volt supply.

5 Pin 5, Current Source. Sets current levels within U2900.

6 Pin 6, Gain. See pin 3.

7 Pin 7, +Sweep. Output for positive-going signal which is supplied to the Horizontal Amplifier in the Main Module.

8 Pin 8, Magnifier Registration. See pin 1.

9 Pin 9, B Sweep Input. The output of the B Sweep Generator is connected here. The more positive of the levels connected to pins 9 and 10 is internally connected to the amplifier and provides the output at pins 2 and 7. The more negative level on pins 9 and 10 is ignored.

10 Pin 10, A Sweep Input. The output of the A Sweep Generator is connected here. See pin 9.

11 **Pin 11, X Signal Input.** A sample of the signal present in the CH 1 Preamplifier is connected here. When pin 12 is HI, the sweep inputs from pins 9 and 10 are internally disconnected and the signal from pin 11 is amplified and connected to the outputs on pins 2 and 7.

12 **Pin 12, X-Y Control.** This pin is set HI only in the X-Y mode. See pin 11.

13 **Pin 13, Frequency Compensation.** The frequency compensating capacitor is connected here.

14 **Pin 14, Horizontal Position.** The horizontal POSITION control is connected here. Changing the dc voltage on this pin shifts the dc level of the outputs at pins 2 and 7, except in the X-Y mode.

(7) +A GATE OUT Amplifier. The +A GATE OUT Amplifier consists of Q2712 and associated circuitry. The A sweep gate signal from the collector of Q2702 (part of the A trigger amplifier) is connected to the base of Q2712. At the beginning of A sweep the sweep gate turns off Q2712, causing its collector to go to +5 volts. At the end of A sweep the sweep gate steps positive, turning on Q2712. The collector of Q2712 goes to about 0 volts. The resultant +A GATE OUT signal is about +5 volts while an A sweep ramp is being generated and about 0 volts the rest of the time.

(8) +B GATE OUT Buffer. The +B GATE OUT Buffer consists of Q2696 and associated circuitry. The input to the buffer circuit is obtained from three sources; the partial B Gate signal from pin 10 of U2690, the B sweep gate from the collector of Q2602 which is part of the B trigger amplifier, and the delayed gate signal from pin 16 of U2790. Figure 4-9 shows the time relationship of the two signals. The output of the Buffer is LO only when both input signals are LO. All three input signals are LO at the same time only while a B ramp is being generated. The output of the Buffer is supplied to the +B GATE OUT Amplifier in the Main Module.

(9) Sweep Control. Sweep Control consists of U2750 and associated circuitry. The circuit controls holdoff duration, AUTO sweep, and single sweep operation. Figure 4-10 shows a functional block diagram of U2750 and associated circuitry.

(a) Holdoff Control. Holdoff control is provided by a Miller ramp generator which consists of three transistors within U2750, and an RC network. Resistors R2776 and R2777 are the timing resistors. Capacitor C2762 and a capacitor selected by the A TIME/DIV switch are the timing capacitors. Figure 4-10 shows a functional block diagram of U2750 and associated circuitry. Figure 4-11 shows the waveforms produced by the holdoff control circuitry.

1 At the beginning of A sweep generation, pin 6 of U2750 steps LO. This LO passes through an inverting amplifier and turns on transistor C and turns off transistors D and E (see Figure 4-10). When transistors D and E turn off, pin 11 of U2750 is pulled more positive through R2762. Pin 11 is clamped at about +5.7 volts by a diode within U2750. The current through the timing resistors (R2776 and R2777) is supplied by transistor C through pin 10 of U2750. This condition is maintained until the end of A sweep generation.

2 At the end of A sweep generation, pin 12 of U2750 momentarily steps HI which sets the holdoff latch within U2750. The Q output of the holdoff latch goes HI causing pin 9 of U2750 to go HI. The HI on pin 9 resets and holds off the A Trigger Generator.

3 When the A Trigger Generator resets (or the AUTO sweep gate steps HI), pin 6 of U2750 steps HI. This turns off transistor C and turns on transistors D and E within U2750. Pin 10 is pulled positive to about +1.4 volts through R2776 and R2777.

4 After transistor C turns off, pin 10 tries to go more positive than +1.4 volts. This turns on transistor D harder and supplies current through C2762, R2776, and R2777. This current holds pin 10 at about +1.4 volts and begins charging C2762. As C2762 charges, pin 11 of U2750 begins going less positive.

5 As pin 11 of U2750 goes less positive, the diode selected by the A TIME/DIV becomes forward biased. Now the current to hold pin 10 at +1.4 volts is supplied through C2762 and a capacitor selected by the A TIME/DIV. Since the voltage across R2776 and R2777 doesn't change, the current doesn't change. Now this current must charge two capacitors, and the voltage ramp on pin 11 of U2750 will not be as steep. The ramp can also be made less steep by increasing the resistance of the A TRIGGER HOLDOFF control (R2777).

6 When the voltage on pin 11 falls to about 1 volt, the R input of the holdoff latch within U2750 is set HI through an inverting amplifier. The holdoff latch resets and its Q output goes LO. When the Q output goes LO, pin 9 of U2750 goes LO and terminates holdoff.

(b) AUTO Sweep Control. When pin 4 of U2750 is set LO by the TRIG MODE switch, Sweep Control provides a baseline trace in the absence of an adequate trigger signal. Figure 4-10 shows the Sweep Control integrated circuit and associated circuitry. Figure 4-12 shows the waveforms produced during AUTO sweep gate generation.

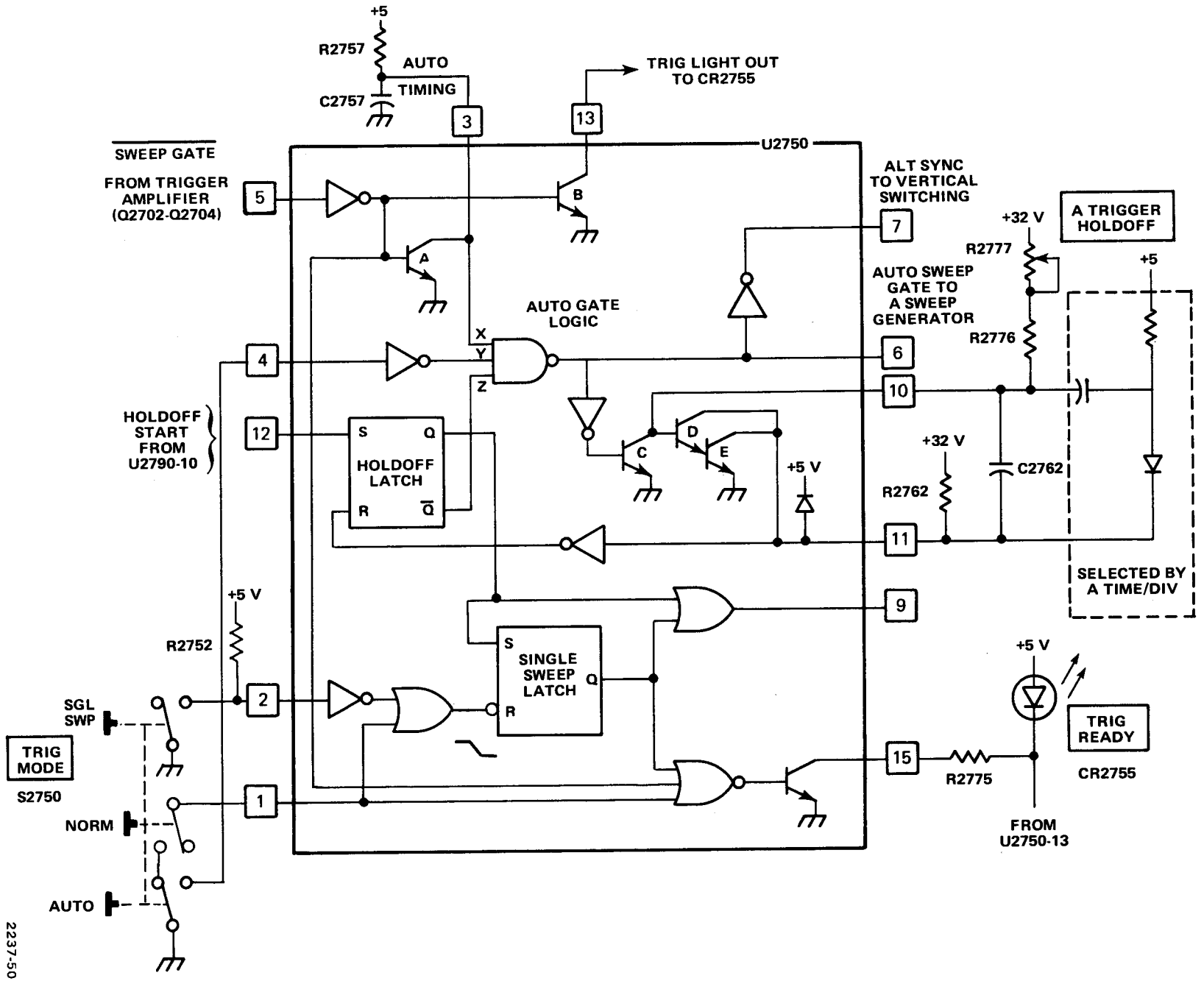


Figure 4-10. Functional block diagram of the sweep control integrated circuit and associated circuitry.

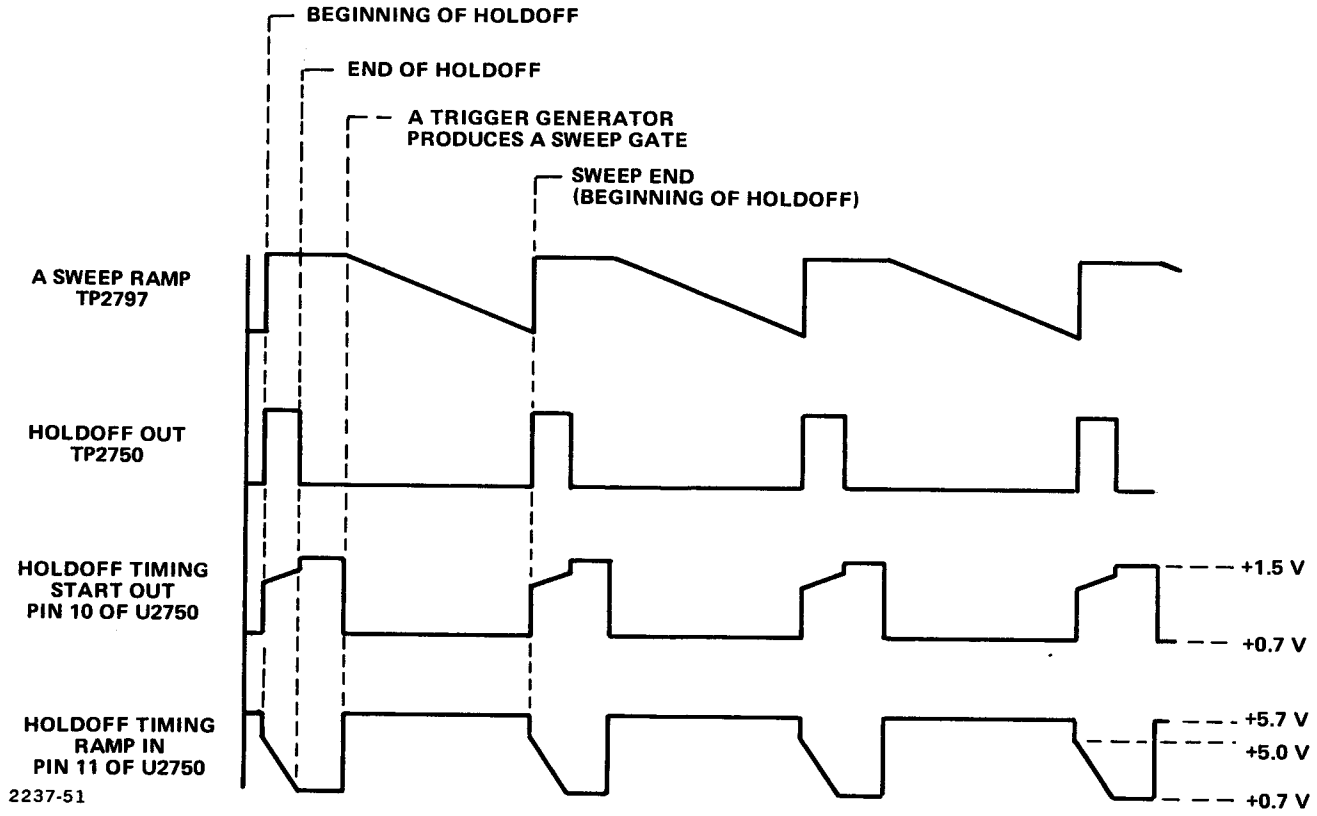


Figure 4-11. Waveforms produced by holdoff control circuitry.

1 When the TRIG MODE switch (S2750) is set to AUTO, pin 4 of U2750 is set LO. This sets input Y of the AUTO gate logic HI through an inverting amplifier within U2750 (see Figure 4-10).

2 If adequately triggered, pin 5 of U2750 steps LO at the beginning of A sweep generation. This turns on transistor A within U2750 and discharges C2757. Discharging C2757 prevents generation of an AUTO sweep gate by keeping input X of the AUTO gate logic LO.

3 Assume that the trigger signal becomes inadequate to cause the A Trigger Generator to generate an A sweep gate. At the end of the last triggered sweep, pin 12 of U2750 momentarily steps HI. This sets the holdoff latch within U2750. The $\overline{Q}$ output of the holdoff latch sets input Z of the AUTO gate logic HI.

4 When the holdoff latch sets, pin 9 of U2750 resets the A Trigger Generator causing pin 5 of U2750 to step HI. The HI on pin 5 turns off transistor A within U2750. Now C2757 starts to charge through R2757.

5 When C2757 charges sufficiently, input X of U2750 is HI. Now all three inputs of the AUTO gate logic are HI which causes an AUTO sweep gate to be generated at pin 6 of U2750.

6 At the end of the first AUTO generated sweep ramp, pin 12 of U2750 momentarily steps HI, resetting the holdoff latch. The $\overline{Q}$ output of the holdoff latch goes LO, causing the output of the AUTO gate logic to step HI. At the same time, the Q output of the holdoff latch steps HI, causing holdoff to begin (pin 9 of U2750 steps HI).

7 When holdoff ends, the R input of the holdoff latch goes HI, resetting the holdoff latch. The $\overline{Q}$ output goes HI, causing the AUTO gate at pin 6 of U2750 to step LO. This causes another AUTO sweep to be generated. As long as no adequate trigger signal is available, all subsequent sweeps will be initiated by the AUTO gate at pin 6 of U2750.

8 Assume an adequate trigger signal becomes available. When A Trigger Generator supplies an A sweep gate to pin 5 of U2750, transistor A within U2750 is turned

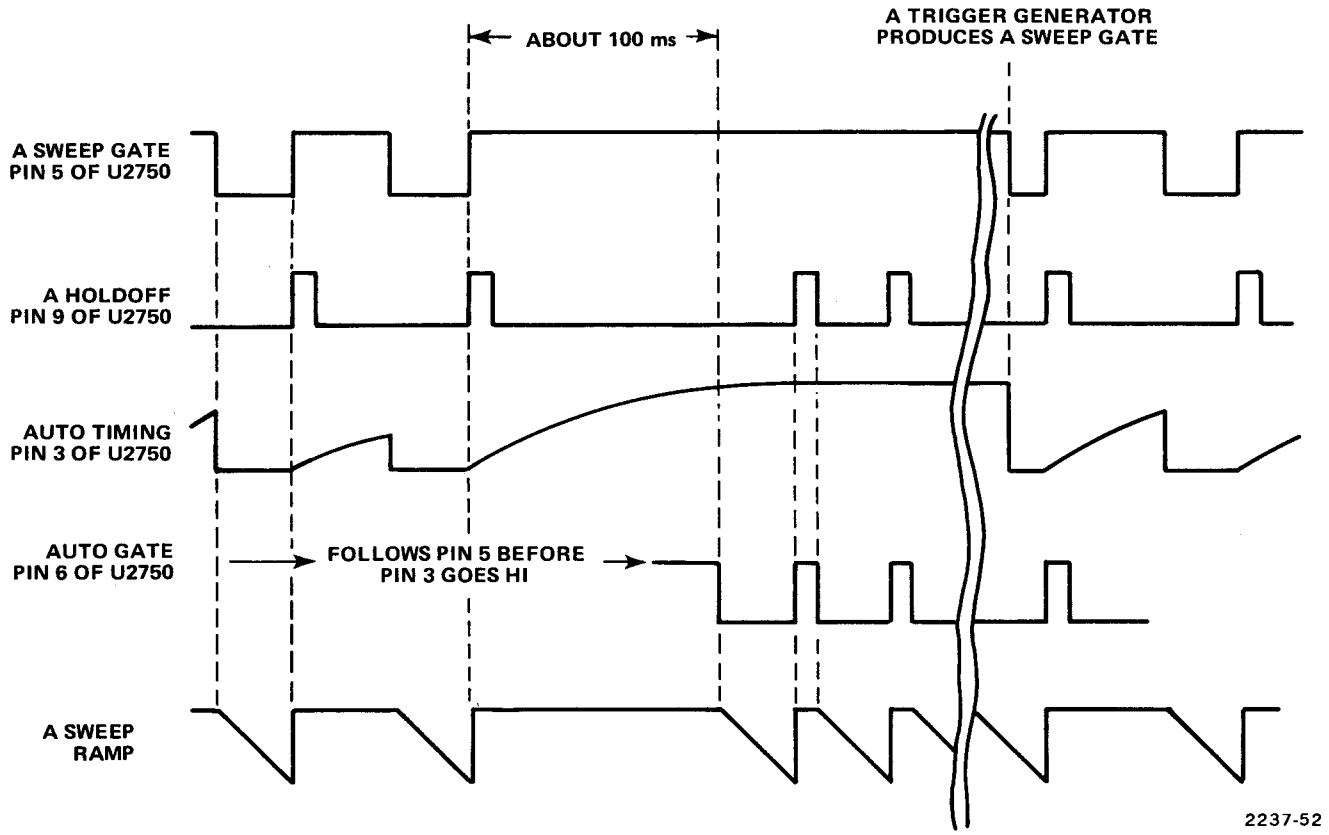


Figure 4-12 Waveforms produced during AUTO sweep gate generation.

on. Capacitor C2757 discharges rapidly through transistor A. This sets input X of the AUTO gate logic LO which disables the logic. Now another AUTO gate can not be generated at pin 6 of U2750 until C2757 charges enough to set input X of the AUTO gate logic HI (about 100 milliseconds after the beginning of holdoff).

(c) Single Sweep Control. When the TRIG MODE switch (S2750) is set to SGL SWP, pin 1 of U2750 is connected to ground. Now, when adequately triggered, only one sweep ramp will be generated. After one sweep is displayed, another sweep can't be presented until after the SGL SWP button has been pushed. Figure 4-10 shows a functional block diagram of the Sweep Control integrated circuit and associated circuitry.

1 To operate in the single sweep mode, pin 1 of U2750 is grounded and pin 2 is pulled HI through R2752. This holds the R input of the single sweep latch within U2750 HI.

2 At the end of sweep ramp generation, the Q output of the holdoff latch steps HI. This HI is connected to the S input of the single sweep latch and sets the latch. The Q output of the single sweep latch holds pin 9 of U2750 HI even after the holdoff latch has reset. This permanetly holds off the A Trigger Generator.

3 To reset the single sweep latch, the SGL SWP button must be pushed and released. When the SGL SWP button is pushed, pin 2 of U2750 is set LO which sets the R input of the single sweep latch HI. When the SGL SWP button is released, pin 2 of U2750 steps HI causing a negative going transition on the R input of the single sweep latch. This transition resets the single sweep latch. The Q output of the single sweep latch goes LO which sets pin 9 of U2750 LO and terminates holdoff.

c. Main Module.

(1) Z-Axis Amplifier. Diagram 8 (FO-10) shows the Z-Axis Amplifier circuitry. The Z-Axis Amplifier consists of Q514, Q518, Q524, Q526 and associated circuitry.

(a) Normal Z-Axis Amplifier Operation. The Z-Axis Amplifier accepts signals from several sources, amplifies them, and supplies a control signal to the CRT Circuit to control display intensity. The sources of the signals used to control display intensity are: Vertical Switching Control circuit, A Sweep Generator, and the B Sweep Generator.

1 The Z Axis Amplifier input signals are applied to the emitter of common base amplifier Q514. Transistor Q514 provides isolation between the signal sorces and the Z Axis Amplifier. The algebraic sum of the signals applied to the emitter of Q514 determines the current supplied to the base of Q518.

2 Transistor Q518 is an emitter follower. The signal on the emitter of Q518 drives Q524 and Q526.

3 Transistors Q524 and Q526 are connected as a complementary symmetry amplifier. The signal from the emitter of Q518 drives both bases and the output is taken from the junction of the two collectors. This output signal is supplied to the crt control grid through the dc restorer portion of the CRT Circuit.

(b) BEAMFINDER Z-Axis Amplifier Operation. When the BEAMFINDER button is pushed and held, the Z Axis Amplifier ignores the input signals and provides a visible display.

1 With the BEAMFINDER button pushed and held, +32 volt is disconnected from R512 and +5 volts is connected to R504.

2 The +5 volts connected to R504 reverse biases CR506 and CR505. This disconnects the input signals from the emitter of Q514.

3 When +32 volts is removed from R512, the base of Q518 is pulled slightly more negative through R514. This sets conduction in Q518 at a level which provides a visible display regardless of the Z Axis Amplifier input signals.

(2) Crt Circuit. Diagram 8 (FO-10) shows the CRT Circuit. The CRT Circuit provides the high voltage levels needed to operate the crt. The CRT Circuit consists of the high voltage oscillator, high voltage regulator, high voltage rectifier, high voltage multiplier, and dc restorer.

(a) High Voltage Oscillator. The high voltage oscillator consists of Q552, Q556, T550 and associated circuitry. Figure 4-13 shows the waveforms produced in the high voltage oscillator.

1 To explain the high voltage oscillator, we must choose a given point in an oscillation and describe the sequence of events. Assume pin 3 of T550 is going more positive and pin 5 is going less positive.

2 As pin 3 of T550 goes more positive, the voltage across the feedback winding of T550 (between pins 3 and 6) adds to the voltage on C548. When the voltage on pin 3 becomes sufficiently positive, it pulls the base of Q552 positive enough to turn on Q552.

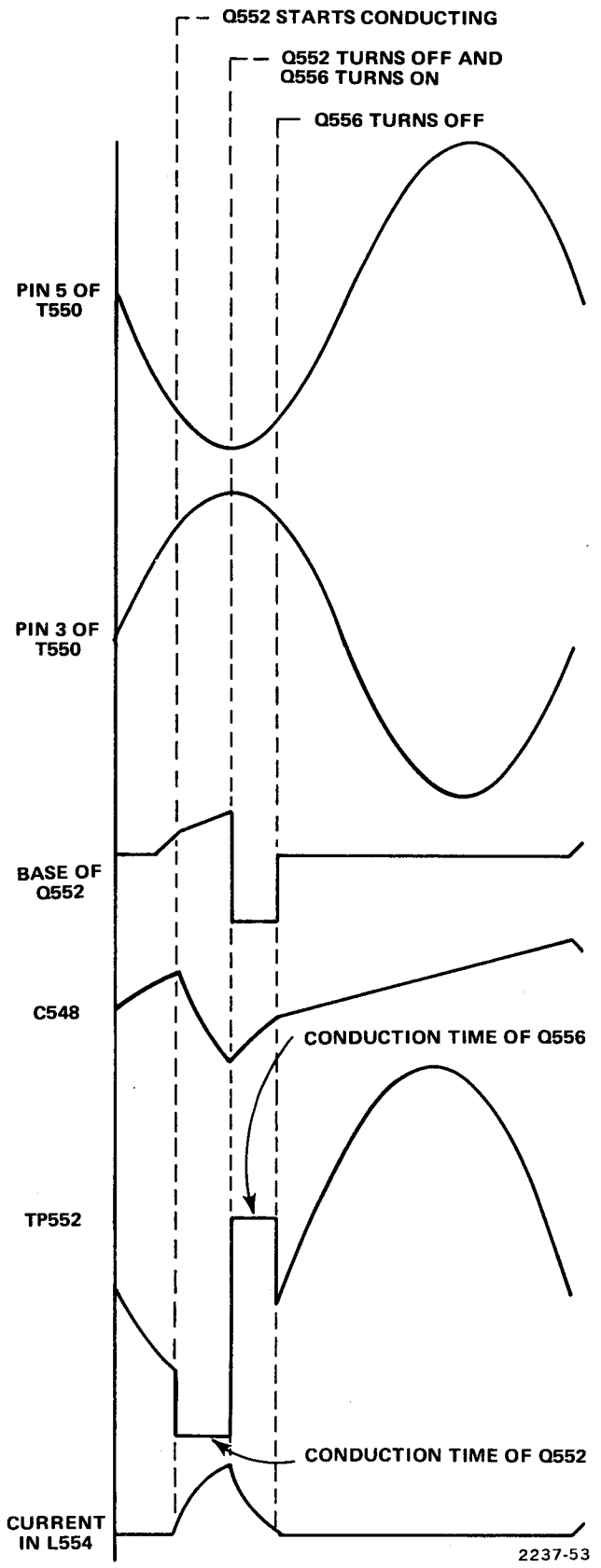


Figure 4-13. Waveforms produced in the high voltage oscillator

3 As Q552 turns on, current is drawn through T550 and L554. This current induces positive feedback into the feedback coil of L554 and turns on Q552 harder. The voltages induced into the feedback coils of T550 and L554 hold Q552 on.

4 As the magnitude of the current in T550 and L554 increases, the rate of change of the current decreases. When the rate of change of the current reaches about zero, the voltage induced in the feedback windings of T550 and L554 becomes insufficient to hold Q552 on. Q552 begins to turn off. Note that at this instant the voltage across the secondary of L554 is 0 volts.

5 As Q552 is turning off, the magnetic field around L554 starts collapsing. This induces a voltage in the feedback winding of L554 which speeds up the turnoff of Q552.

6 The collapsing magnetic field of L554 induces a voltage in L554 which forces the emitter of Q556 more positive. This voltage causes the emitter of Q556 to go more positive than pin 4 of T550. As a result, Q556 turns on and places L554 in parallel with the primary winding of T550.

7 The current produced by the collapsing magnetic field of L554 flows through Q556 and the primary winding of T550. This transfers the energy stored in L554 to T550 and increases the efficiency of the circuit. The amount of energy stored in L554 is controlled by the high voltage regulator.

8 As the oscillation cycle continues, the voltage across L554 decreases until it is not sufficient to hold Q556 on. Therefore Q556 turns off.

9 The cycle continues until pin 3 of T550 again becomes sufficiently positive to turn on Q552. Then the sequence just described repeats.

(b) High Voltage Regulator. The high voltage regulator consists of Q544, Q548, and associated circuitry. Diagram 8 (FO-10) shows the high voltage regulator circuitry. The high voltage regulator controls the output of the high voltage oscillator by controlling the energy in the primary circuit. To fully understand the high voltage regulator, read the previous High Voltage Oscillator discussion before continuing with this discussion.

1 The high voltage regulator controls the point during an oscillation cycle that Q552 is turned on. Assume the −2 kV supply starts to go more negative (too much energy is transferred to the secondary circuit of T550).

2 As the −2 kV supply goes more negative it pulls the base of Q554 less positive. The collector of Q544 goes more positive which decreases the collector current of Q548. Transistor Q548 supplies charge current to C548. Because the collector current of Q548 is decreased, C548 charges more slowly. As a result, the voltage on pin 3 of T550 will not become positive enough to turn on Q552 until later in the oscillation cycle (see Figure 4-13). Therefore less energy is stored in L554 and transferred to the primary of T550 when Q556 turns on. This decreases the amount of energy transferred to the secondary of T550 which causes the −2 kV supply to go less negative.

3 If the −2 kV supply goes less negative, Q544 and Q548 turn on harder charging C548 faster. The voltage on pin 3 of T550 becomes positive enough to turn on Q552 earlier in the oscillation cycle. Therefore more energy is stored in L554 and transferred to the primary of T550 when Q556 turns on. As a result, more energy is transferred to the secondary circuit of T550 and the −2 kV supply goes more negative.

4 In the event the high voltage regulator malfunctions, VR552, VR553, and CR552 provide overvoltage protection. If the peak voltage on pin 8 of T550 exceeds about +200 volts, VR552 conducts. When VR552 and VR553 conduct they turn on Q552 which draws enough current to open fuse F558.

(c) High Voltage Rectifier. Figure 4-14 shows a simplified diagram of the high voltage rectifier. Diagram 8 (FO-10) shows the high voltage rectifier and associated circuitry.

1 The high voltage rectifier is contained within U550. The circuit half wave rectifies the −2 kV peak ac signal at pin 9 of T550. The rectified and filtered voltage is supplied to the crt cathode, dc restorer, FOCUS control, and the high voltage regulator.

2 The heater supply winding of T550 is referenced to the −2 kV supply. This prevents breakdown between the heater and the cathode due to a large voltage difference between them.

(d) High Voltage Multiplier. Diagram 8 (FO-10) shows the high voltage multiplier. The circuit is a standard voltage multiplier consisting of diodes and capacitors. The multiplication factor is 3. The multiplier is contained within module U550. The output of the multiplier supplies the positive anode voltage for the crt.

(e) DC Restorer. The dc restorer is contained within U550. Figure 4-15 shows a simplified diagram of the circuit.

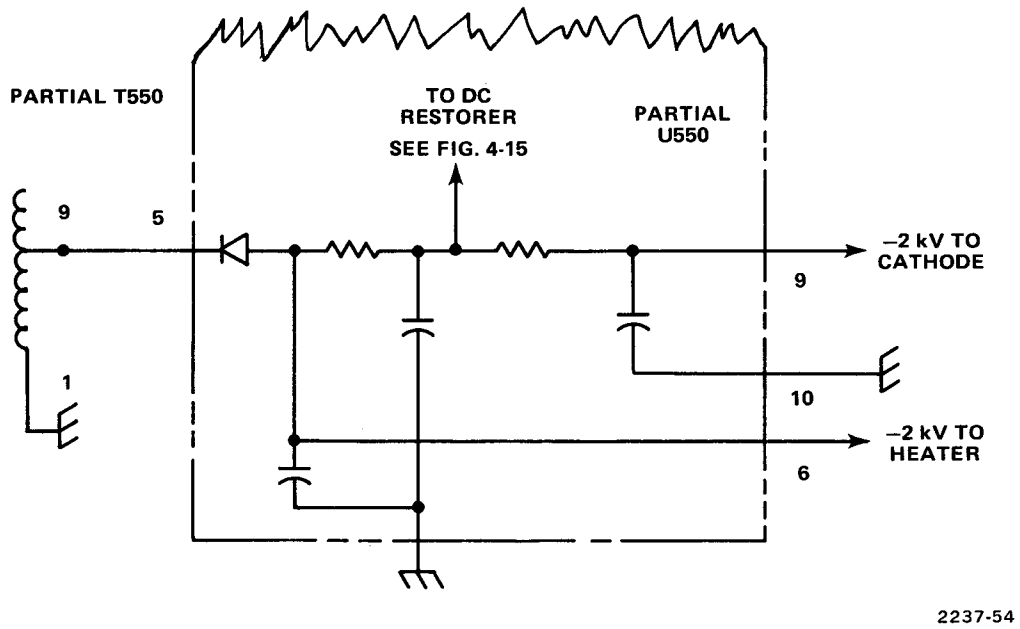


Figure 4-14. High voltage rectifier.

1 To control the crt beam current, and therefore display intensity, the voltage on the crt control grid is varied through the dc restorer. How negative the control grid is with respect to the cathode is determined by the difference in the voltages from the crt bias setting and the Z Axis Amplifier.

2 The voltages from the bias control and the Z Axis Amplifier will vary; however, to make this discussion easier to understand, assume the bias control sets pin 2 of U550 to +100 volts and the Z Axis Amplifier sets pin 1 of U550 to +20 volts.

3 On positive-going excursions of the voltage on pin 8 of T550, diode C clamps the voltage at point X to about the voltage on pin 2 of U550 (see Figure 4-15). We have assumed this voltage to be about 100 volts. Point Y is clamped at about −2 kV by diode G. Capacitor E charges to the difference between the −2 kV supply and pin 2 of U550 (about 2.1 kV). Note that diode F is reverse biased. When the voltage on pin 8 of T550 falls below the level on pin 1 of U550 (set by the Z Axis Amplifier), diode B clamps point X at about the voltage on pin 2 of U550 (+20 volts assumed). Since the voltage on capacitor E can't be changed instantaneously, point Y steps negative by an amount equal to the difference in the levels at which diodes B and C conduct (80 volts assumed) Point Y steps negative to −2080 volts. This is 2100 volts (the charge on capacitor A) more negative than the conduction level of diode B.

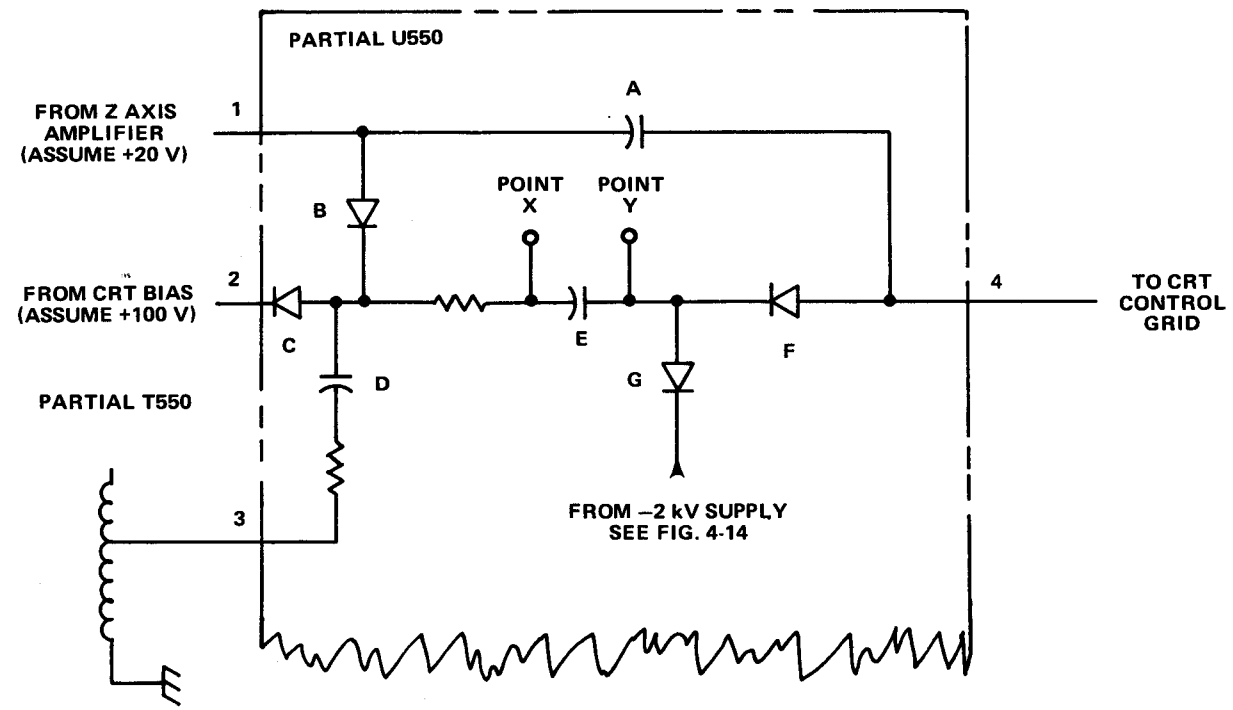
4 When point Y steps to −2080, diode G becomes reverse biased and diode F becomes forward biased. Point Y sets the crt grid to about −2080 volts or about 80 volts more negative than the cathode. While diode F is forward biased, capacitor E discharges slightly into capacitor A. This replaces the charge that leaks off capacitor A while diode F is reverse biased.

5 When the oscillation on pin 8 of T550 again becomes sufficiently positive, the original condition is restored. Diode C clamps point X at about 100 volts and diode F is reverse biased. While diode F is reverse biased, the charge on capacitor A holds the crt control grid at about −2080 volts.

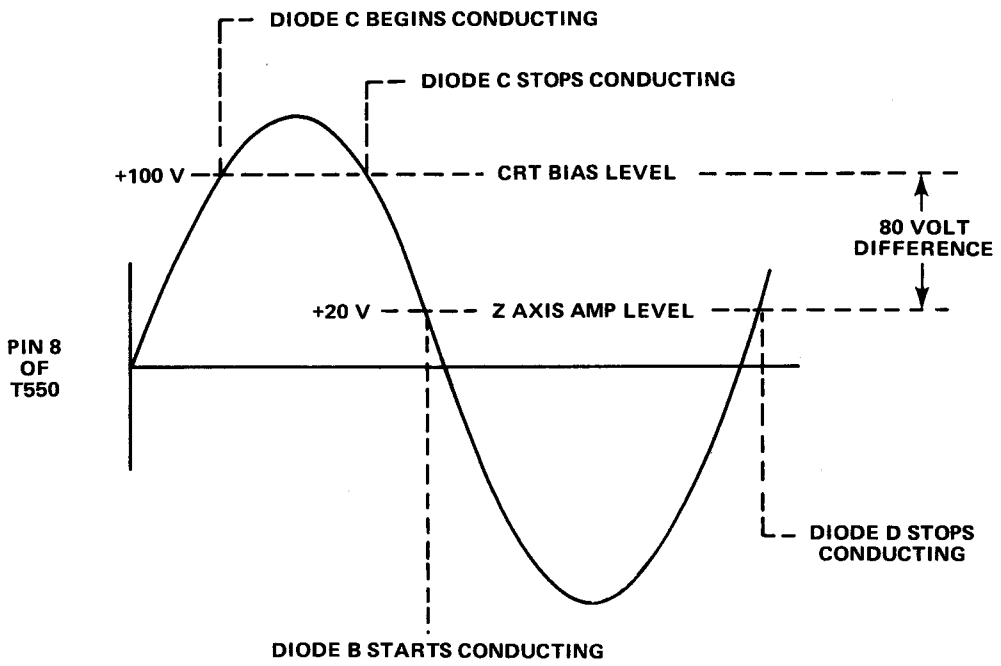
6 The action just described is fairly slow. To provide rapid intensity changes, the rapid voltage changes from the Z Axis Amplifier are supplied directly to the control grid through capacitor A.

(3) Horizontal Amplifier. Diagram 7 (FO-9) shows the Horizontal Amplifier circuitry. The Horizontal Amplifier provides the final signal amplification to drive the horizontal deflection plates of the crt. The circuit consists of two single ended feedback amplifiers. Transistor Q234 is a constant voltage source for the input stages of both amplifiers (Q232 and Q274). The collectors of Q232 and Q274 drive the bases of complementary symmetry amplifiers Q244-Q246 and Q284-Q286 respectively. The signals in the two amplifiers are 180 degrees out of phase with each other.

(4) +B GATE OUT Amplifier. Diagram 7 (FO-9) shows the +B GATE OUT Amplifier circuitry.



[A] DC RESTORER CIRCUITRY



[B] THEORETICAL DC RESTORER WAVEFORM (NOT MEASURABLE)

2237-55

Figure 4-15. Dc restorer.

(a) The +B GATE OUT Amplifier amplifies the signal from the +B GATE OUT buffer. The output of this circuit is connected to a rear panel mounted BNC connector. The output signal steps to about +5 volts during B sweep ramp generation and about 0 volts the rest of the time. The circuit consists of inverting amplifier Q356, emitter follower Q358, and associated circuitry.

(b) When the input of the circuitry goes more positive, Q356 turns on hard and its collector goes to about +0.7 volts. This causes the emitter of Q358 to go to about 0 volts.

(c) When the input steps less positive, Q356 turns off and the base of Q358 is pulled more positive through R354. The emitter of Q358 is prevented from going more positive than +5.1 volts by VR353.

(5) Calibrator. Diagram 7 (FO-9) shows the Calibrator circuitry. The Calibrator generates an accurate 1.0 volt square wave for use in probe compensation and checking vertical gain accuracy. The circuit consists of an astable multivibrator and an output amplifier.

(a) Multivibrator. Transistors Q376 and Q382 form an astable multivibrator. The multivibrator runs at approximately 1 kilohertz. The frequency is determined by the RC time constant of C376-R377-R375. Transistors Q376 and Q382 conduct alternately, producing a square wave output signal at the collector of Q382. Diodes CR372 and CR373 limit the charge on C376 to about 18 volts to prevent damage to Q376 or Q382 when either transistor is removed while the instrument is operating.

(b) Output Amplifier. The square wave output signal from the collector of Q382 drives the output amplifier (Q386). Transistor Q386 is alternately driven into saturation, then into cutoff. This results in a 0 to +5 volt square wave at the collector of Q386. Amplitude adjustment R386 sets the collector current in Q386 to produce a 1 volt square wave across R388. This 1 volt square wave is connected to J387 on the instrument front panel.

(6) Low Voltage Power Supplies. Diagram 9 (FO-11) shows the Low Voltage Power Supplies, except for the +95 volt supply. Diagram 8 (FO-10) shows the +95 volt supply.

(a) Primary Circuit. All the supplies except the +95 volt supply receive power from T700. To reduce electromagnetic interference, the ac supply voltage is filtered by a filter which is part of P700. There are two windings in the primary of T700. These windings can be placed in series or parallel by the line voltage selector switch (S701). The two windings are placed in series for operation from a 232 volt power source or in parallel for operation from a 116 volt power source.

(b) +32 Volt Supply. Diagram 9 (FO-11) shows the +32 volt supply. The +32 volt supply consists of U722A, Q732, Q734, Q736 and associated circuitry.

1 Operational amplifier U722A controls regulation of the +32 volt supply. The noninverting input of U722A is set to +9 volts by VR722. The output of the +32 volt supply sets the inverting input of U722A at +9 volts through voltage divider R735-R736-R737.

2 The output of U722A (about +9 volts) is level shifted by a zener diode (VR725). This level shifted voltage controls the base drive of Q732 and Q736 which are connected as a Darlington amplifier. Transistor Q734 provides overcurrent protection.

3 Regulation occurs as follows. Assume the +32 volt supply tries to go less positive. This is sensed on the wiper of R736 and causes the inverting input of U722A to try to go less positive. As a result, the output of U722A goes more positive which turns on Q732 and Q736 harder. When Q736 turns on harder, the +32 volt supply goes more positive which corrects for the original deviation.

(c) +5 Volt Supply. Diagram 9 (FO-11) shows the +5 volt supply. The +5 volt supply consists of U722B, Q742, Q744, Q746 and associated circuitry.

1 The reference voltage for the +5 volt supply is obtained from the +32 volt supply through R741 and R742. The reference voltage sets the noninverting input of U722B to +5 volts.

2 The inverting input of U722B senses changes in the +5 volt supply through R743.

3 The output of U722B controls conduction in Q744 and Q746 which are connected as a Darlington amplifier. The conduction level of Q746 controls the +5 volt supply output voltage. Transistor Q742 provides overcurrent protection for the +5 volt supply.

(d) −5 Volt Supply. Diagram 9 (FO-11) shows the −5 volt supply. The −5 volt supply consists of U762, Q764, Q766, Q768 and associated circuitry.

1 In the −5 volt supply, the noninverting input of the operational amplifier (U762) is not referenced to the +32 volt supply as in the +5 volt supply. Instead it is connected to ground (0 volts) through R764.

2 The inverting input of U762 does not directly sense the supply output voltage as in the +5 volt supply. Instead the inverting input senses both the +32 and −5 volt supplies through voltage divider R763-R762. This sets the inverting input to 0 volts. Since the +32 volt supply is constant, changes in the −5 volt supply are sensed at the inverting input.

3 The output of U762 is level shifted by several series connected diodes. The level shifted voltage controls the conduction of Q766. The collector of Q766 controls the conduction of Q768 which controls the −5 volt supply output voltage. Transistor Q764 provides overcurrent protection for the −5 volt supply.

4 Regulation of the −5 volt supply occurs as follows. Assume the −5 volt supply tries to go more negative. This tries to force the inverting input of U762 negative. The output of U762 drives the base of Q766 less negative. This causes Q768 to conduct less, causing its collector to go less negative and correct the original condition.

(e) Overcurrent Protection. The following describes overcurrent protection for the +32 volt supply. Overcurrent protection for the +5 volt and −5 volt supplies operates in a similar manner.

1 As the load on the +32 volt supply increases, the voltage dropped across R734 (the current sensing resistor) also increases. As the voltage across R734 increases it forces the emitter and the base of Q736 more positive.

2 When the load on the +32 volt supply becomes excessive, the voltage on the base of Q736 becomes sufficiently positive to forward bias Q734 through R732 and R733. As Q734 begins to conduct, it reduces the forward bias on Q732 and Q736 causing the +32 volt supply output to go less positive. The greater the load on the +32 volt supply the more Q734 conducts and the less positive the +32 volt supply goes.

3 The current sensing resistors for the +5 and −5 volt supplies are R748 and R768 respectively.

(f) +95 Volt Supply. Diagram 8 (FO-10) shows the +95 volt supply. The +95 volt supply consists of CR582 and associated circuitry. The +95 volt supply is powered by the high voltage oscillator through T550. The ac voltage on pin 2 of T550 is half wave rectified by CR582. The half wave rectified voltage is filtered by C582, L582, and C584. Regulation is provided by the high voltage regulator.

4.4 FUNCTIONS OF CONTROLS, CONNECTORS, AND INDICATORS.

The location of controls, connectors, and indicators is shown on Figure 6-2 (FO-1) in the foldout section at the rear of this manual. Detailed function descriptions are listed in Table 4-2.

Table 4-2. Functions of Controls, Connectors, and Indicators

Figure 6-2 Index No.	Control, connector, or indicator name	Function
1	LINE RANGE	Selects the line voltage range on which the instrument is to be operated. The ranges are indicated on the rear panel.
2	Fuse Holder	Contains the instrument line fuse.
3	Power Cord Connector	Connects the detachable power cord to the instrument.
4	POWER	Turns the instrument on and off. Pull to turn on; push to turn off.
5	ON Indicator	Indicates when power is applied to the instrument; flashes if the line voltage drops below allowable limits.
6	INTEN	Controls the brightness of the crt display.
7	ASTIG	Screwdriver adjustment used in conjunction with the FOCUS control to initially obtain a well defined display. Once set, usually requires little or no adjustment.
8	FOCUS	Adjusts for a well defined display during normal operation.
9	TRACE ROTATION	Screwdriver adjustment used to align the trace with horizontal graticule line.
10	CALIBRATOR	Provides a one volt, one kilohertz, square wave output for setting probe compensation and checking vertical gain.
11	Graticule	Internal graticule prevents parallax errors. Rise and fall time measurement points are indicated on the left edge, and near the top and bottom horizontal portions of the graticule.
12	BEAM FINDER	Locates an off screen display. When pushed, a compressed display is visible within the graticule area. This display is independent of position controls, intensity setting, or applied signals.
13	SCALE ILLUM	Controls graticule illumination.
14	VERT MODE	Selects the operating mode for the vertical deflection system. CH 1: Displays only signals applied to the CH 1 input connector. ALT: Signals applied to CH 1 and CH 2 input connectors are alternately displayed. The alternation occurs during retrace at the end of each sweep. Useful at sweep rates of 0.5 milliseconds/division or faster. The display begins to flicker at rates slower than 0.5 milliseconds/division; therefore, the CHOP mode should be used at these rates. ADD: Displays the algebraic sum of the signals applied to the CH 1 and CH 2 input connectors. CHOP: Signals applied to CH 1 and CH 2 input connectors are alternately displayed at a fixed rate of about 250 kilohertz. Useful at sweep rates of 0.5 milliseconds/division or slower. At rates above 0.5 milliseconds/division the chopped segments become visible; therefore, the ALT mode should be used.

Table 4-2. Functions of Controls, Connectors, and Indicators—Continued

Figure 6-2 Index No.	Control, connector, or indicator name	Function
14 (continued)		CH 2 OR X-Y: Displays only signals applied to the CH 2 input connector. Must be selected for X-Y operation. TRIG VIEW or 20 MHz BW: Three position switch. When pulled out, the bandwidth of the vertical deflection system is limited to 20 megahertz; when pushed part way in the vertical bandwidth is normal; and when pushed completely in and held, the signal applied to the A Sweep trigger generator is displayed.
15	VOLTS/DIV	Outer ring portion of the control selects the vertical deflection factor in a 1-2-5 sequence. Factors are calibrated when the VAR portion of the controls is in its fully clockwise detent position.
16	VAR	Inner knob portion of the VOLTS/DIV control. Provides continuously variable uncalibrated vertical deflection factors between calibrated settings. Extends the maximum vertical deflection factor to 125 volts/division when using a 10X probe. This control must be in its fully clockwise detent position for calibrated deflection factors.
17	Deflection Factor Indicator	A light colored area under the VOLTS/DIV control skirt, which indicates the vertical deflection factor associated with the probe being used. Check the attenuation factor of the probe and use the correspondingly marked light colored area.
18	UNCAL Indicator	Indicates when the VAR portion of the VOLTS/DIV control is out of its fully clockwise detent position and uncalibrated deflection factors are being used.
19	AC-GND-DC	Selects the method of coupling the input signal to the vertical input amplifier. AC: Input signals are capacitively coupled, blocking any dc component. Low frequencies are attenuated about 3 dB at 10 hertz using a 1X probe and at 1 hertz using a 10X probe. Ac coupling may cause tilting of square wave signals below about 1 kilohertz. GND: Connects the vertical input amplifier to ground to provide a ground reference display (input signal is disconnected). Connects the input signal to ground through the ac input capacitor and a one megohm resistor to keep the input coupling capacitor precharged. DC: Input signals are directly coupled, thus passing all components of the signal to the input amplifier.
20	Vertical Channel Input Connectors	Connects the Channel 1 and Channel 2 vertical input probes to the instrument. In the X-Y mode of operation, the CH 1 OR X input provides horizontal deflection and the CH 2 OR Y input provides vertical deflection.
21	POSITION	Provides vertical positioning control of the display. In the X-Y mode of operation, the CH 1 OR X control positions the display horizontally and the CH 2 OR Y control positions the display vertically.
22	INVERT	Inverts the Channel 2 display only.

Table 4-2. Functions of Control, Connectors, and Indicators—Continued

Figure 6-2 Index No.	Control, connector, or indicator name	Function
23	HORIZ DISPLAY	Selects the mode of operation for the horizontal deflection system. A: Horizontal deflection is provided by the A sweep generator at a rate set by A TIME/DIV. The B sweep generator (delayed sweep) is disabled. MIXED: The first part of the sweep is displayed at a rate set by A TIME/DIV and the last part of the sweep is displayed at a rate set by B TIME/DIV. The relative amount of display controlled by each setting is determined by the setting on the DELAY TIME POS dial. A INTEN: Horizontal deflection is provided by the A sweep generator at a rate set by A TIME/DIV. The B sweep generator produces an intensified zone on the display. The length of time the display is intensified is about ten times the B TIME/DIV setting except when A sweep ends before B sweep. The location of the intensified zone on the display is determined by the DELAY TIME POS dial setting. B DLY'D: Horizontal deflection is provided by the B sweep generator at a rate set by B TIME/DIV. The A sweep generator continues to operate. With the B sweep SOURCE set to STARTS AFTER DELAY, the start of B sweep is delayed from the start of A sweep by a time determined by the settings of A TIME/DIV and DELAY TIME POS. To calculate the delay, multiply the A TIME/DIV setting by the DELAY TIME POS dial setting.
24	POSITION	Provides horizontal positioning control of the display, except in the X-Y mode of operation when the CH 1 OR X, POSITION control provides horizontal positioning.
25	A AND B TIME/DIV	Selects the sweep rate for the A and B sweep. The A sweep rate is set by rotating the outer ring portion of the control. The rate is shown between the two black lines on the clear skirt of the control. This rate is multiplied by the DELAY TIME POS setting when using the A INTEN or B DLY'D display modes. For calibrated sweep rates, the VAR knob portion of the control must be in the fully clockwise detent position. The B sweep rate is set by pulling the outer ring out and rotating it to a setting shown by the white line scribed on the ring. The X-Y mode of operation is selected with the A sweep rate control is set fully counterclockwise.
26	VAR	Inner knob portion of the A AND B TIME/DIV control. Provides continuously variable uncalibrated sweep rates between calibrated settings of the A TIME/DIV settings. Must be in its fully clockwise detent position for calibrated A sweep rates and delay times.
27	UNCAL Indicator	Indicates when the VAR portion of the A AND B TIME/DIV control is out of its fully clockwise detent position and the A sweep rates are not calibrated.

Table 4-2. Functions of Control, Connectors, and Indicators—Continued

Figure 6-2 Index No.	Control, connector, or indicator name	Function
28	X10 MAG	Increases the displayed sweep rate by a factor of 10. Extends the fastest sweep rate to 5 nanoseconds/division. The magnified sweep display is the center one division of the unmagnified display (0.5 division from either side of the center vertical graticule line).
29	X10 MAG Indicator	Indicates when the X10 MAG is selected.
30	DELAY TIME POS	Provides a variable B sweep delay from 0.000 to 10.000 times the setting of the A TIME/DIV control.
31	TRIG MODE	Selects the mode of operation for the A sweep trigger. AUTO: With proper trigger LEVEL and COUPLING settings, A sweep can be initiated by signals above about 20 hertz. In the absence of a triggering signal or with control misadjustments, the A sweep generator free-runs to provide a reference display. NORM: With proper trigger LEVEL and COUPLING settings, A sweep can be initiated by an input signal. In the absence of a triggering signal or with control misadjustments, the A sweep generator does not run and there is no display. SGL SWP: A momentary contact push button, which cancels previous TRIG MODE selections and selects a single sweep mode of operation. This mode operates the same as NORM, except only one sweep is displayed on a trigger signal. Another single sweep cannot be displayed until the SGL SWP push button is pressed to reset the trigger circuit.
32	TRIG READY Indicator	Indicates the A sweep is reset and ready for a single sweep display when a trigger signal occurs. If the indicator is out when in the SGL SWP mode, the SGL SWP push button must be pressed to reset the trigger circuit.
33	SOURCE	Selects the source of trigger input signal. STARTS AFTER DELAY (B trigger only): B sweep runs immediately after the delay time selected by the A TIME/DIV setting multiplied by the DELAY TIME POS setting. No B trigger is required. In any other B trigger SOURCE setting a trigger is required after the delay time before B sweep will run. NORM: Provides a trigger from the vertical deflection system. The actual source is the displayed signal. In this mode, CH 1 and CH 2 time relationship measurements are not valid and should not be used. This mode is not recommended for use in the CHOP or ALT VERT MODE because the display triggers on the channel switching transients. CH 1: Provides a trigger from the CH 1 preamplifier. The CH 2 display may be unstable if it is not time related to CH 1. CH 2: Provides a trigger from the CH 2 preamplifier. The CH 1 display may be unstable if it is not time related to CH 2. LINE (A trigger only): Provides a trigger from a sample of the power-line frequency. This trigger is useful when channel inputs are time related (multiple or sub-multiple) to the power-line frequency. Also, it is useful for stabilizing a display that has a power-line frequency component on a complex waveform.

Table 4-2. Functions of Control, Connectors, and Indicators—Continued

Figure 6-2 Index No.	Control, connector, or indicator name	Function
33 (continued)		EXT: Provides a trigger from an external signal connected to the External Trigger Input connector. This trigger input must be time related to the input signals to provide a stable display. EXT (÷ by 10): The same as EXT above, except the input signal is attenuated by a factor of 10.
34	COUPLING	Selects the method used to couple signals to the trigger generator. AC: Selects capacitive coupling, which blocks dc components on the signal. Signals below about 60 hertz are attenuated. LF REJ: Selects capacitive coupling, which blocks dc components on the signal. Signals below about 50 kilohertz are rejected. Useful for displaying high frequency components of complex waveforms. HF REJ: Signals are capacitively coupled, which blocks the dc component. Signals below about 60 hertz and above about 50 kilohertz are attenuated. Useful for displaying low frequency components of complex waveforms. DC: All components of the signal are coupled. Useful for displaying low-frequency or low repetition rate signals.
35	LEVEL	Selects the amplitude point on the trigger signal at which the sweep is triggered. It is usually adjusted after the trigger SOURCE, COUPLING, and SLOPE have been selected.
36	SLOPE	Selects the slope of the trigger signal on which the sweep is triggered. OUT +: Sweep is triggered on the positive going portion of the trigger signal. IN−: Sweep is triggered on the negative going portion of the trigger signal.
37	External Trigger Input Connector	Connects external trigger input probe or cables to the instrument.
38	A TRIGGER HOLDOFF	Provides control of holdoff time between sweeps. Variable up to ten times the setting of the A TIME/DIV setting, except in the .2 and .5 second ranges. Useful when triggering on low repetition pulses or aperiodic signals. Obtain the best possible display using the A sweep trigger controls before setting the hold off time.
39	Ground Binding Post	External connector to chassis (earth) ground. The connector will accept cables or wires using open end solder lugs, banana plugs, or stripped wire for connection.
40	+A GATE	Provides a +5 volt positive pulse output during the A sweep time.
41	+B GATE	Provides a +5 volt positive pulse output during the B sweep time.
42	EXT Z AXIS	Connects external Z-axis inputs for crt intensity modulation. External inputs may also be used for crt blanking provided the crt intensity is properly set. Useful for adding time markers to a display, or when using the instrument as a peripheral display in a monitoring system.
43	CH 2 OUT	Provides an output signal from the CH 2 preamplifier. Useful for cascade operation (CH 2 into CH 1) to increase vertical deflection sensitivity. Also, may be used to trigger external equipment.

4-5. OPERATING CONSIDERATIONS.

To ensure optimum measurement accuracy, the following information should be considered before operating the oscilloscope.

a. Signal Connections. In general, probes offer the most convenient means of connecting an input signal to the instrument. They are shielded to prevent pickup of electrostatic interference. The 10X probe offers a high input impedance, which allows the circuit under test to perform very close to normal operation conditions. However, it also attenuates the input signal ten times.

(1) In high frequency applications that require maximum overall bandwidth, use coaxial cables terminated at both ends in their characteristic impedance. For further information, refer to the paragraph on Coaxial Cables below.

(2) High level, low frequency signals may be directly connected to the input connectors with short, unshielded leads. This coupling method works best for signals below about one kilohertz and deflection factors above one volt/division. When this method is used, establish a common ground between the instrument and the equipment under test. To avoid errors in the display, keep the leads away from any source of interference. If interference is excessive with unshielded leads, use a coaxial cable or a probe.

b. Loading Effect of Input Connections. As nearly as possible, simulate actual operating conditions in the equipment under test. Otherwise, the equipment under test may not produce a normal signal. Because of their high input impedance, the supplied probes offer the least circuit loading. When the signal is directly coupled to the input of this instrument, the input impedance is about one megohm paralleled by about 20 picofarads. When the signal is coupled to the input through a coaxial cable, the effective input capacitance depends upon the type and length of cable used. For information on obtaining maximum frequency response with coaxial cables, refer to the paragraph on Coaxial Cables below.

c. Coaxial Cables. Cables used to connect signals to the input connectors have a large effect on the accuracy of a displayed high frequency waveform.

(1) To maintain the high frequency characteristics of an applied signal, high quality, low loss coaxial cable should be used. Also, the cable should be terminated at both ends in its characteristic impedance. If it is necessary to use cables with differing characteristic impedances, use suitable impedance matching devices.

(2) To maintain fast rise time pulse characteristics; use the shortest length of coaxial cable possible. Also, observe the cable criteria for high frequency characteristics in (1) above.

d. Grounding. Reliable signal measurements cannot be made unless both the instrument and equipment under test are connected together by a common reference (ground) lead in addition to the signal lead or probe. Although the three-wire ac power cord provides a common connection when used with equipment with similar power cords, the ground loop produced may make accurate measurements impossible. The short ground lead connected to the probes provide the best signal ground. On coaxial cables, the shield provides a common ground when connected between two coaxial connectors (or with suitable adapters to provide a common ground). When using unshielded signal leads, a common ground lead should be connected from the chassis of the instrument (rear panel Ground Binding Post) to the chassis of the equipment under test.

e. Graticule. The internal 8 X 10 cm graticule provides parallax-free measurements. The graticule area is divided horizontally and vertically into 1 cm divisions. Vertical gain and horizontal timing are calibrated to the graticule, so accurate measurements can be made from the crt. Figure 4-17 shows the graticule with its various measurement markings. The terminology shown is used throughout this manual in discussions involving graticule measurements. Note the numeric scaling markings on the left side of the graticule. These are used when making rise or fall time measurements.

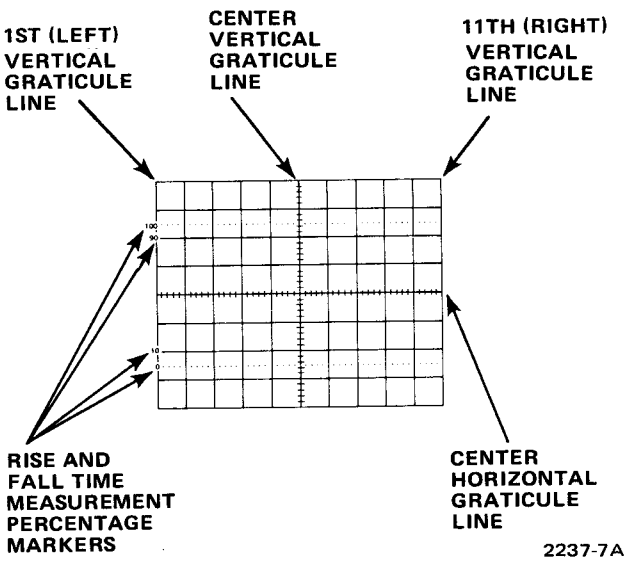


Figure 4-17 Graticule measurement markings

f. Common Mode Rejection (Figure 4-18). Some signals may contain undersirable components, such as in the dotted portion of Figure 4-18A. Common mode rejection can eliminate or reduce these components from the measurement. Use the following procedure to reduce or eliminate an undesireable line frequency component:

(1) Apply signal to CH 1 input connector.

(2) Apply line frequency signal to CH 2 input connector.

(3) Set VERT MODE to ALT.

(4) Push in INVERT button to invert channel 2 display.

(5) Set CH 2 VAR control to make channel 2 display amplitude about equal to undesired component of channel 1 display.

(6) Set VERT MODE to ADD and slightly readjust CH 2 VAR control for maximum rejection of undesired signal component (see Figure 4-18B).

g. Cascaded Operation. Maximum vertical sensitivity can be increased to approximately 1 millivolt/division by cascading the CH 1 and CH 2 amplifiers as follows:

(1) Connect CH 2 OUT signal (on rear panel) to CH 1 input via a 50 ohm cable and a 50 ohm termination.

(2) Set VERT MODE to CH 1.

(3) Apply an input signal to CH 2 input connector.

NOTE

In this mode, bandwidth is limited to about 40 megahertz.

h. Delayed Sweep Magnification. Following are two B Delayed modes, which may provide a higher apparent sweep rate magnification than provided by X10 MAG. First, try the Magnified Sweep Starts After Delay method. If this produces too much horizontal jitter, try the Magnified Triggered After Delay method.

(1) Magnified Sweep Starts After Delay (Figure 4-19). Use the following procedure to make delayed sweep magnification measurements.

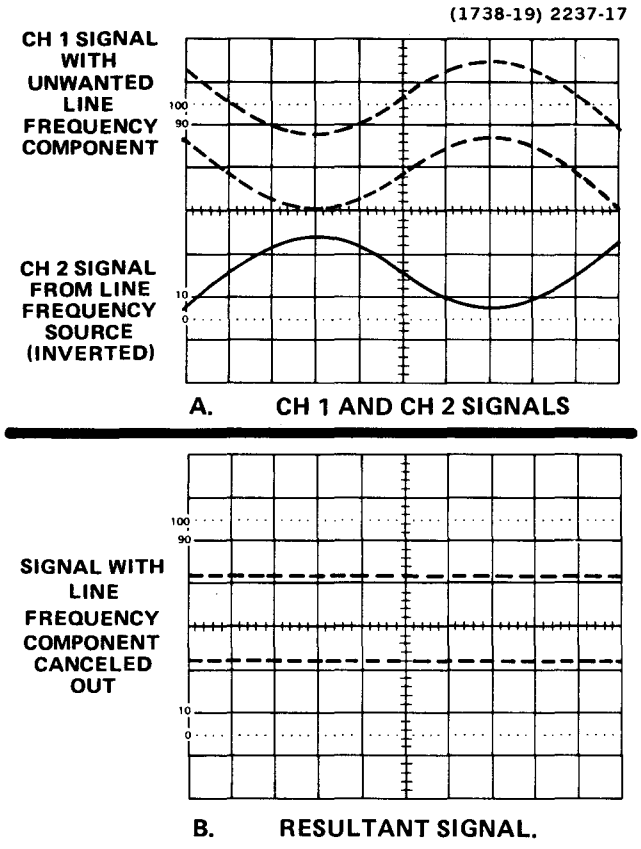


Figure 4-18. Common mode rejection of an undesired line-frequency.

(a) Set HORIZ DISPLAY to A INTEN and B SOURCE to STARTS AFTER DELAY.

(b) Use DELAY TIME POS to move the left edge of the intensified display to the left side of that portion of A sweep to be magnified.

(c) Set B TIME/DIV so just that portion of A sweep to be magnified is intensified (see Figure 4-19A).

(d) Set HORIZ DISPLAY to B DLY'D. The portion of A sweep that was intensified in (c) above is displayed in magnified form (see Figure 4-19B). The displayed sweep rate is determined by B TIME/DIV. To calculate the apparent magnification factor, use formula:

$$\text{Apparent Magnification} = \frac{\text{A TIME/DIV setting}}{\text{B TIME/DIV setting}}$$

(2) Magnified Sweep Triggered After Delay. If the Magnified Sweep Starts After Delay method above produces too much jitter, operate B sweep as follows:

(a) Perform steps (1) (a) through (1) (c) of Magnified Sweep Starts After Delay procedure above.

(b) Set B SOURCE to the same setting as A SOURCE. Set B LEVEL for a stable intensified zone.

NOTE

If the intensified zone cannot be stabilized, reset VOLTS/DIV for more display amplitude or use external triggering.

(c) Set HORIZ DISPLAY to B DLY'D. To obtain a stable display it may be necessary to slightly reset B LEVEL control.

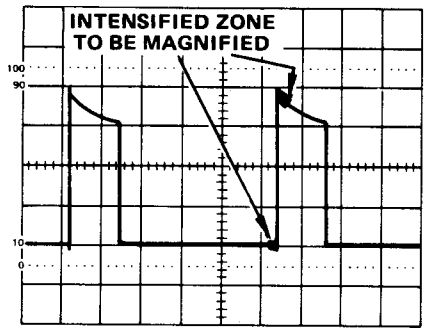
4-6. INITIAL INSTRUMENT TURN-ON.

Apply power to the instrument as follows:

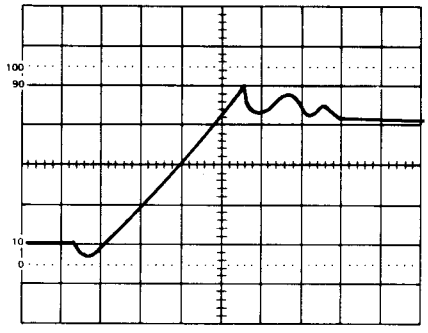
a. Verify that the instrument is configured for the correct power source (refer to the Operating Voltage Selection paragraphs in Section III, Preparation for Use and Shipment).

b. Remove the power cord from the front panel cover and plug it into the rear panel connector.

c. Connect the power cord to the power source receptacle.



A. A INTENSIFIED DISPLAY



B. B DLY'D DISPLAY

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Figure 4-19. Delayed sweep magnification.

d. Pull on the POWER switch. The ON indicator should light; if it blinks, the line voltage is too low.

e. Allow the instrument a few minutes to warm up (if actual measurements are to be taken, allow 5 minutes when the instrument has been stored in a temperature above 0°; 20 minutes for lower temperatures).

4-7. PRELIMINARY ADJUSTMENTS.

Before using the instrument for the first time, make the following preliminary settings and adjustments, then perform a NORMAL OPERATION functional check.

a. Initial Control Settings. Set the controls as follows (both channels if applicable):

VOLTS/DIV	.2 in 10X probe window
VAR	Fully clockwise (calibrated detent)
POSITION	Midrange
AC-GND-DC	DC
VERT MODE	CH 1
INVERT	Out (normal)
20 MHz BW	In (off)
TRIG MODE	AUTO
LEVEL	Midpoint of + slope, then adjust as necessary
SLOPE	OUT +
COUPLING	AC
A SOURCE	CH 1
B SOURCE	STARTS AFTER DELAY
DELAY TIME POS	Fully counterclockwise
A and B TIME/DIV	.2 ms
A VAR	Fully clockwise (calibrated detent)
HORIZ DISPLAY	A
X10 MAG	OUT (off)
A TRIGGER HOLDOFF	NORM
SCALE ILLUM	Fully counterclockwise
POSITION, INTEN, and FOCUS	Midrange

NOTE

At this point there should be a trace displayed. If not, recheck control settings. Then press BEAM FINDER and adjust the POSITION controls so the trace is centered vertically and horizontally on the crt. If no trace appeared when BEAM FINDER was pressed, the instrument is malfunctioning. If the trace appeared and could be centered, but disappeared when BEAM FINDER was released, increase the INTEN control.

b. Intensity Adjustment. Set the INTEN control for a comfortable viewing level. Later when FOCUS and ASTIG are adjusted, INTEN may need readjustment.

CAUTION

To protect the crt phosphor, do not turn the INTEN control higher than necessary to provide a satisfactory display. Since the blue faceplate filter reduces the display light output, avoid using too high an INTEN setting with this filter. When more intensity is desired, use the clear filter or reduce the ambient light level. The intensity may increase too high when changing the TIME/DIV settings from a fast to a slow sweep speed.

c. Focus and Astigmatism Adjustment. Adjust the FOCUS and ASTIG controls as follows:

(1) Connect a probe to either vertical channel. Then connect the probe to the CALIBRATOR output. Set VERT MODE to the channel being used.

(2) Adjust FOCUS so horizontal portion of display is focused.

(3) Adjust INTEN so rising portion of the display can be seen (If display is unstable, A LEVEL may need adjustment).

(4) Adjust ASTIG so horizontal and vertical portions of display are as equally focused as possible.

(5) Adjust FOCUS so vertical portion of display is as thin as possible.

(6) Repeat steps (4) and (5) for best overall display focus.

(7) Disconnect the probe from the CALIBRATOR output.

d. Trace Rotation Adjustment. Adjust the TRACE ROTATION control as follows:

(1) Set AC-GND-DC to GND.

(2) Vertically position the trace to the center horizontal graticule line.

(3) Adjust TRACE ROTATION so the trace is parallel to the center horizontal graticule line.

e. Graticule Scale Illumination. To obtain scale illumination, rotate SCALE ILLUM clockwise until the desired amount of illumination is reached.

f. Probe Compensation (Figure 4-20). Each time the P6104 probes are used with the instrument, probe compensation should be checked and adjusted if necessary. A low capacitance screwdriver should be used. Use the following procedure for adjusting P6104 probe compensation:

(1) Connect P6104 probes to CH 1 and CH 2 vertical inputs.

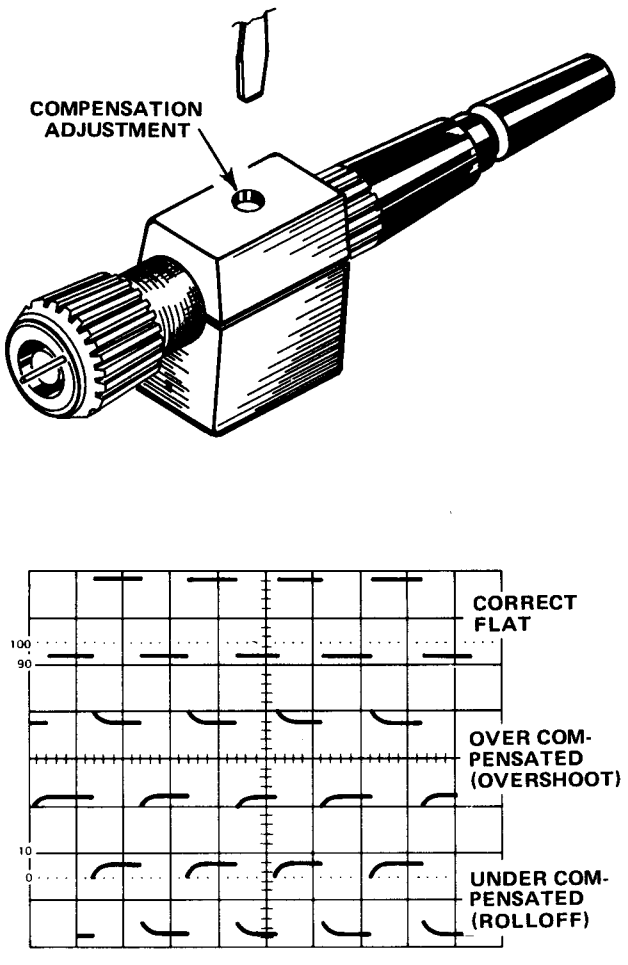


Figure 4-20. Probe compensation.

(2) Set the instrument controls as follows:

VOLTS/DIV	.2 (in 10X probe window)
A AND B TIME/DIV	.2 ms
AC-GND-DC	DC
VERT MODE	CH 1
A SOURCE	CH 1
A COUPLING	DC
HORIZ DISPLAY	A
SLOPE	OUT: +
LEVEL	Adjust as necessary for a stable display

(3) Connect the CH 1 and CH 2 probes to the CALIBRATOR. Adjust the POSITION controls so the top of at least one complete positive pulse is displayed.

(4) Adjust CH 1 probe compensation through hole in compensation box for the best flat top display.

(5) Set A SOURCE and VERT MODE to CH 2.

(6) Repeat step (4) above for CH 2.

4-8. NORMAL OPERATION.

The following procedures demonstrate the operation of the controls, connectors, and indicators. These procedures may also be used for operator familiarization or as an instrument functional check. Before starting, preset the controls as listed in paragraph 4-7. a., connect probes to CH 1 and CH 2, and connect the probes to the CALIBRATOR. Where vertical channel and horizontal sweep or trigger controls are duplicated, only one set of controls is demonstrated. The procedures are intended to be preformed in the sequence listed.

a. Beam Finder. Demonstrate BEAM FINDER operation as follows:

(1) Position the CH 1 display off screen with the vertical POSITION control.

(2) Push in and hold BEAM FINDER. The display should return to on screen. Adjust POSITION to center the trace vertically and horizontally. Release BEAM FINDER. The trace should be on screen.

(3) Adjust INTEN until the display disappears.

(4) Push in and hold BEAM FINDER. The display should reappear. Release BEAM FINDER. Readjust INTEN for a visible display.

b. Intensity and Focus. Demonstrate INTEN and FOCUS operation as follows:

(1) Rotate INTEN between its maximum clockwise and counterclockwise positions. The display should vary from a blooming intensity to no display. Reset INTEN to a comfortable viewing level.

(2) Rotate FOCUS between its maximum clockwise and counterclockwise positions. The display should become blurred on either side of an optimum control setting. Reset the control for the best focused display.

c. Vertical Deflection System. Demonstrate the operation of the controls in the vertical deflection system as follows:

(1) Select CH 1 on VERT MODE. There should be one display.

(2) Rotate CH 1 POSITION between its maximum settings. The display should move off screen in both vertical directions. Reset POSITION for a visible display.

(3) Set VERT MODE to ALT. There should be two displays.

(4) Alternately rotate CH 1 and CH 2 POSITION between their maximum settings. Their respective displays should move off screen in both vertical directions. Reset POSITION for two visible displays.

(5) Set A AND B TIME/DIV to 20 ms. The CH 1 and CH 2 traces should be alternately displaying.

(6) Set VERT MODE to CHOP. The CH 1 and CH 2 traces should be simultaneously displayed. Reset A AND B TIME/DIV to 5 ms and VERT MODE to ALT.

(7) Set A SOURCE to LINE. Push in and hold TRIG VIEW. The display should be a sample of the power line trigger signal. Release TRIG VIEW and reset A SOURCE to CH 1.

(8) Set A AND B TIME/DIV to .5 ms and VOLTS/DIV to .5.

(9) Adjust vertical POSITION for one display on each side of the center horizontal graticule line. If the display is not stable, adjust A LEVEL. The display should be two vertical divisions in amplitude and each pulse width one division wide (corresponds to a one volt peak to peak, one kilohertz square wave CALIBRATOR output).

(10) Set AC-GND-DC to GND and note the position of the baseline trace. Set AC-GND-DC to AC. The display should be equally displayed on each side of the baseline trace position. Reset AC-GND-DC to DC.

(11) Adjust horizontal POSITION so the display starts at the left vertical graticule line.

(12) Push in INVERT and adjust CH 2 vertical POSITION for an on screen display. The CH 2 display should be inverted. Push in INVERT again (releases it) and readjust POSITION for separated dual displays.

(13) Rotate CH 2 VAR to its fully counterclockwise position. The UNCAL indicator should light and the display should decrease in vertical size to 0.8 divisions or less. Return VAR to its fully clockwise detent position.

(14) Set A AND B TIME/DIV to X-Y and VERT MODE to CH 2 (same as OR X-Y). The two dot display should form a 45 degree angle to the horizontal.

(15) Set CH 1 AC-GND-DC to GND. The display should be two dots in a vertical line. Reset control to DC.

(16) Set CH 2 AC-GND-DC to GND. The display should be two dots in a horizontal line. Reset control to DC.

(17) Set A AND B TIME/DIV to .5 ms and VERT MODE to ALT.

NOTE

At this point there should be a dual display with two divisions of vertical amplitude and one division pulse widths. The displays should be somewhat centered in the upper and lower halves of the screen. If not, reset the vertical deflection system controls and A AND B TIME/DIV until this display is obtained before proceeding to the horizontal deflection system procedures.

d. Horizontal Deflection System. Demonstrate the operation of the controls in the horizontal deflection system (sweep) as follows:

(1) Normal and Magnified Sweep.

(a) Set VERT MODE to CH 1.

(b) Rotate A AND B TIME/DIV one or two positions on either side of .5 ms. The display sweep rate should change. Reset A AND B TIME/DIV to .1 ms. The display pulse width should be five divisions.

(c) Rotate VAR to its fully counterclockwise position. The UNCAL indicator should light and the display pulse width should decrease to two divisions or less. Return VAR to its fully clockwise detent position.

(d) Set A AND B TIME/DIV to 1 ms and push in X10 MAG. The X10 MAG indicator should light and the display pulse width should expand to five divisions. The magnified display is the center one division (0.5 division on either side of the center vertical graticule line) of the normal display.

(e) Push in X10 MAG again (releases it).

(2) Mixed Sweep.

(a) Set A AND B TIME/DIV to .5 ms, HORIZ DISPLAY to MIXED, and DELAY TIME POS to 5.0.

(b) Pull out on the A AND B TIME/DIV outer ring, rotate B TIME/DIV to .2 ms, and release the outer ring. The display should show a sweep rate change at about the center of the display. The first five divisions of the display is at the A sweep rate and the last five divisions of the display is at the B sweep rate.

(c) Rotate DELAY TIME POS on each side of the 5.0 setting and observe the movement of the starting point of the B sweep rate portion of the display. Reset DELAY TIME POS to 5.0.

(3) A Intensified Sweep.

(a) Set HORIZ DISPLAY to A INTEN and B TIME/DIV to .1 ms. The intensified portion of the display is the B sweep time.

(b) Rotate DELAY TIME POS on either side of 5.0 and observe the movement of the intensified portion of the display.

(4) B Delayed Sweep.

(a) Set HORIZ DISPLAY to B DLY'D. The display is the intensified portion of the display seen in (3) (a) above.

(b) Rotate B TIME/DIV one position on either side of .1 ms. The display sweep rate should change. Reset B TIME/DIV to .1 ms.

(5) Normal Trigger.

(a) Set HORIZ DISPLAY to A and TRIG MODE to NORM. Rotate A LEVEL for a stable display. Adjust horizontal POSITION so display starts at the left vertical graticule line. Note that the display starts with a positive pulse.

(b) Push in A SLOPE (IN:—). Note that the display now starts with a negative pulse. Push in SLOPE again to reset it to the OUT: + position.

(6) Single Sweep Trigger.

(a) Adjust A LEVEL so display is just barely stabilized.

(b) Set A COUPLING to LF REJ.

(c) Push and release SGL SWP. The previously selected TRIG MODE should cancel.

(d) While watching the TRIG READY indicator and the display, push in and release SGL SWP. The indicator should have blinked and a display should have flashed across the screen. This indicates the trigger circuit was reset and then triggered.

(e) Disconnect the CH 1 probe tip from the CALIBRATOR and push in SGL SWP again. The TRIG READY indicator should be lit. While watching the TRIG READY indicator and the display, touch the CH 1 probe tip to the CALIBRATOR. The TRIG READY indicator should have gone out as the display flashed across the screen.

(f) Reset A COUPLING to AC and TRIG MODE to AUTO.

(g) Disconnect the probe tips from the CALIBRATOR.

(7) Low Frequency Rejection Trigger.

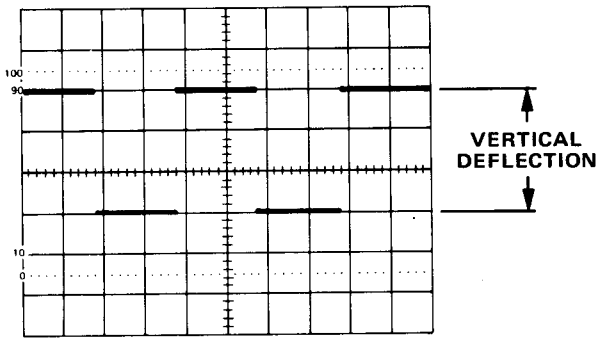
(a) Set A SOURCE to LINE and A AND B TIME/DIV to 10 ms.

(b) Push in and hold TRIG VIEW. The display should be a sample of the power line trigger input. Set A COUPLING to LF REJ. The display should disappear showing that the low frequency trigger rejection circuitry is working.

4-9. INSTRUMENT TURN OFF. The instrument is turned off by pushing in on the POWER push button. When turned off, the ON indicator should extinguish.

4-10. APPLICATIONS. The following information describes procedures and techniques for making specific measurements.

a. Peak to Peak Amplitude Measurement (Figure 4-21). Measure the peak to peak amplitude of a signal by multiplying the vertical deflection (in divisions) by the VOLTS/DIV setting.



EXAMPLE:

VERTICAL DEFLECTION	X	VOLTS/DIV SETTING	=	AMPLITUDE
3 DIVISIONS	X	.5 VOLTS/ DIVISION	=	1.5 VOLTS PEAK-TO-PEAK

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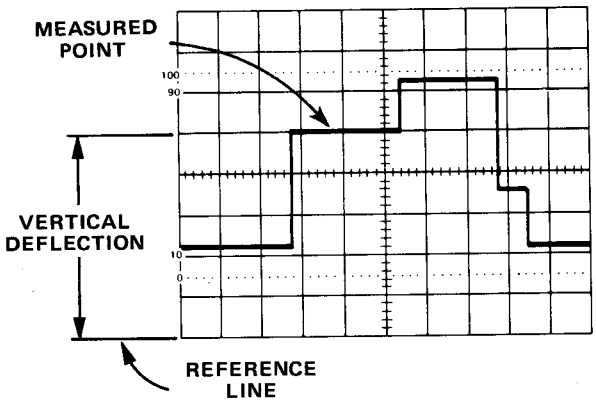
Figure. 4-21. Example of peak to peak voltage measurement.



EXAMPLE:

VERTICAL DEFLECTION FROM REFERENCE LINE TO MEASURED POINT	X	VOLTS/DIV SETTING	=	INSTANTANEOUS AMPLITUDE
5 DIVISIONS	X	10 MILLIVOLTS/ DIVISION	=	50 MILLIVOLTS

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Figure 4-22. Example of instantaneous voltage measurement.

b. Instantaneous Amplitude Measurement (Figure 4-22). Measure the amplitude of any point on a waveform with respect to ground as follows:

(1) Set AC-GND-DC to DC.

(2) Apply signal to be measured to either vertical input connector. Set VERT MODE to channel being used.

(3) Obtain a stable display.

(4) Set AC-GND-DC to GND. Position trace to a reference line.

(5) Set AC-GND-DC to DC. If waveform appears above reference line, voltage is positive. If waveform appears below reference line, voltage is negative.

(6) Measure vertical difference (in divisions) between reference line and desired point on waveform and multiply by VOLTS/DIV setting.

c. Dual Trace Phase Difference Measurement (Figure 4-23). Phase comparisons between two signals of the same frequency can be made using the dual trace feature. This method can be used up to the frequency limit of the vertical system and is usually more accurate and easier to use then the X-Y method. To make the comparison, use the following procedure:

(1) Set both AC-GND-DC to AC.

(2) Set VERT MODE to CHOP or ALT. (CHOP is more suitable for low frequency signals; ALT is more suitable for high frequency signals.) Position both traces to center horizontal graticule line.

(3) Set A SOURCE to CH 1.

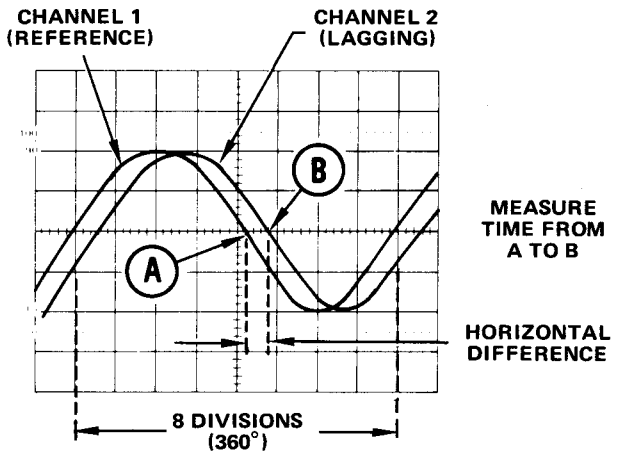
(4) Connect reference signal to CH 1 input connector and comparison signal to CH 2 input connector using coaxial cables or probes which have equal time delay.

(5) If signals are of opposite polarity, push INVERT button to invert CH 2 display. (Signals may be of opposite polarity due to 180° phase difference; if so, take this into account in final calculation.)

(6) Set CH 1 and CH 2 VOLTS/DIV and their associated VAR controls so displays are equal and about five divisions in amplitude.

(7) Set TIME/DIV to a sweep rate which displays about one cycle of reference waveform.

(8) Set VAR TIME/DIV until one cycle of reference signal (CH 1) occupies exactly 8 divisions between the second and tenth graticule lines.



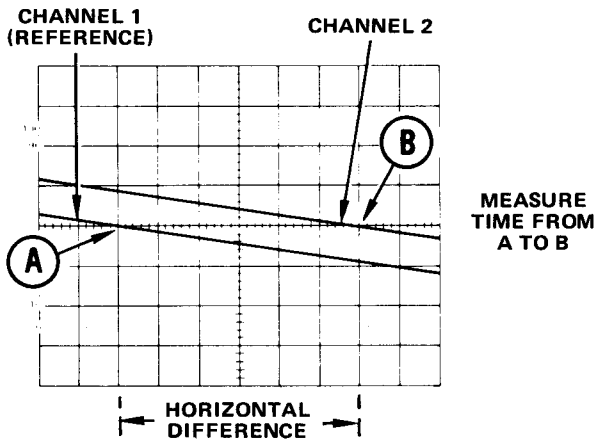
EXAMPLE:

HORIZONTAL DIFFERENCE (A TO B) X DEGREES/ DIVISION = PHASE DIFFERENCE

0.6 DIVISION X 45°/ DIVISION = 27°

(465/DM-0-15) 2237-21

Figure 4-23. Example of dual trace phase difference measurement



EXAMPLE:

HORIZONTAL DIFFERENCE (A TO B) X DEGREES/ DIVISION = PHASE DIFFERENCE

6 DIVISIONS X 4.5°/ DIVISION = 27°

(465/DM-0-16)2237-22

Figure 4-24. Example of high resolution phase difference measurement.

NOTE

Each division of graticule represents 45° of cycle (360° ÷ 8 divisions = 45°/division). Therefore; the sweep rate can be stated in terms of degrees as 45°/division.

(9) Measure horizontal difference (in divisions) between corresponding points on waveforms.

(10) Multiply difference (in divisions) by 45°/division (sweep rate) to obtain exact amount of phase difference.

d. High Resolution Phase Difference Measurement (Figure 4-24). For phase differences less than 45°, measurement accuracy is increased by using X10 MAG as follows:

(1) Perform steps (1) through (8) of 4-10 c above.

(2) Center the measurement points on the vertical graticule line.

(3) Push in X10 MAG. Sweep rate is now 4.5°/division (45°/division ÷ 10).

(4) Slightly reset horizontal POSITION control to move measurement points within graticule area.

(5) Measure horizontal difference (in divisions) between corresponding points on waveforms.

(6) Multiply difference by magnified sweep rate (4.5°/division).

e. Time Duration and Frequency Measurement (Figure 4-25). Measure the time duration between two points on a waveform by multiplying the horizontal distance (in divisions) between the points by the TIME/DIV setting. Frequency is the reciprocal of the time duration measurement of one cycle.

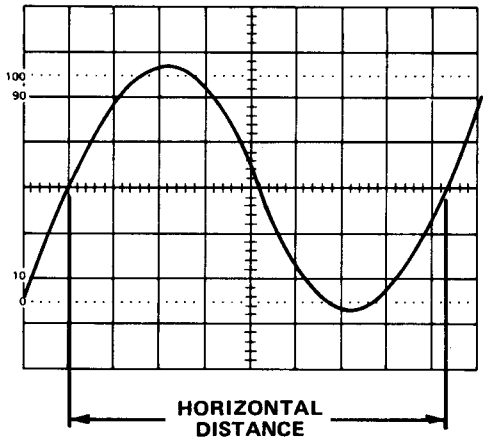
f. Rise Time Measurement (Figure 4-26). Rise time measurements are made in the same manner as time duration measurements, except the horizontal measurements are made between the 10% and 90% points of the waveform amplitude (see percentage markings on the left edge of the graticule) as follows:

(1) Set VOLTS/DIV and its associated VAR control for a 5 division display.

(2) Adjust vertical POSITION so display is between the 0% and 100% lines.

(3) Measure horizontal distance (divisions) between 10% and 90% points on waveform (points A and B).

g. Differential Time Measurement. Differential time measurements can be made using either the A INTENS, B DLY'D, or MIXED HORIZ DISPLAY modes.



EXAMPLE:

HORIZONTAL DISTANCE X **TIME/DIV SETTING** = **TIME DURATION**

8.3 DIVISIONS X **2 MILLISECONDS/ DIVISION** = **16.6 MILLISECONDS**

$$\frac{1}{\text{TIME DURATION}} = \text{FREQUENCY}$$

$$\frac{1}{16.6 \text{ MILLISECONDS}} = 60 \text{ HERTZ}$$

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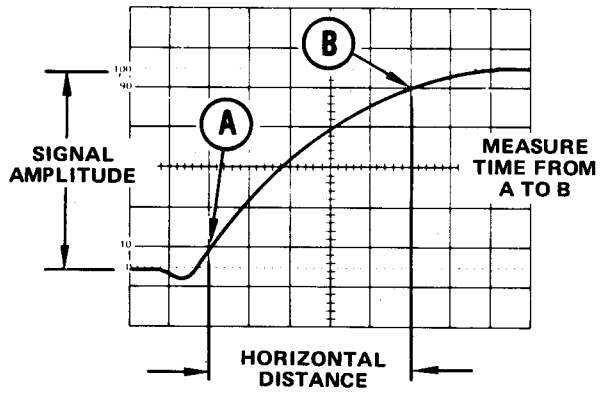
Figure 4-25. Example of time duration and frequency measurement



EXAMPLE:

HORIZONTAL DISTANCE (A TO B) X **TIME/DIV SETTING** = **RISE TIME**

5 DIVISIONS X **1 MICROSECOND/ DIVISION** = **5 MICROSECONDS**

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Figure 4-26. Example of rise time measurement.

(1) A Intensified Differential Time Measurement (Figure 4-27). Use the following procedure to make differential time measurements using the A INTEN mode:

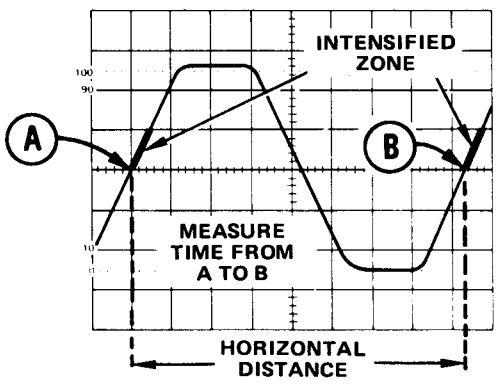
(a) Set A TIME/DIV and horizontal POSITION control to locate both time measurement points within graticule area.

(b) Set HORIZ DISPLAY to A INTEN and B SOURCE to STARTS AFTER DELAY.

(c) Pull out and set B TIME/DIV for the shortest useable intensified display zone.

(d) Use DELAY TIME POS control to move the left edge of intensified zone to just touch the first time measurement point (point A). Note DELAY TIME POS (1st DTP setting) setting.

(e) Use DELAY TIME POS control to move left edge of intensified zone to just touch the second time measurement point (point B). Note DELAY TIME POS (2nd DTP setting) setting.



EXAMPLE:

2ND DTP SETTING − **1ST DTP SETTING** X **A TIME/DIV SETTING** = **TIME DIFFERENCE**

9.56 − **1.23** X **2 MILLISECONDS** = **16.66 MILLISECONDS**

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Figure 4-27. Example of time duration measurement using A INTEN mode.

(2) B Delayed Differential Time Measurement (Figure 4-28). Use the following procedure to make differential time measurements using the B DLY'D mode:

(a) Set A TIME/DIV and horizontal POSITION control to locate both time measurement points within graticule area (see Figure 4-28A).

(b) Set HORIZ DISPLAY to A INTEN and B SOURCE to STARTS AFTER DELAY.

(c) Pull out and set B TIME/DIV for the shortest usable intensified display zone.

(d) Turn DELAY TIME POS so that first time measurement point (point A) is in center of intensified zone.

(e) Set HORIZ DISPLAY to B DLY'D.

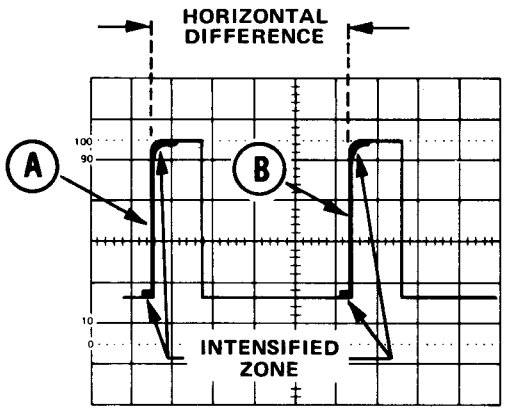
(f) Slightly reset DELAY TIME POS to move first time measurement point to the closest vertical graticule line (see Figure 4-28B). Note DELAY TIME POS (1st DTP setting) setting.

(g) Set HORIZ DISPLAY to A INTEN.

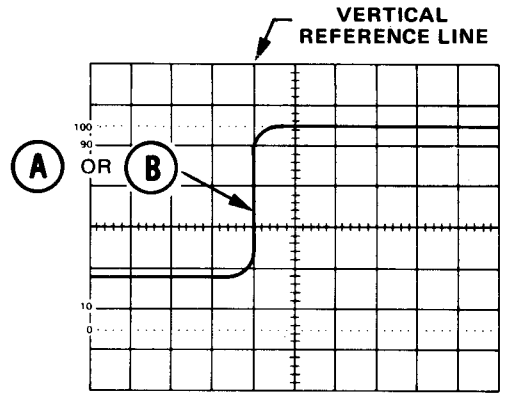
(h) Repeat step (d) for the second time measurement point (Point B).

(i) Set HORIZ DISPLAY to B DLY'D.

(j) Slightly reset DELAY TIME POS to move second time measurement point to the same vertical graticule line used in step (f). Note DELAY TIME POS (2nd DTP setting) setting.



A. A INTENSIFIED DISPLAY



B. B DELAYED DISPLAY

EXAMPLE:

2ND DTP SETTING	−	1ST DTP SETTING	×	A TIME/DIV SETTING	=	TIME DIFFERENCE
5.57	−	0.88	×	.2 MICROSECONDS	=	0.938 MILLISECONDS

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Figure 4-28. Example of time duration measurement using B DLY'D mode.