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COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7A42
LOGIC TRIGGERED VERTICAL AMPLIFIER

SERVICE (VOLUME 1)

For Qualified Service Personnel Only

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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Product Group 42

Serial Number _____

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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CIRCUIT-BOARD PINS ...
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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL

Static-Sensitive Devices

This symbol indicates where applicable cautionary or other information is to be found.

AS MARKING ON EQUIPMENT

DANGER—High voltage

Protective ground (earth) terminal.

ATTENTION—refer to manual.

WARNINGS

POWER SOURCE

This product is intended to operate in a mainframe connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, plug the mainframe power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective-ground connection by way of the grounding conductor in the mainframe power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating), can render an electric shock.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gasses.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels *properly installed.*

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury, *do not operate this product* without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary

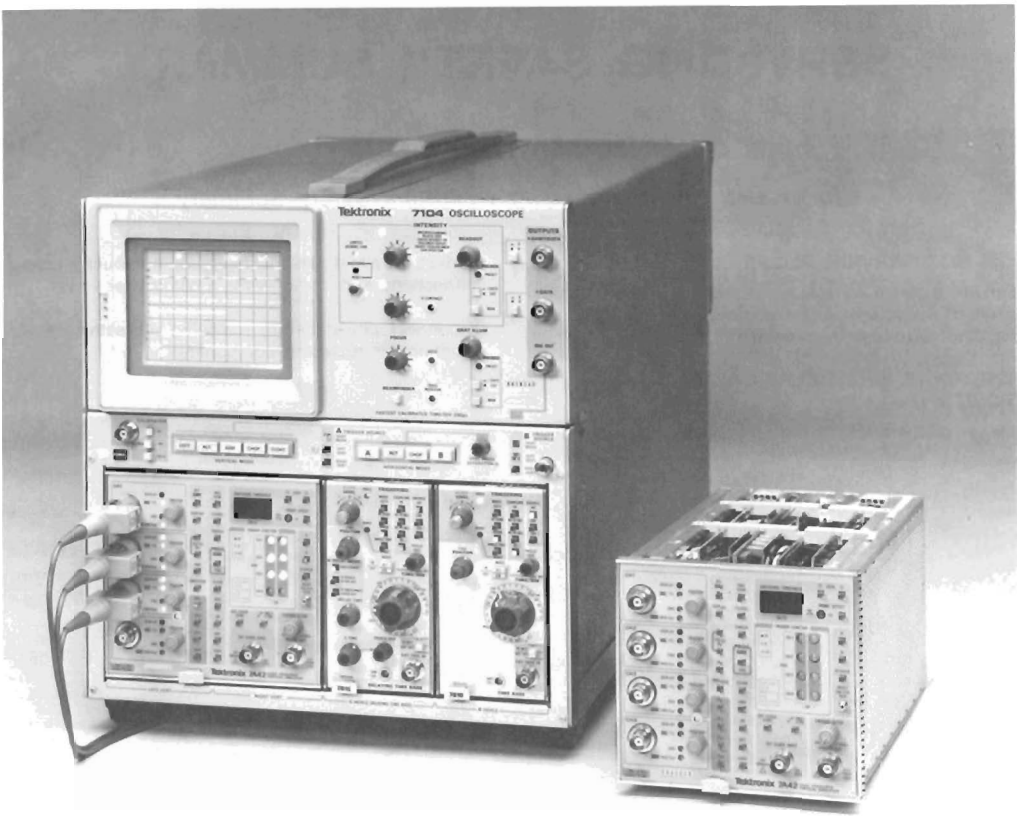
DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.



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7A42 FEATURES

The 7A42 Logic Triggered Vertical Amplifier is a four channel, wide bandwidth, plug-in unit, compatible with Tektronix 7000-series Oscilloscopes. It was specifically designed to display and make measurements on digital logic signals in the TTL, ECL and CMOS logic families. While the display output from the 7A42 is analog, the trigger output is digital and is comprised of a user selectable Boolean function of the four input channels. A fifth TRIGGER VIEW trace depicts either the trigger function output or the external clock input.

GENERAL INFORMATION

This section contains a basic content description of both the Operators and Service manuals, information on instrument installation, power requirements, packaging for shipment, Standard Accessories, Optional Accessories, Specifications and a dimensional drawing of the 7A42. The specification portion consists of three tables: Electrical, Environmental, and Physical Characteristics.

TECHNICAL MANUALS

An operators and two service manuals are supplied with your 7A42 as standard accessories. The following information outlines the content of these manuals.

Operators Manual

The Operators Manual is divided into the following four sections:

Section 1—GENERAL INFORMATION contains content descriptions of the Operators and Service manuals, instrument description, mainframe and plug-in compatibility, packaging instructions and instrument specifications.

Section 2—OPERATING INSTRUCTIONS contains a block diagram description, a front-panel drawing and brief description of controls, connectors and indicators. Get-Acquainted Exercises provide a basic operating procedure for the first-time user followed by a systematic demonstration of all front-panel controls. A detailed description of all front-panel controls is also given in this section.

Section 3—APPLICATIONS gives examples of how to use the 7A42 to make some difficult measurements.

Section 4—INSTRUMENT OPTIONS contains a description of available options.

Service Manual

WARNING

The following service instructions are for use by qualified personnel only. To avoid personal injury, do not perform any service other than that contained in the operating instructions unless you are qualified to do so. Refer to Operators Safety Summary and Service Safety Summary prior to performing any service.

The service manual is divided into 2 volumes. Volume 1 contains the following:

Section 1—GENERAL INFORMATION contains content descriptions of the Operators and Service manuals, mainframe and plug-in compatibility, packaging instructions, instrument specifications, and operating instructions.

Section 2—THEORY OF OPERATION contains basic and general circuit analysis that is useful for servicing the instrument.

Section 3—MAINTENANCE describes preventive maintenance procedures, conventional troubleshooting and diagnostic troubleshooting procedures with detailed instructions for replacing assemblies, subassemblies, and individual components.

Section 4—CHECKS AND ADJUSTMENT contains procedures to check the operational performance and electrical characteristics of the instrument. Procedures also include methods for adjustment of the instrument to meet specifications.

Section 5—INSTRUMENT OPTIONS contains a description of available options.

Section 6—REPLACEABLE ELECTRICAL PARTS contains information necessary to order replaceable parts and assemblies related to the electrical functions of the instrument.

Section 7—DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS includes detailed circuit schematics, locations of assembled boards within the instrument, voltage and waveform information and circuit board component locators.

Section 8—REPLACEABLE MECHANICAL PARTS includes information necessary to order replaceable mechanical parts and shows exploded drawings which identify assemblies.

Volume 2 of the service manual contains signature analysis tables to be used with the diagnostic information provided in the Maintenance section of the Volume 1 service manual.

INSTALLATION

INITIAL INSPECTION

This instrument was inspected both mechanically and electrically before shipment. It should be free of mars or scratches and should meet or exceed all electrical specifications. To confirm this, inspect the instrument for physical damage incurred in transit and check the basic instrument functions by performing the Performance Check Procedure in the Checks and Adjustment section of this manual. If there is damage or deficiency, contact your local Tektronix Field Office or representative.

OPERATING TEMPERATURE

The 7A42 can be operated where the ambient air temperature is from 0° to +50° C and can be stored in ambient temperatures from −55° to +75° C. After storage at temperatures outside the operating limits, allow the chassis temperature to reach operating limits before applying power.

INSTALLING THE 7A42 IN THE MAINFRAME

The 7A42 is designed to operate in the two center or the two left plug-in compartments of a Tektronix 7000-series oscilloscope mainframe.

NOTE

Switch off the mainframe power before installing or removing the 7A42.

To install the 7A42 in the mainframe, align the grooves in the top and bottom of the instrument with the guides at the top and bottom of the plug-in compartment. Then push the 7A42 in until its front panel is flush with the front panel of the mainframe.

To remove the 7A42 from its host mainframe, pull the release latch (see Fig. 1-1) to disengage the unit from the mainframe, then pull the 7A42 straight out from the plug-in compartment leaving the mainframe on the bench.

MAINFRAME COMPATIBILITY

The 7A42 is compatible with all Tektronix 7000 series mainframes. In four-wide plug-in compartment mainframes, it can be installed in either the two left or two center plug-in compartments. When used in the two left compartments, select the Left Vertical Mode to display the analog signals. The associated time base plug-in Trigger Source should be Left Vertical with the time-base trigger controls set to Auto or Norm, Dc, Internal, Slope to +, with the Level control centered. The A Then B Gate Output can be picked off from the RIGHT VERTICAL TRIGGER SOURCE by a 7D11 or 7D15 from either horizontal compartment. In three-wide plug-in compartment mainframes, the 7A42 must be used in the two left compartments in a similar way.

When the 7A42 is installed in the center two plug-in compartments of a four compartment mainframe; set the

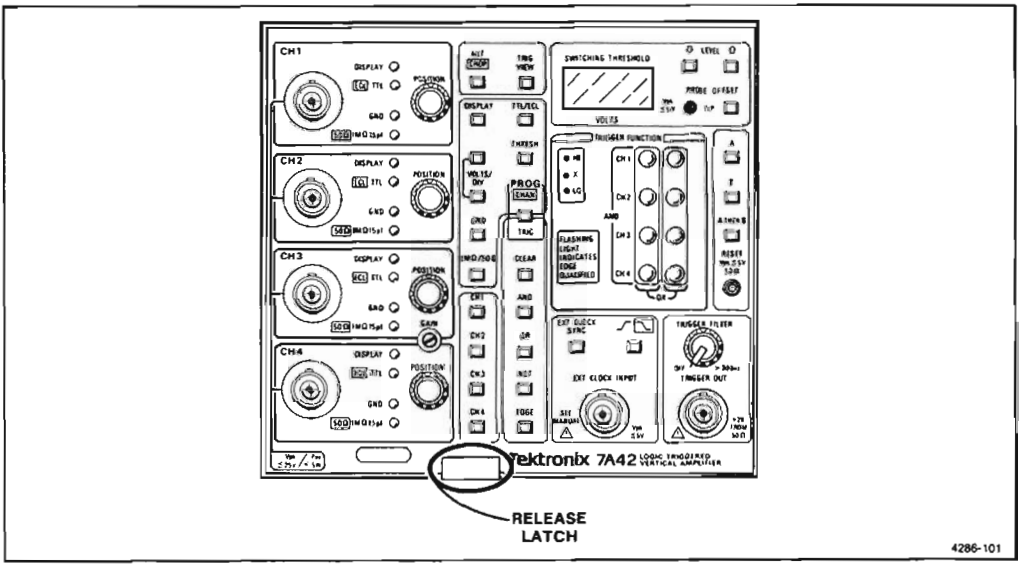


Figure 1-1. 7A42 release latch.

mainframe Vertical Mode and Trigger Source to Right Vertical. The mainframe A Then B Gate Output can not be used in this configuration, however, the A Then B Gate is still available at the front-panel TRIGGER OUT bnc connector.

Since all analog channels are sent out the 7A42's left interface connector, it cannot use the full capabilities of a dual beam oscilloscope such as the 7844, R7844, and the 7612D. However, it has full compatibility with these mainframes in a single beam configuration.

Since the 7A42 uses the mainframe crt readout to display the channel volts per division and error warning messages, the 7A42 is not recommended for use in mainframes without readout.

If the 7A42 is used with two time-base units in a four compartment mainframe where Chop has been selected as the Horizontal Mode, and if exactly four traces are to be displayed by the 7A42, two of the traces may synchronize to one time base while the other two traces synchronize to the other time base. To prevent this from happening, one trace should be removed, or a fifth trace should be added to the mainframe crt display (even if it is positioned off screen so it cannot be seen). With one, two, three, or five traces, the channel display will not synchronize to the horizontal chop frequency.

The 7A42 is compatible with the 7854 Oscilloscope mainframe when the 7854 is operated in real-time. However, when the 7854 is operated in digital storage, and waveform and readout acquisition is desired, the 7A42-7854 mode should be selected by moving jumper P540 to the 7854 mode. To locate P540 refer to Figure 3-7 in the Maintenance section of this manual. Once the 7A42-7854 mode has been selected, proper readout and waveform acquisition can be guaranteed with the following 7A42 display conditions:

1. Any single channel displayed alone (CH1, CH2, CH3, CH4, or TRIG VIEW).

2. Channels 1 and 2 only displayed together, ALT display mode selected.

3. Channels 3 and 4 only displayed together, ALT display mode selected.

Refer to the Applications section in the Operators manual for further information.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped by commercial transportation, we recommend that the instrument be packaged in the original manner. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

NOTE

Package and ship Plug-Ins and Mainframes separately.

If this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of a person at your firm who can be contacted, complete instrument type and serial number, and a description of the service required.

If the original package is unfit for use or not available, package the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions; refer to Table 1-1 for carton test strength requirements.

2. Enclose the instrument with polyethylene sheeting or equivalent to protect the finish of the instrument.

3. Cushion the instrument on all sides by tightly packaging dunnage or urethane foam between the carton and the instrument, allowing three inches of packaging on each side.

4. Seal the carton with shipping tape or with an industrial stapler.

5. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

TABLE 1-1
Shipping Carton Test Strength

Gross Weight (lb)	Carton Test Strength (lb)
0	200
10-30	275
30-120	375
120-140	500

SPECIFICATION

The electrical characteristics listed in Table 1-2 apply when the following conditions are met: (1) Adjustment of the instrument must have taken place at an ambient temperature between +20° and +30° C, (2) the instrument is allowed a 20-minute warm-up period, (3) specifications are valid at an ambient temperature of 0° to +50° C, unless otherwise stated, (4) the instrument must be in an environment that meets the limits described in Table 1-3, (5) the instrument must be operated in a calibrated 7000-series mainframe.

Any applicable conditions not listed above may be stated as part of the characteristic. Environmental characteristics are listed in Table 1-3 and Physical characteristics are listed in Table 1-4.

TABLE 1-2
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY		
Deflection Factor		
Calibrated Range at Input BNC Connector		
TTL (CMOS) Family	0.1, 0.2, 0.5 V/div.	
ECL Family	20, 50, 100 mV/div.	
Calibrated Range through a 10X Probe		
TTL (CMOS) Family		1, 2, 5 V/div.
ECL Family		0.2, 0.5, 1 V/div.
Channel to Channel Gain Match	Within 2% in ECL Logic Family, 20 mV/div, 1 Megohm input impedance.	
Gain Ratio Accuracy within the same Channel	Within 2% of indicated deflection factor relative to ECL Logic Family, 20 mV/div, 1 Megohm input impedance.	
GAIN Range		Permits adjustment of deflection factor for calibrated operation with any calibrated 7000-series mainframe. Adjustable at least +4% to -4% from calibrated setting.
Frequency Response		
Bandwidth	350 MHz in 7104, 0°-35°C mainframe ambient temperature. Refer to Tektronix Product Catalog 7000-Series Oscilloscope System Specification for system bandwidths.	

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY (CONT)		
Input Signal Dynamic Range		
Maximum Signal Voltage at tip of 10X Probe		
TTL (CMOS) Family		±30 V.
ECL Family		±6 V.
Output Dynamic Range		Limited to the CRT display area. Mainframe Vertical Trace Separation should not be used to bring an off-screen signal onto screen.
Maximum Input Voltage		
1 Megohm		25 V (dc + peak ac) 36 MHz or less, derated linearly to 3 V (peak ac) at 300 Mhz.
50 Ohm		5 V RMS during any 1 ms time interval. Active internal protection opens all inputs if overvoltage is applied to any channel.
50-Ohm Input Protection Reaction Time		
Maximum time to open input with applied overvoltage of:		
10 V DC	10 seconds.	
15 V DC	1 second.	
20 V DC	0.5 second.	
Input Characteristics		
Input Coupling		
DC		Incoming signal is dc-coupled to the amplifier.
GND		A grounded input is actually open at the input BNC, (i.e., 1 Megohm or 50 Ohm termination is disconnected). Internally, the amplifier input is grounded to provide a zero-volt input reference.
High Impedance	1 Megohm ±1%, in parallel with approximately 15 pF.	
Low Impedance	50 ohms ±1 ohm at dc.	
VSWR		≤1.15:1, dc to 300 MHz.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY (CONT)		
VOLTS/DIV Shift	0.2 divisions or less shift when VOLTS/DIV is changed in either TTL or ECL Families or between Families.	
POSITION Range		At least +7 divisions to −7 divisions but less than +9 divisions to −9 divisions from graticule center with gain calibrated.
Displayed Noise		Grounded input at maximum sensitivity, 7A42 triggered on another channel, tested at 1 ms/div and 10 ns/div, not more than 0.02 divisions RMS, as measured in a 7854.
DC Drift		
Drift with Time		Not more than 0.2 divisions in any 10 minutes after twenty minute warm-up (ambient temperature and line voltage constant).
Drift with Temperature		Not more than 0.2 divisions for 10° C ambient change (line voltage constant).
Differential Delay Between Any Two Channels, set to Same Logic Family and VOLTS/DIV	200 ps maximum.	
Plug-in Delay Time		Typically 25 ns from channel input to A11 and B11 of mainframe interface connector.
Channel to Channel Crosstalk		Typically less than 0.05 divisions with logic signal inputs applied through a 10X probe.
Chop Frequency		See mainframe manual for specifications.
TRIG VIEW or External Clock View		
Amplitude	0.35 divs ±0.1 div.	
Position		Baseline to be set 3 divisions (±0.5 divisions) below graticule center. Internally adjustable approximately ±4 divisions from graticule center. See Section 4 for adjustment procedure.
Risetime		2 ns or less.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
DISPLAY (CONT)		
TRIG VIEW or External Clock View (cont)		
Time Coincidence with Channel Display		
TRIG VIEW	Within 3 ns.	
External Clock View	Within 5 ns.	
Readout		Displayed on crt, see detailed operating information.
TRIGGER		
SWITCHING THRESHOLD		
Voltage Range		
At Input BNC		
TTL (CMOS) Family	+1.28 V to -1.27 V.	
ECL Family	+256 mV to -254 mV.	
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		+12.8 V to -12.7 V.
ECL Family		+2.56 V to -2.54 V.
Resolution		
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		100 mV.
ECL Family		20 mV.
Accuracy, at Center Value of Hysteresis Window		
At Input BNC		
TTL (CMOS) Family	±5 mV ±2% of setting.	
ECL Family	±1 mV ±2% of setting.	
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		±50 mV ±2% of setting.
ECL Family		±10 mV ±2% of setting.
Hysteresis, Centered at Threshold, 50kHz (sine-wave)		
At Input BNC		
TTL (CMOS) Family	40 mV +20%, -50%.	

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
SWITCHING THRESHOLD (cont)		
Hysteresis, Centered at Threshold, 50kHz (sine-wave)		
ECL Family	8 mV +20% -50%.	
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		400 mV ±20%, -50%
ECL Family		80 mV ± 20% -50%
Presets		
At tip of 10X probe with readout compensation		
TTL (CMOS) Family		+1.4 V.
ECL Family		−1.30 V.
PROBE OFFSET Activated		0 V.
TIP (PROBE OFFSET) Input		
Maximum Voltage Range	+5.10 V to −5.10 V, dc only.	
Input Resistance		≥100 KΩ.
DVM Resolution		20 mV.
DVM Accuracy	±20 mV ±2% of reading.	
TRIGGER FILTER		
Range	Off, or adjustable from <15 ns to >300 ns.	The trigger filter cannot be activated if the EXT CLOCK is turned on, nor will it operate with any trigger function that contains an edge sensitive channel.
Match, Function A to Function B	Within 20%, at maximum setting.	
⚠ EXT CLOCK Input		
Maximum Voltage Range		+5V to −5V (DC + peak AC).
Threshold		Two EXT CLOCK INPUT modes are available, TTL or ECL; for selection of either mode see Figure 1-11.
TTL Level		
Logic Zero	≤0.8 V.	
Logic One	≥2 V.	

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
EXT CLOCK Input (cont)		
Maximum Voltage Range (cont)		
ECL Level		
Logic Zero	≤-1.5 V.	
Logic One	≥-1.1 V.	
Input Impedance		The EXT CLOCK INPUT may be connected directly to the clock source, or through a 1X probe (TTL only). The EXT CLOCK Input is not compatible with a 10X probe.
TTL Level		Approximately 10K ohm in parallel with approximately 55 pF, terminated to +5 V.
ECL Level		Approximately 50 ohms, terminated to -2 V.
Minimum Input Slew Rate		
TTL Level		None.
ECL Level		100 mV/ns.
Pulse Width		
TTL Level	20 ns minimum.	Either pulse transition selected.
ECL Level	5 ns minimum.	Leading pulse transition selected.
	10 ns minimum.	Trailing pulse transition selected.
Set-up Time	10 ns minimum.	Time that level sensitive channels must be valid before EXT CLOCK INPUT transition.
Hold Time	10 ns minimum.	Time that level sensitive channels must remain valid after EXT CLOCK INPUT transition.
Channel EDGE Sensitivity		
Set-up Time, Channel to Channel	5 ns minimum.	Time that level sensitive portion of trigger function must be true before EDGE sensitive channel transition.
Hold Time, Channel to Channel	5 ns minimum.	Time that level sensitive portion of trigger function must remain true after EDGE sensitive channel transition.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
Channel EDGE Sensitivity (cont)		
Set-up Time, EDGE Sensitive Channel	10 ns minimum.	Time that level of EDGE sensitive channel must be stable before transition.
Hold Time, EDGE Sensitive Channel	5 ns minimum.	Time that level of EDGE sensitive channel must remain stable after transition.
Mainframe Trigger Output		
Amplitude, 1 MHz square wave		300 mV ±50 mV p-p differential, into A13 and B13 of main interface connection on left side of plug-in.
Centering, 1 MHz square wave		Mean value of square wave within one division of graticule center.
Risetime, 10% to 60%		2 ns ±1 ns.
Falltime, 90% to 40%		2 ns ±1ns.
⚠ TRIGGER OUT Connector		
Output Voltage		
Logic Zero	≤0.2 V into 50 ohm load.	
Logic One	≥0.8 V into 50 ohm load.	
Output Impedance		Approximately 50 ohms.
Toggle Frequency	125 MHz maximum.	A Mode or B Mode, with displayed input signal of 60mV p-p in ECL or 300mV p-p in TTL Logic Family, centered at threshold.
Propagation Delay		
Channel Input to Trigger Output		25 ns or less.
Differential Propagation Delay from Channel Input to Trigger Output through any Trigger Function		5 ns or less.
A THEN B Mode		
Time Between A and B	5 ns minimum.	Minimum set-up time from event A to event B to insure that trigger output occurs with event B.
Time From B to A	5 ns minimum.	Minimum time after event B to next event A to insure proper arming.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
TRIGGER OUT Connector (cont)		
Event Duration		Minimum time to insure proper arming and triggering.
Event A	5 ns minimum.	
Event B	5 ns minimum.	
Front-Panel A THEN B Gate Output		The front-panel A THEN B Gate Output is active only if selected and in the A THEN B mode; see Figure 1-15 for selection.
Voltage		
Logic Zero		≤0.2 V into 50 ohm load.
Logic One		≥0.8 V into 50 ohm load.
Output Impedance		Approximately 50 ohms.
Timing		
Time from Event A Recognition to Rising Edge of Gate	25 ns or less.	
Mainframe A THEN B Gate Output		Active only in A THEN B Mode.
Amplitude, 1 MHz Square Wave		300 mV ±50 mV p-p differential, into A13 and B13 of main interface connector on right side of plug-in.
Centering, 1 MHz Square Wave		Mean value of square wave within one division of graticule center.
Risetime, 10% to 60%		2 ns ±1 ns.
Falltime, 90% to 40%		2 ns ±1 ns.
Timing		
Time from Event A Recognition to Rising Edge (50% point) of Gate Output		Approximately 15 ns.
Time from Event B Recognition to Falling Edge (50% point) of Gate Output		Approximately 15 ns.

TABLE 1-2 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
TRIGGER (CONT)		
Mainframe A THEN B Gate Output (cont)		
Pulse Width		
Gate Output width, Measured at the 50% Points	Greater than the time between event A and event B by 5 ns ±2 ns.	
RESET Input		
Maximum Input Voltage		+5 V to −5 V (DC + peak AC).
Input Impedance		Approximately 50 ohms.
Levels		
Logic Zero	≤0.2 V.	
Logic One	≥0.8 V.	
Pulse Width	100 ns minimum.	
Timing, Post-RESET Inhibit Time to Next Trigger	10 ns minimum.	Time from falling edge of RESET to next recognizable event.
Response Time	RESET pulse must lead or be coincident with event recognition, to inhibit trigger output. Event recognition must lead the RESET pulse by 10 ns to guarantee trigger output.	
BATTERY BACK-UP		
Ni-Cad Battery (3.75 V)		Provides power to preserve front-panel control status a minimum of 200 hours while main power is off. Battery requires about 24 hours to fully charge from discharged condition.

TABLE 1-3
Environmental Characteristics

Characteristics	Information
Temperature (External Ambient Mainframe)	
Temperature	
Operating	0 to +40° C in 7403N/7603 without fan (fan kit is available). 0 to +50° C in other 7000-series mainframes.
Storage	-55° C to +75° C.
Altitude	
Operating	15,000 feet (4.6 Km).
Nonoperating	To 50,000 feet (15.2 Km).
EMC	Tested to MIL-T-28800C, MIL-STD-461A (excluding RE-01).
Vibration	
Operating and Nonoperating	Tested to MIL-T-28800C, SECT. 4.5.5.3.1 Type III, Class 5.
Shock	Tested to MIL-T-28800C, SECT. 4.5.5.4.1 Type III, Class 5.
Bench Handling	Tested to MIL-T-28800C, SECT. 4.5.5.4.4 Type III, Class 5.
Transportation	National Safe Transit Association, Preshipment Test Procedure.
Vibration and Bounce (packaged product)	NSTA, PROJECT 1 A-B-1.
Drop (packaged product)	NSTA, PROJECT 1 A-B-2.

TABLE 1-4
Physical Characteristics

Characteristics	Information
Net Weight	Approximately 6.2 lb, 2.8 Kg.
Dimensions	See dimensional drawing Figure 1-2.

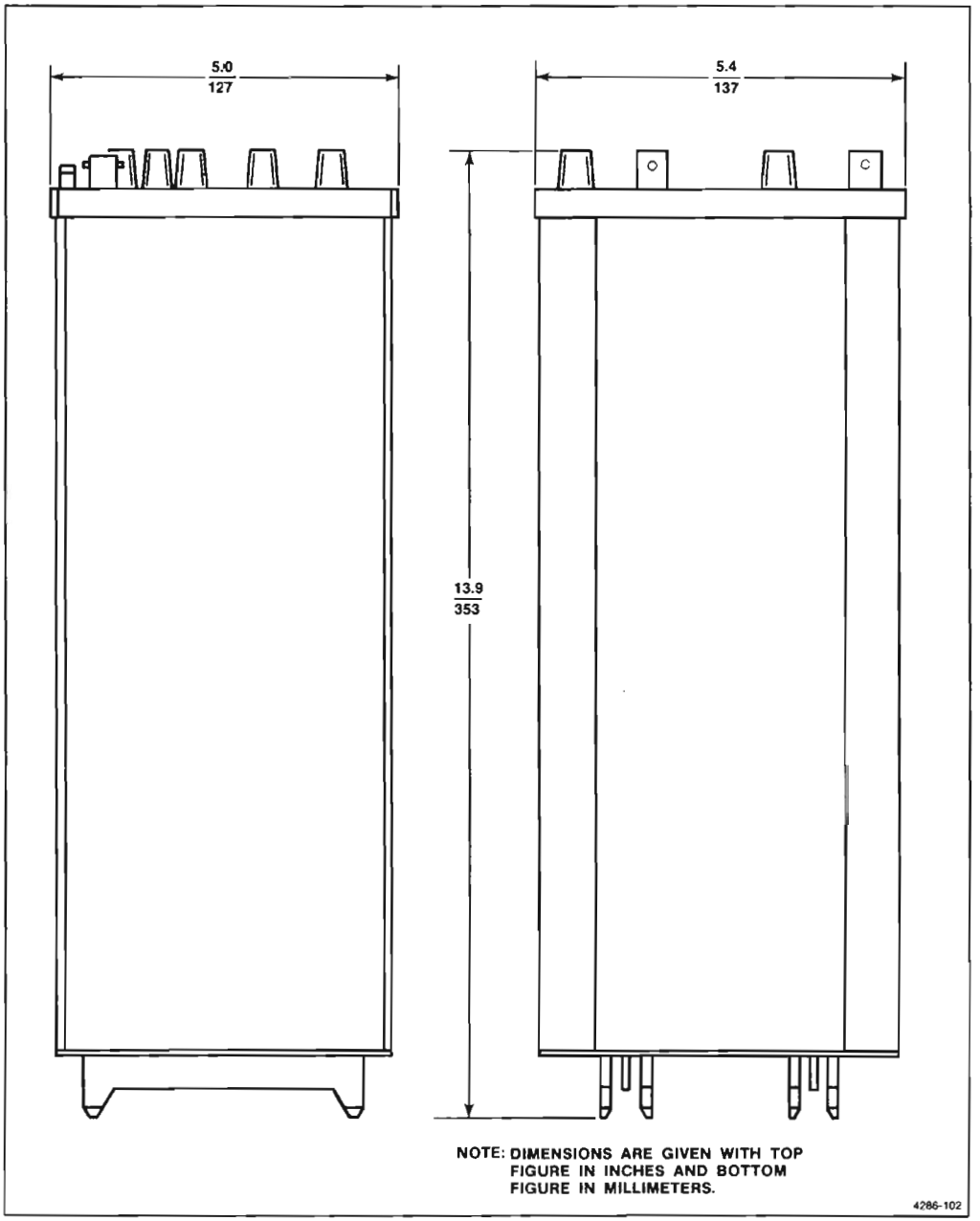


Figure 1-2. 7A42 dimensional drawing.

STANDARD ACCESSORIES

1 ea	Operators Manual
1 ea	*Service Manual (Volume 1)*
1 ea	Service Manual (Volume 2)
1 ea	SMB to BNC Cable

For part numbers, refer to the tabbed Accessories page at the rear of this manual.

OPTIONAL ACCESSORIES (not included)

The following accessories have been selected from our catalog specifically for your instrument. They are listed as a convenience to help you meet your measurement needs. For detailed information and prices, refer to a Tektronix Products Catalog or contact your local Tektronix Field Representatives.

PROBES

The P6131 10X passive probe (10 Megohm, 10.8 pF) has a 1.3 meter cable, a narrow barrel and variety of probe tips (hooks, IC grabbers, and ground leads) available.

The P6230 is an active 450 ohm variable bias/offset probe, which is an excellent ECL logic probe due to its low capacitances and minimal loading (because of the variable bias/offset feature). The 7A42's PROBE OFFSET feature is designed to work with the P6230. The P6131 accessories will also fit the P6230. (*See ECL Probing Techniques in the* Application section of the 7A42 Operators manual.)

Passive probes such as the P6131, *require low-frequency compensation into the inputs of the 7A42*, as with any vertical amplifier. The mainframe calibrator provides a signal suitable for making this adjustment. For optimum high-frequency performance, the probe high-frequency compensation should also be adjusted directly into the 7A42 inputs. See the *probe manual for instructions to perform this adjustment.*

OPERATING INSTRUCTIONS

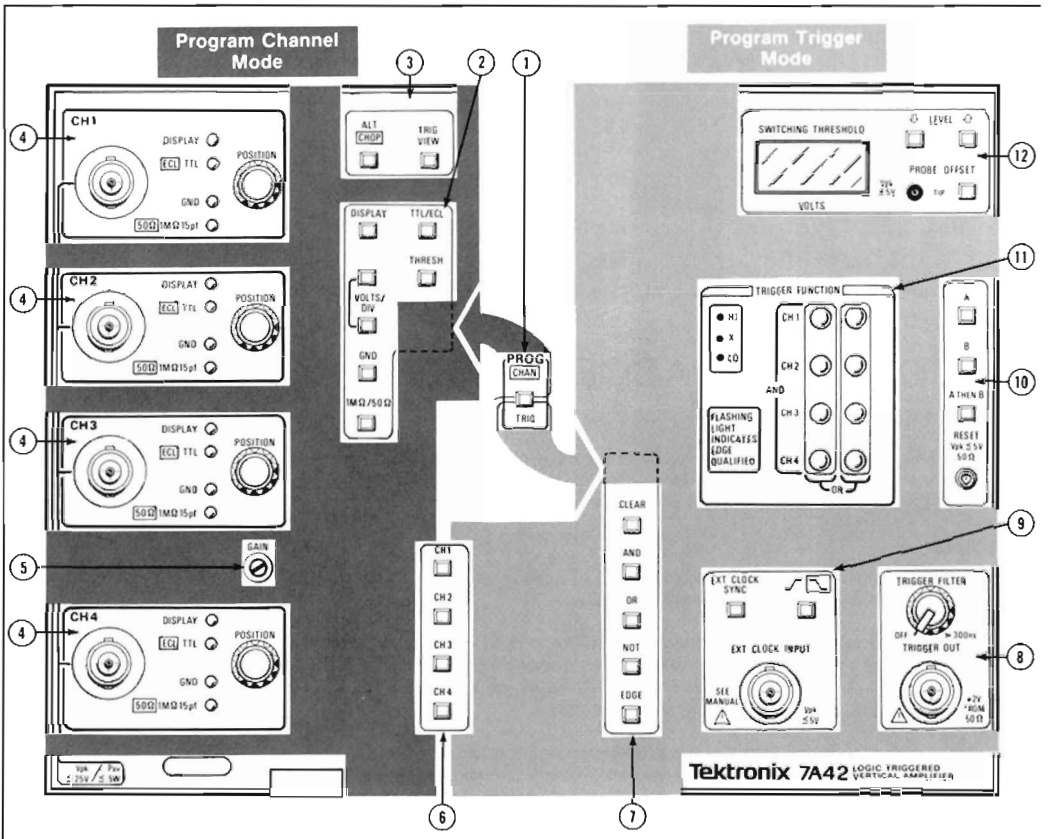
This section will familiarize you with the capabilities and operation of the 7A42. A thorough understanding of this information will remove later uncertainty when operating your 7A42.

OPERATION

For operation, your 7A42 Logic Triggered Vertical Amplifier must be properly installed in a Tektronix 7000-series mainframe. Installation is explained in the General Information section of this manual.

CONTROLS, CONNECTORS, AND INDICATORS

All controls, connectors, and indicators required for the normal operation of the 7A42 Logic Triggered Vertical Amplifer unit are located on the front panel. Figure 1-3 shows an exploded front panel and gives a brief functional description of each control, connector, and indicator.



4286-103A

(1) **PROG CHAN or TRIG**—Pushbutton selects one of two modes; when light is on, those controls associated with programming the TRIGGER FUNCTION are operable (see **6**, **7** and **10**). When light is out, those controls associated with CH1, CH2, CH3, CH4 setup conditions are operable (see **6** and **2**).

(2) **DISPLAY**—Pushbutton turns on or off the display of the incoming signal selected by controls listed under number **6**[1]. Nondisplayed channels may still contribute to the TRIGGER FUNCTION.

VOLTS/DIV—Two pushbutton switches increase or decrease vertical deflection factor of the channel selected by controls listed under number **6**[1].

GND—Pushbutton grounds the selected channel amplifier input and disconnects the incoming signal, of the channel selected by controls listed under number **6**[1].

1MΩ/50Ω—Pushbutton switch selects input impedance to be either one megohm or 50 ohms of the channel selected by controls listed under number **6**[1].

TTL/ECL—Pushbutton switch selects the deflection factor range and preset threshold to be compatible with either TTL or ECL logic families of the channel selected by controls listed under number **6**[1].

THRESH—Pushbutton switch activates the LEVEL pushbuttons and SWITCHING THRESHOLD VOLTS display, allowing operator to set the threshold voltage of the channel selected by controls listed under number **6**[1].

Figure 1-3. 7A42 controls, connectors, and indicators.

(3) **ALT/CHOP**—Pushbutton switch, determines whether the displayed channel(s) are displayed alternately, after each sweep of the time base, or are displayed simultaneously in a chopped mode.

TRIG VIEW—Pushbutton to display TRIGGER FUNCTION output signal or EXT CLOCK signal on crt.

(4) The following controls, connectors, and indicators are common to CH1, CH2, CH3, and CH4.

Input Connector—Bnc for signal connection.

POSITION—Vertically positions the incoming signal. Clockwise rotation moves displayed trace upward.

DISPLAY—When DISPLAY indicator light is on, channel is selected for display.

ECL/TTL—When indicator light is on the preset threshold voltage and range of deflection factors are compatible with TTL logic levels; when off they are compatible with ECL Logic levels.

GND—When indicator light is on, the amplifier input is grounded and the input signal is electrically disconnected from the amplifier.

50Ω/1MΩ—When indicator light is on, the input impedance is one megohm, 15 picofarads; when off, input impedance is 50Ω.

(5) **GAIN**—Screwdriver control adjusts display gain of channels CH1, CH2, CH3, and CH4.

(6) **CH1, CH2, CH3, and CH4**—Operate in either the PROG CHAN or the PROG TRIG modes. In the PROG CHAN mode the self-cancelling pushbutton switches determine which channel is affected by the controls listed under number **2**[1]. In the PROG TRIG mode the CH1 through CH4 pushbutton switches determine which channel is programmed into the TRIGGER FUNCTION, as selected by the controls listed under number **10**[2].

(7) **CLEAR**—Pushbutton switch clears the programmed TRIGGER FUNCTION selected by the controls listed under **10**[2].

AND, OR, NOT—Pushbutton switches used with controls listed under number **6** to program the TRIGGER FUNCTION selected by the controls listed under **10**[2].

EDGE—Pushbutton selects edge sensitivity for the channel being programmed into the TRIGGER FUNCTION[2].

(8) **TRIGGER FILTER**—Variable control sets minimum duration of TRIGGER FUNCTION output before it is sent to the time base or TRIGGER OUTput connector.

TRIGGER OUT—Provides a front-panel output of the trigger signal.

(9) **EXT CLOCK INPUT**—Provides external clock input for synchronizing triggers to an external clock signal source (EXT CLOCK SYNC light must be on).

EXT CLOCK SYNC—Pushbutton switch allows an external clock to qualify the TRIGGER FUNCTION.

—Pushbutton switch selects positive going or negative going edge of the external clock signal which qualifies TRIGGER FUNCTION.

(10) **A, B, A THEN B**—Two independent TRIGGER FUNCTION programs are available (A and B). The A THEN B is a nested combination where A must occur to arm triggering before B is allowed to produce a trigger output.

RESET—External input to disable the TRIGGER FUNCTION output and disarm the A THEN B nested triggering; no arming or triggering can occur while a high level is applied.

(11) **TRIGGER FUNCTION**—LED display indicates the Boolean function which will produce a TRIGGER FUNCTION output. Number **6**, **7**, and **10** controls are used to program TRIGGER FUNCTION lights[2].

(12) **SWITCHING THRESHOLD VOLTS**—LED display indicates threshold voltage of the channel selected by controls listed under number **6** or displays probe offset[3].

LEVEL—Two pushbutton switches set threshold voltage of channel selected by the controls listed under number **6**[3].

PROBE OFFSET—Measures offset voltage of probe connected to the channel selected by controls listed under number **6**[3].

[1]**PROG CHAN/TRIG must be set to CHAN.**
[2]**PROG CHAN/TRIG must be set to TRIG.**
[3]***PROG CHAN/TRIG must be set to CHAN, and* THRESH must be active.**

4286-103B

Figure 1-3 (cont). 7A42 controls, connectors, and indicators.

DETAILED OPERATING INFORMATION

Detailed information concerning the controls and operation of the 7A42 is given in the following pages.

SELF-TEST

When power is applied to the 7A42 an internal self-test sequence is automatically performed. While the self-test sequence is in progress the mainframe crt readout shows 7A42 TEST BUSY, see Figure 1-4. When the self-test sequence is finished, the message 7A42 TEST COMPLETE appears momentarily on the mainframe oscilloscope crt, as shown in Figure 1-5. During the self-test sequence some of the front-panel pushbuttons and all of the indicators are illuminated.

The SWITCHING THESHOLD VOLTS indicator will display 8.8.8.8. during the first part of the self-test sequence to verify that all segments operate. If there are no self test failures, the Firmware Version number will then be displayed for a few seconds before the self test is completed.

Self-test failures are indicated by three different methods: 1. on the mainframe crt, 2. on the 7A42 SWITCHING THRESHOLD display, and 3. on the TRIGGER FUNCTION indicators. Figure 1-6 illustrates a typical self-test failure, indicated by the three display methods. Displaying the self-test failure messages in three different ways increases the chance that the failure message will be displayed, even if the failure affects the operation of two of the three display methods.

The TRIGGER FUNCTION display indicates a self-test failure with the color red and self-test passed with the color green. If a failure occurs, the self-test sequence will stop.

The SWITCHING THRESHOLD VOLTS indicator and mainframe crt readout display indicate a self-test failure with a numeric code. All of the self-test code numbers are listed in Table 1-5, along with the nature of the failure and an explanation of the severity of the failure. The severity information is helpful in determining if the 7A42 can still be used for the intended purpose or whether repair is necessary. To continue the self-test sequence, press any of the 7A42 front-panel pushbuttons.

NOTE

Before the 7A42 Self Test feature can verify that the 7A42 readout circuitry is operating properly, mainframe crt readout system must be set to the "Freerun" (non-Gated) mode.

FRONT-PANEL INITIALIZATION

While getting acquainted with the 7A42, it might be desirable to begin operation with the front-panel controls set to a known state (initialized). The front panel will initialize to the control settings listed in Table 1-6. To initialize the 7A42 front-panel controls to a known state, perform the procedure of Figure 1-7.

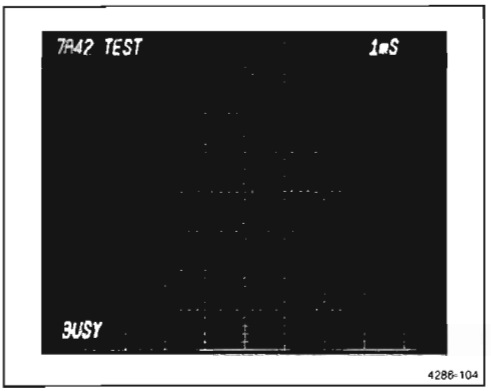


Figure 1-4. Self-test in progress.

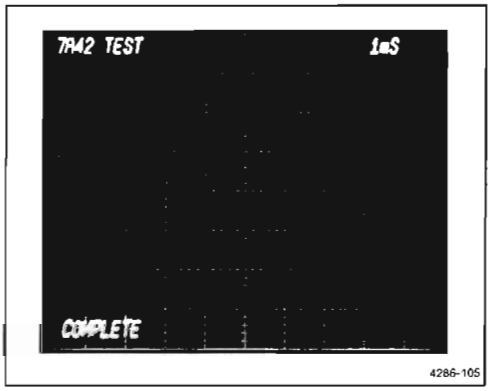
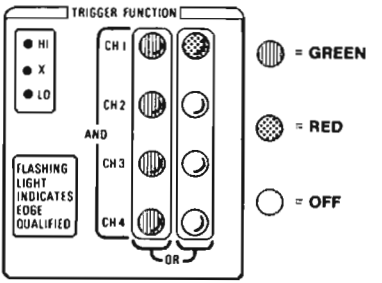
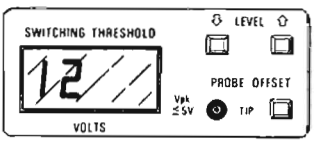
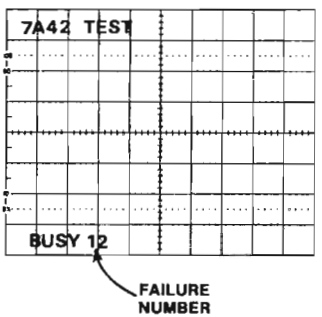


Figure 1-5. Self-test finished.

DISPLAY MEDIA	TYPICAL MEDIA
TRIGGER FUNCTION LEDS GREEN = TEST PASSED RED = TEST FAILED	
SWITCHING THRESHOLD VOLTAGE MONITOR (Numeric Display)	
CRT READOUT (Numeric Display) NOTE: During some self tests, the crt readout is unstable; this condition is normal.	

4286-106

Figure 1-6. Typical self-test failure display.

BATTERY BACKUP

The 7A42 battery backup feature restores the 7A42 front-panel control settings to the same settings that were present when the power was turned off.

The battery-backup feature can be defeated if so desired. If the battery-backup feature has been disabled, the 7A42 front-panel control settings will return, at power up, to the settings listed in Table 1-6. To disable the battery back up feature disconnect J747 from the MPU Board, see Figure 1-8.

OPERATOR MESSAGES

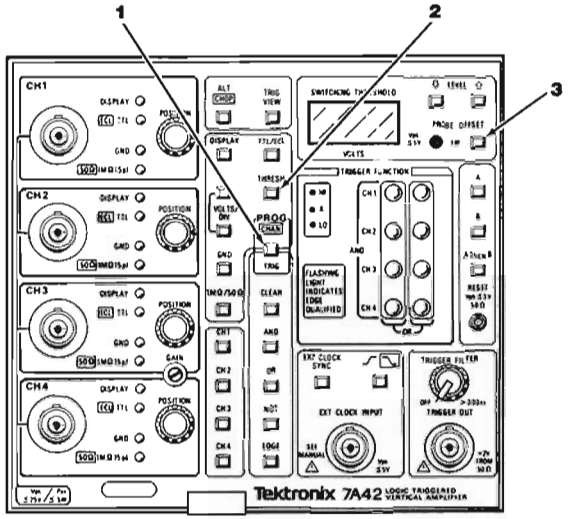
Operator Messages occur under several operating conditions and are accompanied by an audible beep. When they occur, the mainframe readout will display a mnemonic at the top of the crt and a number code at the bottom. The mnemonic is an abbreviated explanation of the operating condition which caused the message to be displayed. The code number references the message to Table 1-7 which gives a more complete explanation of the operating condition.

TABLE 1-5
7A42 Self-Test Failure Messages

TRIGGER FUNCTION (LED display)		SWITCHING THRESHOLD VOLTS and crt readout display		Severity of failure; functional usability of instrument
Indication	**Test**	**Indication**	**Test**	
CH1, first column	ROM	01 to 04	ROM	Possible loss of front-panel control; repair before use.
CH2, first column.	RAM	05 to 06	RAM	
CH3, first column.	Microprocessor control logic.	07 to 09	Microprocessor control logic.	
CH4, first column.	PROBE OFFSET	10	PROBE OFFSET	Avoid use of probe offset feature. 7A42 otherwise fully functional. Repair when convenient.
CH1, second column.	Crt display and readout	11	Crt trace display.	Channels 1 through 4 may not be displayable. Repair before use.
		12,13	Crt readout.	Crt readout may not be functioning. Cause could be lack of mainframe readout. Repair when convenient.
CH2, second column.	Trigger	14	Trigger control.	Some or all trigger functions may not be operational. Repair before use.
		15	Trigger logic.	Some channels may not trigger properly. Repair before use.
		23	Boolean logic.	Some trigger functions may not be operational. Repair before use.
		26	A THEN B	Avoid use of A THEN B mode. Repair when convenient.
CH3, second column.	Edge detectors.	34	Edge detectors.	Avoid use of Edge-qualified triggering mode and external clock. Repair when convenient.
CH4, second column.	EXT CLOCK	70	EXT CLOCK	Avoid use of external clock. Repair when convenient.

NOTE

For more detailed information, see Table 3-6, extended test failure messages, in this manual.



a. Set the PROG pushbutton **1** to the CHAN mode (pushbutton light out).

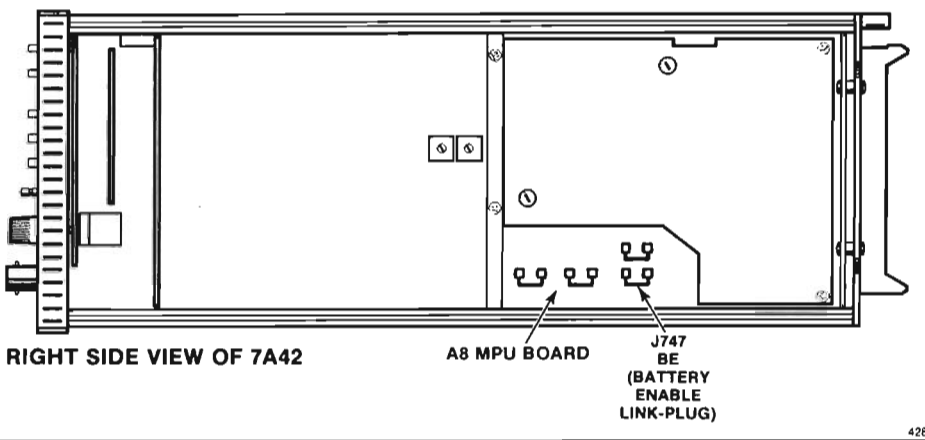
b. Press the THRESH pushbutton **2** so that the pushbutton light is on (Threshold Mode).

c. Press the PROBE OFFSET pushbutton **3** until it illuminates red (Acquire Mode).

d. Turn the oscilloscope mainframe Power off and then on again.

4286-113

Figure 1-7. Initialization of the 7A42 front-panel controls.



4286-406

Figure 1-8. Location of J747 Battery Enable link plug.

NOTE

The audible beep can be turned off, by installing a link plug on P730. See Figure 3-8 in the Maintenance section of this manual for the location of P730.

SIGNAL CONNECTIONS

Generally, probes offer the most convenient means of connecting input signals to the instrument. Probes are shielded to prevent electromagnetic interference. The

TABLE 1-6
7A42 Front-Panel Control Settings When Initialized

Control	Control Setting
PROG CHAN/TRIG	Program Channel (light off)
Programmable Channel	CH1 only
DISPLAY	CH1 only
VOLTS/DIV (CH1 through CH4)	Preset to 0.5 V/Div at bnc input
TTL/ECL (CH1 through CH4)	TTL
GND (CH1 through CH4)	Ungrounded
1MΩ/50Ω (CH1 through CH4)	1MΩ
ALT/CHOP	ALT
TRIG VIEW	Off
SWITCHING THRESHOLD voltage (CH1 though CH4)	Preset TTL (+1.4V); display off
THRESH	Off
PROBE OFFSET	Off
A TRIGGER FUNCTION	CH1 (HI)
B TRIGGER FUNCTION	Cleared
TRIGGER MODE TRIGGER FUNCTION A THEN B	 A Off
EXT CLK SYNC	Off
External Clock Slope	Off

NOTE

Controls not listed above are not preset.

TABLE 1-7
7A42 Operator Message Summary

Code	Mnemonic	Description and Corrective Action
1	OVERLOAD	A channel input is overloaded. Remove the overvoltage and unground the channels to continue operation.
2	OFFSET ACQ	A key was pressed while Probe Offset acquisition was in progress. Push PROBE OFFSET once to lock in acquired value, or twice to turn PROBE OFFSET off, before continuing operation.

TABLE 1-7 (CONT)
7A42 Operator Message Summary

Code	Mnemonic	Description and Corrective Action
3	PUSH PROG	Key(s) pressed is/are active only in PROG CHAN mode. To use key, first press PROG CHAN.
4	PUSH PROG	Key(s) pressed is/are active only in PROG TRIG mode. To use key, first press PROG TRIG.
5	AND/OR REQ	While programming a trigger function, a CH1, CH2, CH3, CH4, NOT, or EDGE was pressed when an AND or an OR key was expected.
6	CH KEY REQ	While programming a trigger function, two Boolean operator keys (AND or OR) were pressed without pressing a channel key (CH1, CH2, CH3, or CH4) in between. Channel keys and Boolean operator keys should be pressed alternately, e.g., CH1 AND NOT CH2 OR CH3 EDGE.
7	OR IS FULL	The OR key was pressed again. Only one TRIGGER FUNCTION OR is allowed.
8	EXTCLK ON	The EDGE key was pressed while in the EXT CLOCK SYNC mode. The selection of an EDGE sensitive channel and the EXT CLOCK SYNC mode are mutually exclusive. If EDGE sensitivity is desired, first turn off the EXT CLOCK SYNC mode.
9	EXTCLK REQ	The EXT CLOCK slope key was pressed when the EXT CLOCK SYNC button was turned off. The EXT CLOCK SYNC slope key is operational only when the EXT CLOCK SYNC button is turned on.
10	EDGE IS ON	The EXT CLOCK SYNC key was pressed when one of the trigger functions (either A, B, or both) already have an EDGE sensitive channel. Channel EDGE sensitivity and EXT CLOCK are mutually exclusive. If EXT CLOCK SYNC operation is desired, first CLEAR the channel EDGE sensitive trigger function.
11	THRESH REQ	Either a LEVEL key or the PROBE OFFSET key was pressed without pressing the THRESH key first. The THRESH key must be lit to change a threshold level or acquire a probe offset.

TABLE 1-7 (CONT)
7A42 Operator Message Summary

Code	Mnemonic	Description and Corrective Action
12	NO FUNC A	The A THEN B key was pressed without having programmed function A; or while in A THEN B mode function A was CLEARed. Both trigger functions (A and B) must be programmed for proper A THEN B operation. Program function A; then proceed.
13	NO FUNC B	The A THEN B button was pressed without having programmed function B; or while in A THEN B mode function B was CLEARed. Both trigger functions (A and B) must be programmed for proper A THEN B operation. Program function B; then continue.

WARNING BEEPS: Although no messages are displayed, short warning beeps are issued to indicate "out of range." A beep will sound when the VOLTS/DIV keys are pushed beyond the available selections or when the variable threshold level reaches its limits.

NOTE

The audible beep can be turned off, by installing a link plug on P730. See Figure 3-8 in the Maintenance section of this manual for location of P730.

10X probe offers a high input impedance to minimize circuit loading when measurements are made; signal amplitude is attenuated by a factor of 10 by the probe, so the scale-factor readout is switched to indicate the correct scale factor.

The limited TTL/ECL VOLTS/DIV ranges require that attenuation be used to obtain useful signal levels at the 7A42 channel inputs. Ten times probes are recommended on the channel inputs to attenuate TTL and ECL signals; otherwise 10X attenuators should be used. When 10X probes are used the VOLTS/DIV and SWITCHING THRESHOLD are automatically compensated to reflect the characteristics at the probe tip.

RECOMMENDED PROBES

The Tektronix P6131 and P6230 probes are recommended for use with the 7A42. The Tektronix P6131 is a 10X passive probe with 10 megohm at 10.8 picofarads. A variety of probe tips (hooks, IC grabber and ground leads) are available with this probe.

The Tektronix P6230 is an active 450 ohm bias/offset probe which is especially useful with ECL logic circuits due to its minimal circuit loading characteristics. For information on how to use the P6230 probe, refer to the Application section in the 7A42 Operators manual.

Probe Compensation

Maladjustment of probe compensation is one source of measurement error. Most 10X passive high impedance probes are equipped with a compensation adjustment. To ensure optimum measurement accuracy, always compensate the oscilloscope probe before making measurements. Refer to the probe instruction manual for probe adjustment procedure.

For optimum 7A42/P6131 performance the P6131 should be high-frequency compensated while connected to the 7A42; see the P6131 probe manual for high-frequency compensation adjustment procedure.

COAXIAL CABLES

Although the 7A42 input channel VOLT/DIV ranges are intended to be used with 10X probes, coaxial cables may be used for signal connections. When coaxial cables are used a 10X attenuator must be used to reduce TTL/ECL signals to usable levels. When 10X attenuators are used the VOLTS/DIV and SWITCHING THRESHOLD readings are not automatically compensated and will indicate values a factor of 10 lower than actual.

Cables also may be used to connect signals to the input connectors, but they may have considerable effect on the accuracy of the displayed waveform. To maintain the original frequency characteristics of an applied signal, use only low-loss, 50 ohm, high-quality coaxial cable. Cables should be terminated into 50 ohms. The 7A42 has an internal 50 ohm termination for each input channel which can be selected from the front-panel.

CRT READOUT

Figures 1-9 and 1-10 show the 7A42 scale factor readout location. Figure 1-10 was taken with X10 probes attached to the channel inputs. Figure 1-9 was taken without probes attached to the channel inputs and without changing the channel VOLTS/DIV settings from those of Figure 1-10.

NOTE

Improper crt readout operation may be caused by the 7A42-7854 mode being selected when the 7A42 is operated in other 7000-series mainframes. See Figure 3-7 in the Maintenance section of this manual to determine if the 7A42-7854 mode is selected.

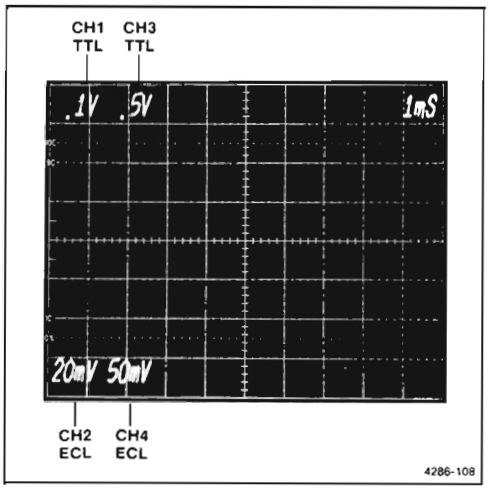


Figure 1-9. Channel readout display.

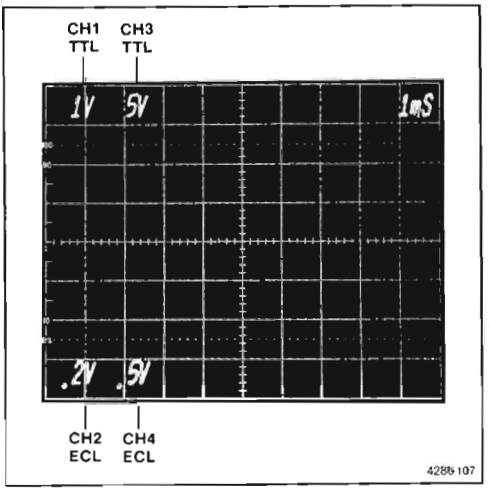


Figure 1-10. Channel readout display with 10X probes attached to inputs of CH1, CH2, CH3, and CH4.

POSITION

A POSITION control is provided for each of the four channels. The control vertically positions the displayed trace on the host mainframe crt (clockwise rotation moves the trace upward).

GAIN

This screwdriver control adjusts the 7A42 display output (of all four channels) to match the vertical gain tolerance of any Tektronix 7000-series mainframe.

STATUS INDICATORS (CH1, CH2, CH3, CH4)

Each channel has four status indicators (DISPLAY, ECL/TTL, GND and 50Ω/1MΩ). These indicators show the status of each individual channel. A description of each indicator is given below.

DISPLAY

When the DISPLAY indicator is lit, the associated channel is displayed on the mainframe crt. If the indicator is extinguished, any signal applied to the channel input will still be routed to the TRIGGER FUNCTION circuitry, providing the GND indicator is not lit.

ECL/TTL

When the ECL/TTL indicator is lit, the channel threshold voltage range and deflection factors match the voltage levels and signal amplitudes of the TTL logic family. When the indicator is extinguished the threshold voltage range and deflection factors are in accord with the ECL logic family.

GND

When the GND indicator is lit, the input to the selected channel amplifier is grounded and the signal path from the front-panel bnc connector to the amplifier is open. An external signal applied to this channel is not terminated (it is open). Grounded channel traces are still displayed to enable the ground reference position to be established.

50Ω/1MΩ

When the 50Ω/1MΩ indicator is lit, the input impedance of the associated channel is one megohm. When the indicator is extinguished the input impedance is 50 ohms.

ALT/CHOP

The ALT/CHOP pushbutton selects either alternate or chopped as the display mode (for all channels). When the ALT/CHOP indicator is lit, the channels selected for display are alternately displayed on the mainframe oscilloscope crt after each sweep of the time base. When the ALT/CHOP indicator is extinguished, the display is electronically switched between channels at about a one-megahertz rate. In general, the ALT mode provides the best display at sweep rates of 100

microseconds/division and faster while the CHOP mode provides the best display at sweep rates slower than about 200 microseconds/division or whenever multiple single-shot signals are to be photographed.

TRIGGER FUNCTION

The two-color TRIGGER FUNCTION indicators display the Boolean trigger function. The color red indicates a HI (logic 1, or higher than threshold voltage) condition. Green indicates LO (logic Ø, or lower than threshold voltage) condition. An indicator that is not lit represents the X (don't care) condition. A red flashing or green flashing indicator signifies that the channel is edge sensitive (rising, red; or falling, green) as opposed to being level sensitive.

The TRIGGER FUNCTION indicators are arranged in two columns of four each. Each column represents a logical AND function, (a Boolean product of the four input channels). After the AND functions are performed, the columns are ORed together to form the complete Boolean TRIGGER FUNCTION. Thus each TRIGGER FUNCTION is equivalent to two four-bit word recognizers ORed together.

There is one exception to this convention. While an extinguished indicator represents the "don't care" condition, an entire column that is not lit is considered to be inactive. If an unlit column were interpreted as a don't care, that column ORed with any other column would always be true.

A TRIGGER FUNCTION AND B TRIGGER FUNCTION

There are two separate TRIGGER FUNCTIONS available, A and B. They are identical; either may be used. One pushbutton will always be lit to indicate which function is displayed by the TRIGGER FUNCTION indicators and therefore, the function that will produce the trigger output. The other function is stored in memory and may be called up by pressing that pushbutton. The programming or clearing of the function displayed will not affect the other function.

A THEN B NESTED TRIGGERING

One level of nested triggering is available when this mode is used. The trigger output to the mainframe time base occurs only after the triggering is first armed by the occurrence of function A. The trigger output then takes place with the next occurrence of function B. After this cycle, the 7A42 will begin to look for another occurrence of function A, to begin the next nested trigger cycle.

TRIG VIEW

The TRIG VIEW trace provides a visible replica of the trigger output signal as it is processed by the 7A42 according to the programmed TRIGGER FUNCTION. This trigger signal is also sent to the time base. When the EXT CLOCK SYNC pushbutton switch is lit, the TRIG VIEW trace displays the external clock input signal.

The TRIG VIEW trace is normally located near the bottom of the crt display. There is an internal provision for repositioning the trace; refer to the Performance Check and Adjustment section of this manual, for a procedure to reposition the TRIG VIEW trace. If all of the channel displays are turned off the TRIG VIEW trace will be on and cannot be turned off.

TRIGGER FILTER

The TRIGGER FILTER control provides a selectable amount of delay between the time that the TRIGGER FUNCTION is recognized as true, and the time that the Trigger Output is sent to the time base to trigger the sweep. Thus the TRIGGER FILTER will inhibit trigger events that are shorter in duration than those for which the control is set. A longer trigger event will pass through the TRIGGER FILTER and can cause a triggered sweep as well as a signal at the front-panel TRIG OUT connector. The TRIGGER FILTER control can be used only with level-sensitive trigger functions (it is inactive with any TRIGGER FUNCTION that contains an edge-sensitive channel). The TRIGGER FILTER operates independently on TRIGGER FUNCTION A and TRIGGER FUNCTION B. In the A THEN B mode, the TRIGGER FILTER may be inactive on function A because of an edge sensitive channel, while at the same time be active on function B. The TRIGGER FILTER is not active when in the EXT CLOCK SYNC mode or when the control is in the counterclockwise detent (OFF) position.

EXT CLOCK SYNC

The EXT CLK SYNC pushbutton allows the 7A42 to be used in a synchronous mode of operation. The trigger output (in either A, B, or A THEN B mode) will occur only on the selected edge of an external clock signal, providing the TRIGGER FUNCTION is also true at that time. If TRIG VIEW is selected, a replica of the external clock input signal having a fixed amplitude and position will be displayed on the TRIG VIEW trace.

SLOPE SELECT

Either the rising or falling edge of an external clock signal can be used to qualify the TRIGGER FUNCTION. When the Slope Select pushbutton is lit the TRIGGER FUNCTION is qualified on the rising transition of the external clock signal.

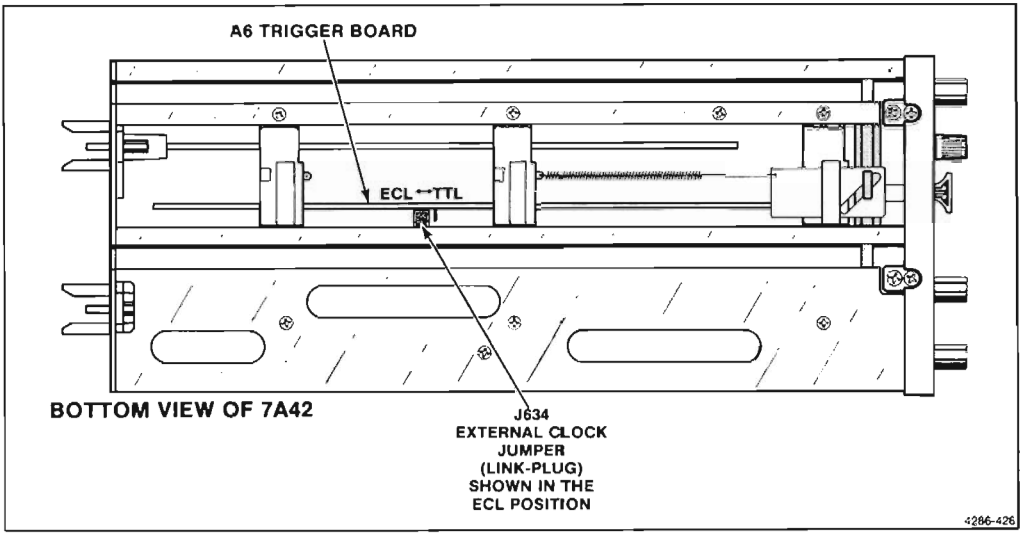


Figure 1-11. Location of J634, External Clock Jumper, on A6 Trigger Board.

EXT CLOCK INPUT

The EXT CLOCK INPUT is directly compatible with either TTL or ECL logic families. The instrument is shipped from the factory in the TTL mode.

For selection of the ECL or TTL mode see Figure 1-11. The EXT CLOCK INPUT can be used with a 1X probe in TTL mode, or can be directly connected to the logic circuit in either TTL or ECL mode; 10X probes should not be used with this input.

RESET INPUT

The RESET INPUT allows the operator to apply a signal to inhibit the trigger output. Applying a positive 0.8 volt level to the RESET input will prevent the programmed TRIGGER FUNCTION from being recognized as true. The result is that no trigger output signal will occur until the reset voltage is removed.

If the A THEN B nested-trigger mode is selected, TRIGGER FUNCTION A has occurred, and TRIGGER FUNCTION B has not occurred; the RESET signal will reset function A (the armed condition) as well as inhibit function B. Therefore, the RESET input can be used to enhance the A THEN B nested trigger operation by providing an "A THEN B unless RESET" feature.

TRIGGER OUT

The TRIGGER OUT bnc connector is a trigger output signal source. This signal can be used to synchronize other equipment with the 7A42 TRIGGER FUNCTION. The output of the TRIGGER FUNCTION is determined by the setting of the A, B, or A THEN B pushbuttons, the programming of the A and B functions, and the channel input signals. Timing diagrams for a typical set of conditions are shown in Figures 1-12 and 1-13.

Two modes of operation can be selected for the TRIGGER Out connector; Normal, and A THEN B Gate. In Normal Mode, the A THEN B Trigger Out is a pulse, regardless of the duration of Trigger Function B. A typical timing diagram depicting the Normal and A THEN B Gate modes, is shown in Figure 1-14. For selection of either mode see Figure 1-15. The TRIGGER OUT signal levels are compatible with the RESET input levels.

PROG CHAN/TRIG

The PROG CHAN/TRIG pushbutton selects one of two modes, PROG CHAN (program channel) or PROG TRIG (program trigger). In the PROG CHAN mode the DISPLAY, VOLTS/DIV, GND, 1MΩ/50Ω, TTL/ECL, and THRESH pushbuttons are activated. These controls are used with the CH1, CH2, CH3 and CH4 pushbuttons to individually set the channel status. In the PROG TRIG mode CLEAR, AND, OR, NOT, and EDGE pushbutton controls are activated and are used with the CH1, CH2, CH3, and CH4 pushbutton controls to program a Boolean equation into the A TRIGGER FUNCTION or B TRIGGER FUNCTION. The following text discusses first the PROG CHAN controls and then the PROG TRIG controls.

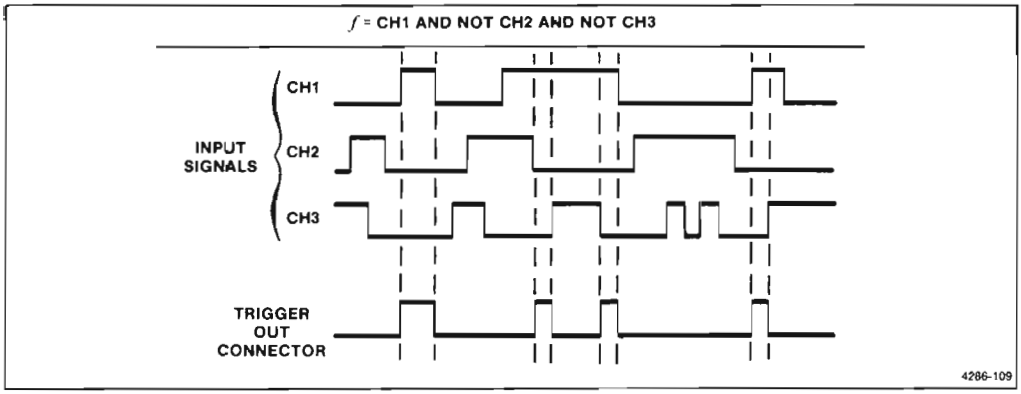


Figure 1-12. Timing diagram showing the relationship of the TRIGGER OUT waveform to the input signals.

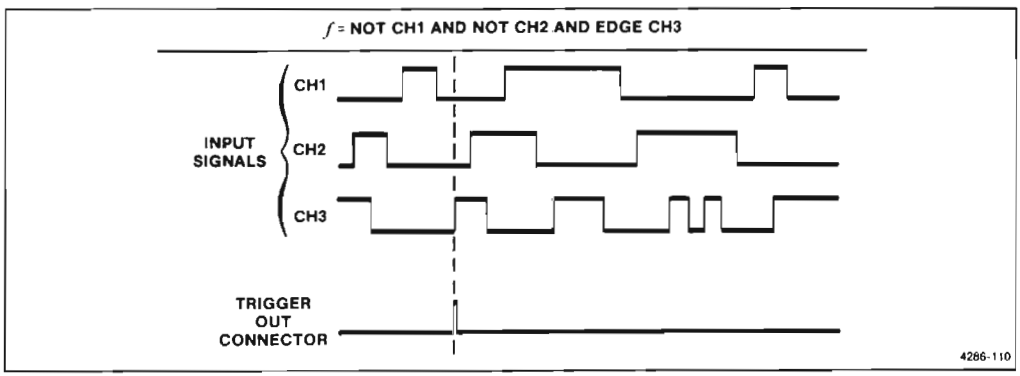


Figure 1-13. Timing diagram depicting the TRIGGER OUT waveform, as a result of the TRIGGER FUNCTION reacting to the input signals.

PROGRAM CHANNEL MODE

The TTL/ECL, VOLTS/DIV, GND, 1MΩ/50Ω, and DISPLAY, controls are active in the PROG CHAN mode. These controls are used with the CH1, CH2, CH3, and CH4 pushbuttons to set the status of each channel.

CH1, CH2, CH3, CH4. In the PROG CHAN mode the CH1, CH2, CH3, and CH4 pushbuttons are used to select and indicate the channel which will respond to the TTL/ECL, VOLTS/DIV, GND, 1MΩ/50Ω, DISPLAY and THRESH pushbutton controls.

DISPLAY. The DISPLAY pushbutton turns the selected channel display on or off. In the off position the trace is removed from the crt display. However, the signal applied to that channel is still routed to the TRIGGER FUNCTION circuitry, providing the channel GND indicator is not lit.

TTL/ECL. The TTL/ECL pushbutton offers a threshold range and selection of display sensitivities appropriate for either TTL or ECL logic families.

VOLTS/DIV. The VOLTS/DIV pushbuttons set the scale factor of the selected channel. The scale factor is displayed on the mainframe crt readout; refer to CRT Readout in this section. Three sensitivities are available in each logic family; see Table 2-4. To increase the sensitivity (display size) press the upper button.

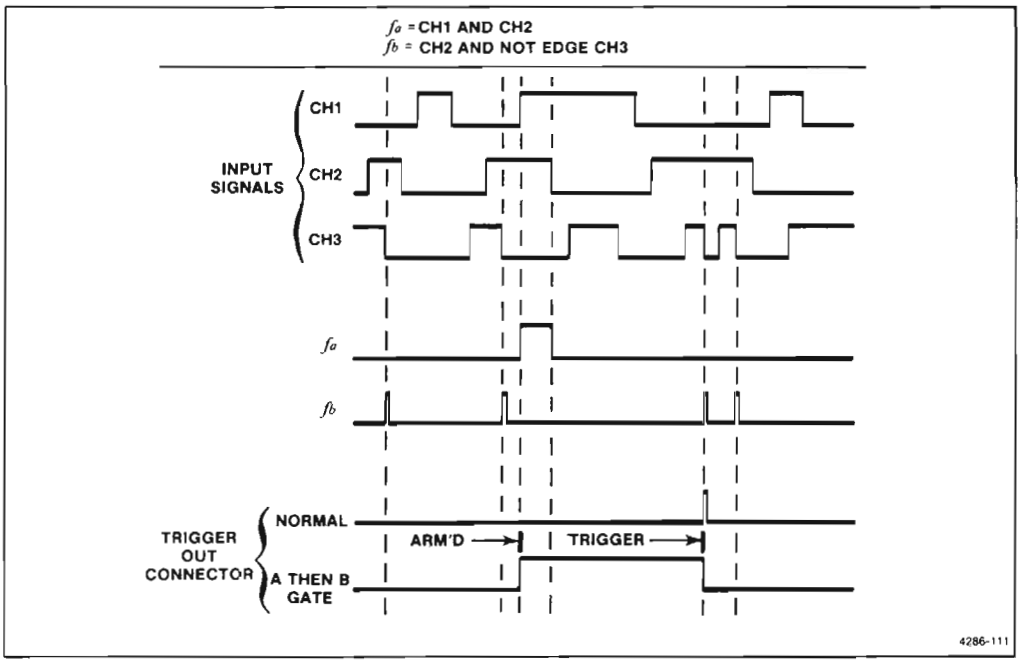


Figure 1-14. Example of A THEN B, level and EDGE sensitive TRIGGER FUNCTION, showing the Normal and A THEN B Gate waveform alternatives.

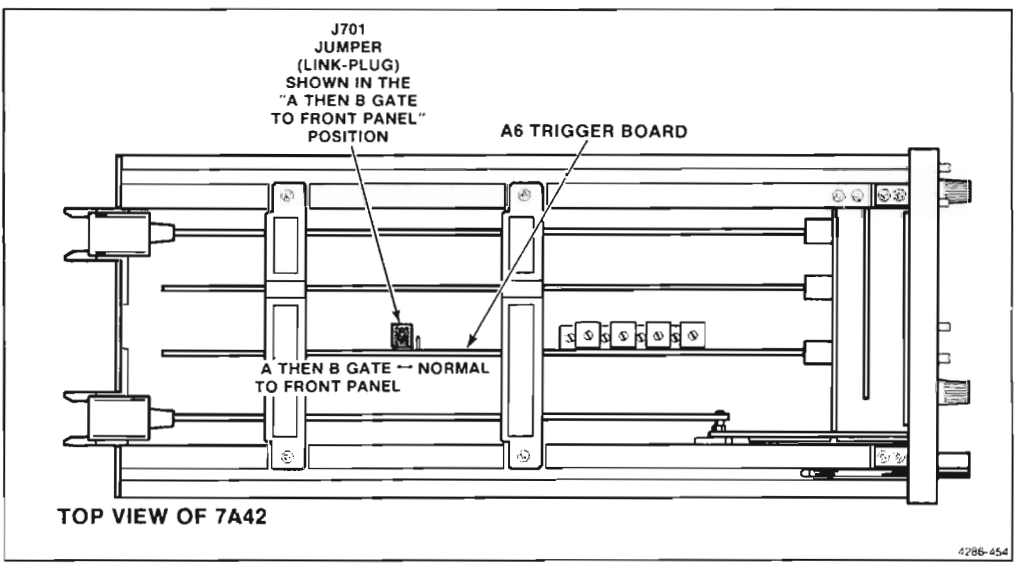


Figure 1-15. Location of J701, on A6 Trigger Board.

TABLE 1-8
Channel Volts/Division Ranges

Logic Family	At The BNC	Through a 10X Probe
TTL (CMOS)	.1, .2, .5 V/Div	1, 2, 5 V/Div
ECL	20, 50, 100 mV/Div	.2, .5, 1 V/Div

GND. The GND pushbutton connects the selected channel amplifier input to ground as a reference for trace positioning. However, the incoming signal is not grounded; it is disconnected from the amplifier input.

1MΩ/50Ω. The 1MΩ/50Ω pushbutton selects the input impedance of the selected channel. The available impedances are 1 megohm in parallel with about 15 pF, or 50 ohms.

THRESH. Each of the four input channels have two possible preset threshold voltages, +1.4 volts for the TTL mode and −1.30 volts for the ECL mode. In addition, these threshold voltages can be altered using the LEVEL⇧ or LEVEL⇩ pushbuttons. The SWITCHING THRESHOLD VOLTS display will indicate the threshold voltage present at each of the channel inputs. To turn the SWITCHING THRESHOLD VOLTS display on, press the THRESH pushbutton (the light should be on).

The SWITCHING THRESHOLD VOLTS display corresponds to the channel pushbutton that is lit (CH1, CH2, CH3, or CH4). While the button is lit, the actual threshold voltage for the channel is indicated in the seven-segment LED display. For each logic family there are internally preset thresholds that can be altered by pressing either the LEVEL⇧ or LEVEL⇩ button. A single push changes the threshold by one increment. When either LEVEL button is held down the rate accelerates. Each channel's threshold level is maintained when THRESH is pushed again to turn off the seven-segment display and button light. However, for a particular channel, the v

TIP jack, push the PROBE OFFSET button once again to acquire this offset measurement into the 7A42. The probe offset button will now light green and the probe tip may now be removed. The offset measurement remains in the display. Altering the 7A42 trigger threshold (independent of the probe offset) may be done using the LEVEL buttons. Pushing the PROBE OFFSET button once more turns off the lit button and clears the acquired offset measurement. The 7A42 PROBE OFFSET feature is appropriate for use only with the P6230 probe.

The acquired PROBE OFFSET voltage, whether zero or otherwise, is maintained when the THRESH button is turned off or while threshold information of another channel is being displayed. That value is also maintained if the logic family is changed, adding to the preset threshold levels as expected. If a channel has a non-zero offset and THRESH (with that channel selected) is turned on, the PROBE OFFSET button will be lit green (a reminder of the offset status).

LEVEL. The LEVEL⇧ and LEVEL⇩ controls are used to set the threshold voltage of each channel to a value other than the preset threshold voltage. These controls are active only in the PROG CHAN mode and when the THRESH pushbutton switch is lit.

When either the LEVEL⇧ or LEVEL⇩ button is held, the variable threshold changes at an accelerating rate, pausing momentarily at the preset value.

The SWITCHING THRESHOLD VOLTS display indicates the preset threshold voltage or the variable threshold voltage set by the LEVEL⇧ and LEVEL⇩ controls. The CH1, CH2, CH3, and CH4 pushbuttons indicate which channel's threshold voltage is being monitored.

PROGRAM TRIGGER MODE

CLEAR. The CLEAR pushbutton erases the TRIGGER FUNCTION program currently displayed by the TRIGGER FUNCTION indicators. The other stored TRIGGER FUNCTION program remains unaffected by the CLEAR operation (see A, B and A THEN B).

NOT. The NOT pushbutton is used to negate a variable in the Boolean TRIGGER FUNCTION. For example, if CH1 is entered into the TRIGGER FUNCTION display (that is, CH1 is an active HI, red), pressing the NOT key will change it to an active LO (green). Successively pressing the NOT key will alternately change the CH1 indicator from HI to LO; this sequence will continue until a delimiter is entered (AND or OR).

EDGE. The EDGE pushbutton is used to change a level sensitive variable in a Boolean TRIGGER FUNCTION from level to edge sensitive. The NOT pushbutton is used with the EDGE pushbutton to select falling edge sensitivity. For example, the keystroke sequence CH1 EDGE programs the 7A42 to trigger on the rising transition of CH1; the keystroke sequence CH3 NOT EDGE sets it to trigger on the falling transition of CH3. Pressing the EDGE key twice changes the channel to edge-sensitive and back to level-sensitive, similar to the operation of the NOT key.

The 7A42 allows one independent EDGE-sensitive channel per product in each TRIGGER FUNCTION (A and B).

NOTE

The channel (CH1, CH2, CH3 or CH4), EDGE, and NOT keys can be entered in any order. For instance, the keystroke sequences CH1 NOT EDGE, NOT CH1 EDGE, and EDGE NOT CH1 are equivalent.

If the product already contains one edge-sensitive channel at the time a second edge-sensitive channel is entered into the same product, the last entered channel will receive the edge-sensitive status. The previous edge-sensitive channel will become level-sensitive only. This is because only one edge-sensitive channel per product is allowed. If the last entered channel is converted back to level-sensitive, the previous edge-sensitive channel will again become edge-sensitive.

THEORY OF OPERATION

This section describes the circuitry in the 7A42 Logic Triggered Vertical Amplifier. The description starts with a discussion of the instrument, using the block diagram shown in Figure 2-1. Next, each circuit is described in detail with supporting illustrations, where appropriate, to show the relation between the stages in each major circuit. Detailed schematic diagrams of each circuit are located in the Diagrams and Circuit Board Illustrations section at the back of this manual. Refer to these schematics throughout the following description for specific values and relationships.

BLOCK DIAGRAM

The following discussion presents an overview of the 7A42 before discussing the individual circuits in detail. In the simplified block diagram shown in Figure 2-1, each major circuit has a block. The number(s) in each block refer(s) to the schematic diagram(s) that show(s) the complete circuitry. The schematic diagrams are located at the back of this manual.

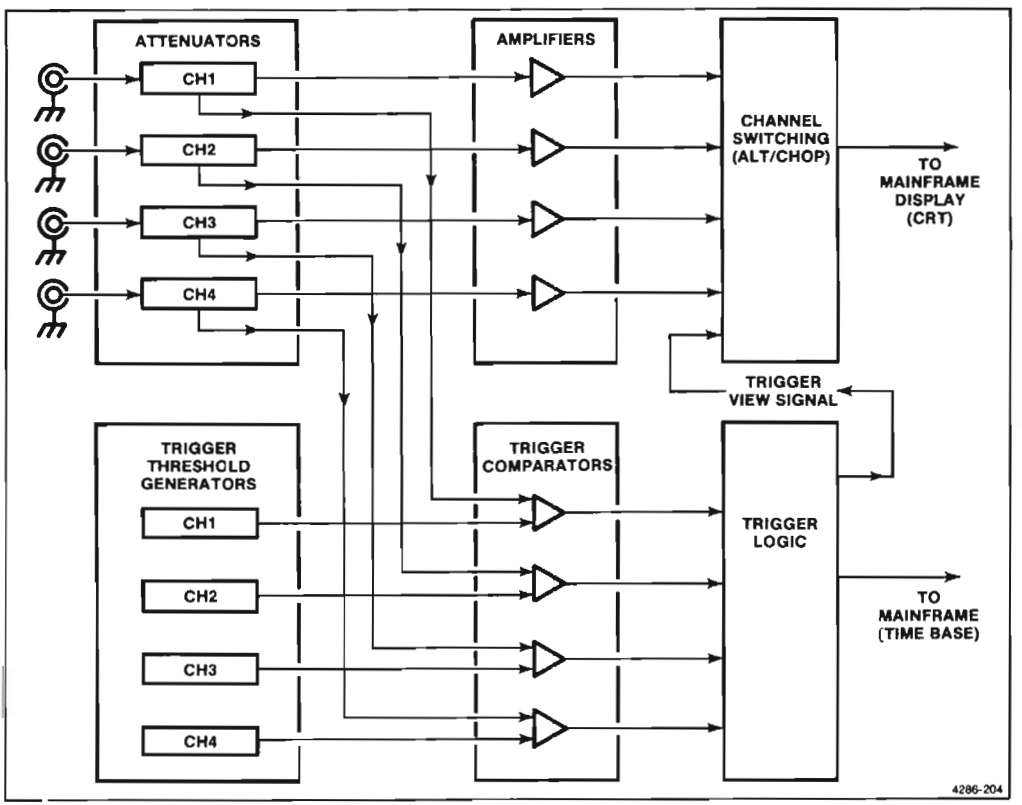


Figure 2-1. Simplified Block Diagram.

DESCRIPTION

The 7A42 has six functional blocks of circuitry; attenuators, amplifiers, channel-switching, trigger-threshold generators, trigger comparators, and trigger logic (see Fig. 2-1).

Each channel (Ch1 through Ch4) has its own attenuator, amplifier, trigger-threshold generator, and trigger comparator. Impedance selection (50 ohms or 1 megohm) and gain switching (volts/div) are accomplished by the attenuator. Each channel's attenuator has two signal outputs, one for the trigger comparator and another for the amplifier.

The amplifiers provide the gain necessary to drive the vertical amplifiers in the host oscilloscope. The channel-switching stage provides vertical signal processing to display the channel traces and the trigger-view trace on the host oscilloscope crt. This is accomplished by either chopping between the channels selected for display, or by displaying them alternately after each sweep.

The trigger comparator compares the signal from the attenuator with the voltage from the trigger-threshold generator. When the signal from the attenuator exceeds the threshold voltage, the trigger comparator produces an output which is applied to the trigger-logic stage.

The trigger-logic stage accepts outputs from the comparator and compares them with the programmed logic level of each channel. When the applied input signal(s) match the programmed trigger-logic conditions, a trigger pulse is produced. The user sets the trigger-logic conditions via the 7A42 front panel.

TABLE 2-1
Signal Name Dictionary

Signal Name	Description	Located on Diagram
+15B	+15 volt power supply—Decoupled mainframe power supply from right side of 7A42.	1, 2, 4, 10, 11
+5B	+5 volt power supply—Decoupled power supply from right side of 7A42.	1, 2, 4, 10, 11
+5C	+5 volt power supply—Decoupled mainframe supply from left side of 7A42.	1, 2, 4, 10, 11
+5D	+5 volt power supply—Digital power supply from Power Supply Board.	1, 2, 4, 10, 11
-15B	-15 volt power supply—Decoupled mainframe power supply from left side of 7A42.	4, 5, 6, 7, 8, 9, 10
-15C	-15 volt power supply—Decoupled power supply from left side of 7A42.	3, 4, 7, 10, 11
-2D	-2 volt power supply—Source is Power Supply Board.	1, 5, 6, 7, 8, 9, 11
-5D	-5 volt power supply—Source is Power Supply Board.	1, 5, 6, 7, 8, 9, 11
-5V1--5V4	Separate -5 volt power supplies to CH1-CH4 attenuator hybrids.	2, 11
-11V1--11V4	Separate -11 volt supplies to CH1-CH4 attenuator hybrids.	2, 11
1AXON, ...4BYON	Channel (1), Function (A), First Product (X), On—Control lines from the trigger logic control shift register level shifters to the Boolean logic. These lines gate the desired signals into the Boolean logic.	5
$\overline{\text{1AXINV}}$, ...$\overline{\text{4BYINV}}$	Channel (1), Function (A), First Product (X), Invert—Control lines from the trigger logic control shift register level shifters to the Boolean logic. These lines selectively invert the input signals.	5
1CW-4CW	Clockwise—Connections to CH1 position control pot. There is 0 ohms between 1W (wiper) and this pin when the knob is rotated to the clockwise (CW) position.	3, 12

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
1CCW-4CCW	Counterclockwise—Connections to CH1 position control potentiometer. There is 0 ohms between this pin and pin 1W (wiper) when the knob is rotated to the counterclockwise (CCW) position.	3, 12
1W-4W	Wiper—Wiper connection of CH1 position control potentiometer.	3, 12
$\overline{7854}$	7854—Decoded read strobe used to determine the location of link-plug jumper 540.	9
A9-A11	Address—Address lines to an address decocer on the Digital Board.	4, 9
$\overline{\text{A MODE}}$	A MODE—When low, enables trigger function A.	7, 8
$\overline{\text{A THEN B}}$	A THEN B—A control signal to enable the A THEN B latch.	7, 8
ALE	Address Latch Enable—Decodes the multiplexed AD bus from the microprocessor.	9
ALT	ALT—Selects ALT display mode.	4
ALT DRIVE	Mainframe ALT DRIVE—A6 of Main Interface connector.	4
ALTSN	ALT Sync—When high, this signal synchronizes the displayed channel to the ALT DRIVE signal.	4
$\overline{\text{AT COL}}$	Attenuator Column—An address decoded write select which clocks the Attenuator Column latch (part of the armature relay driver circuit).	2, 4
$\overline{\text{AT ROW}}$	Attenuator Row—An address decoded write select which clocks the Attenuator Row latch (part of the armature relay driver circuit).	2, 4
BD0-BD7	Buffered Data—Buffered Data Bus lines zero through seven (external to kernal).	1, 2, 4, 5, 8, 9, 10, 12
BEXTCLK	Buffered External Clock—This is the external clock signal from the clock buffer to the edge detector.	6, 7
BUSCLR	Bus Clear—This signal (in the XBUSX diagnostic test) lights a LED if the External Bus is operational.	9
$\overline{\text{CATS}}$	Not implemented.	9
$\overline{\text{CATSRD}}$	Not implemented.	9
$\overline{\text{CH13}}$, $\overline{\text{CH24}}$	Control lines to the (CH1, CH2) and (CH3, CH4) channel switches (M211s).	3, 4
$\overline{\text{CH12}}$, $\overline{\text{CH34}}$	Control lines to the (CH1, CH2) or (CH3, CH4) channel switch (M211).	3, 4
CH1 COL	Channel 1 Column—7K-series CH1 column readout information.	10
CH1 ROW	Channel 1 Row—7K-series CH1 row readout information.	10
CH1-CH4 SIG	Input lines from the hybrid attenuator impedance converter to the trigger amplifier.	3
$\overline{\text{CH1-CH4}}$	CH1-CH4—Indicates currently displayed channel when low.	4

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
CH2 COL	Channel 2 Column—7K-series CH2 column readout information.	10
CH2 ROW	Channel 2 Row—7K-series CH2 row readout information.	10
CHOP	CHOP—Selects CHOP display mode.	4
CHOP DRIVE	CHOP DRIVE—A5 of Main Interface connector.	4
$\overline{\text{DSPC}}$	Display Control—An address decoded write select which clocks the Display Control latch.	4
$\overline{\text{DSPT}}$	Display Test—An address decoded write select which clocks the Display Test latch.	4
$\overline{\text{DSPV}}$	Display View—Channel Switch signal controlling Trigger View display.	3, 4
DVD0-DVD3	DVM Digit—Probe Offset DVM display Digit drivers (active low).	1, 12
$\overline{\text{DVM LED}}$	Digital Volt Meter LED—An address decoded write select which clocks the Probe Offset DVM display driver IC (7218B).	1, 4
DVS0-DVS7	DVM Segment—Probe Offset DVM display Segment drivers (active high).	1, 12
$\overline{\text{ERRTRG}}$	Error Trigger—When used in the diagnostics mode, is pulsed by diagnostic firmware whenever an error is detected (active low).	9
$\overline{\text{ETST}}$	Enable Test—Used to enable the Wait State Test circuit.	9
$\overline{\text{EXEDGEN}}$	External Edge Enable—When low enables external clock. See Theory of Operation for more details.	6, 7
EXT CLK EXER	External Clock Exercise—This signal is high during some diagnostics to control the state of the External Clock input.	7, 8
EXT CLK SLOPE	External Clock Slope—A control signal which selects the desired external clock edge.	7, 8
EXT CLK SYNC	External Clock Sync—A control signal which enables the external clock buffer when external clock synchronization is desired.	7, 8
EXT CLOCK INPUT	External Clock Input—This input is from a peltola connector on the front panel jack to the Trigger Board.	7
FD0-7	Filtered Data bus—The buffered data bus after passing through some series resistors that slow the transistions.	5
FILTER OFF	Filter Off—A control signal used to disable the trigger filter.	6
FNA, FNB	Function A, Function B—The output of the Boolean logic. These lines go high when the function is true.	5, 7
FPLC0-FPLC7	Front Panel LED Column—Front panel LED column drivers zero through seven.	1, 12
$\overline{\text{FP LED}}$	Front Panel LED—An address decoded write select which clocks the display driver IC (7218A) of the Front Panel LEDs.	1, 4
FPLR0-FPLR4	Front Panel LED Row—Front Panel LED row drivers zero through four.	1, 12
$\overline{\text{GENIN}}$	General Input—An address decoded read select (active low) used to read the General Input latch onto the data bus.	9

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
$\overline{\text{GENOUT}}$	General Output—Address decoded write select (active low) used to write data into the General Output latch.	9
$\overline{\text{INTAC}}$	Interrupt Acknowledge—Resets the RST5.5 latch (real time interrupt).	9
KPD1-4	Relay Pull Down—Pull-down lines in armature drive circuit.	2, 12
KPU1-4	Relay Pull Up—Pull-up lines in armature drive circuit.	2, 12
KPUD1-5	Relay Pull Up-Down—Pull-up/down lines in armature drive circuit.	2, 12
$\overline{\text{KYCD}}$	Key Code—An address decoded read select (active low) used to read keycode data.	1, 9
$\overline{\text{LO READ}}$	Lower Readout—An address decoded write select which clocks the lower readout latch.	4, 10
$\overline{\text{MATRIX}}$	Matrix—Address decoded write select (active low) to LED matrix driver IC.	1, 9
$\overline{\text{MENAX-MENBY}}$	Multiplexer Enable, Function (A), First Product (X)—Control lines from the trigger logic control shift register level shifters to the Edge Detectors. These lines enable the multiplexer for an edge sensitive channel.	5, 8
MS0AX, ...MS2BY	Multiplexer Select, Channel (0), Function (A) First Product (X)—Control lines from the trigger logic control shift register level shifters to the Edge Detectors. These lines select the desired edge sensitive channel.	6, 8
MXCX, MXCY	Matrix Column X and Matrix Column Y—Matrix LED column driver lines (active low).	1, 12
MXR0-MXR7	Matrix Rows—Matrix LED row driver lines (active high) zero through seven.	1, 12
PC1-4	Probe Coding—Probe coding channels one through four.	2, 9, 12
PIM	Plug-In Mode—TTL version of Plug-In Mode, B35 of 7K-series interface.	4
$\overline{\text{PODAC}}$	Probe Offset DAC—Address decoded select (active low) used to write data to the Probe Offset DAC which is used to do an analog to digital conversion of the Probe Offset voltage.	9
POG	Probe Offset Green—A signal which lights the green Probe Offset LED.	4, 12
POR	Probe Offset Red—A signal which lights the red Probe Offset LED.	4, 12
$\overline{\text{PUPCK}}$	Power Up Clock—Clock signal indicates instrument power up.	9
$\overline{\text{PUST1}}$	Pull Up Strobe 1—Strobe which clocks the armature relay drive circuitry.	2
$\overline{\text{PUST2}}$	Pull Up Strobe 2—Strobe which clocks the armature relay drive circuitry.	2
PUST/$\overline{\text{PDST}}$	Pull Up Strobe/Pull Down Strobe—Strobe which clocks the armature relay drive circuitry.	2

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
QWR	Qualified Write—This is the qualified WR of the 8085 (active high) with A12 ∧ A13 ∧ A14.	4, 9, 12
$\overline{\text{RAM}}$	Random Access Memory—An address decoded select (active low) which is further decoded to produce RAM chip select.	9
RD	Read—Read strobe.	9
$\overline{\text{RD}}$	Read—Compliment of Read strobe.	9
RD+WR	Read OR Write—Signal is high during Read OR Write operation.	9
$\overline{\text{RELN}}$	Relay Enable—This signal is used to disable the attenuator relay drivers at power-up until the processor can initialize the system. It also disables the piezo speaker in a similar fashion.	2, 4, 9, 12
$\overline{\text{RESET INPUT}}$	Reset Input—This input is a peltola connector from the LED Board to the Trigger Board.	7
RL0-RL7	Return Lines—Keyboard switch Return Lines (active low) zero through seven.	1, 12
RSAX, RSAY	*Reset, Function (A), First Product (X)*—Reset signal for trigger function A.	6, 7
RST 5.5	RST 5.5—Interrupt to 8085 which occurs with the real time clock.	1, 9
RST 6.5	RST 6.5—Interrupt to 8085 from the keyboard decoder.	1, 9
RST 7.5	RST 7.5—Interrupt to 8085 which occurs with each timeslot.	9, 10, 12
$\overline{\text{ARST}}$	Restart—No automatic restart when low.	9
SA START	Signature Analysis Start—Signature Analysis Start bit.	9
SA STOP	Signature Analysis Stop—Signature Analysis Stop bit.	9
SACK	Signature Analysis Clock—Signature Analysis Clock bit.	9
SID	Serial Input Data—Serial input to 8085. This signal is an inverted TTL representation of TS1 (Time Slot one).	9, 10, 12
$\overline{\text{SINGCH}}$	*Single Channel—When low this line indicates only a single* channel is displayed.	4
SL0-SL3	Scan Lines—Keyboard switch Scan Lines (active high) zero through three.	1, 12
SOD	Serial Output Data—Serial output data from 8085. This is used as a control to the 7218 Display driver chips.	1, 9
STAX, ...STBY	Strobe, Function (A), First Product (X)—Strobe trigger function.	5, 6
$\overline{\text{SYNCAX}}$, ...$\overline{\text{SYNCBY}}$	Sync, Function (A), First Product (X)—Control lines from the trigger logic control shift register level shifters to the Edge Detectors. The line is low when edge sensitivity or external clock is active.	5, 6
TB0	Test bit 0—Used in Self Test and Diagnostics from Trigger Board.	6, 7, 9
TB1	Test Bit 1—Used in Self Test and Diagnostics from Digital Board.	4, 9, 12

TABLE 2-1 (CONT)
Signal Name Dictionary

Signal Name	Description	Located on Diagram
TB2	Test bit 2—Used in Self Test and Diagnostics from Trigger Board.	6, 9, 12
TB3	Test bit 3—Used in Self Test and Diagnostics from Trigger Board.	5, 6, 9, 12
TB4	Test bit 4—Used in Self Test and Diagnostics from Trigger Board.	5, 6, 9, 12
TB5	Test bit 5—Used in Self Test and Diagnostics from Trigger Board.	8, 9, 12
TEST	Test—When active, this line causes the PAL to be in test mode, e.g., setup for LSSD (Level Sensitive Scan Design).	4
TFP1-TFP2	Trigger Filter Pot—The two connections to the trigger filter potentiometer.	5, 12
TFS1-TFS2	Trigger Filter Switch—The two connections to the trigger filter switch.	5, 12
TIP	Tip—Front panel Probe Offset jack.	9, 12
TRAP	Trap—A nonmaskable interrupt to the 8085. It will occur when any of the 50 ohm input resistors are over dissipated. This interrupt is rising edge sensitive.	2, 9, 12
TRAP1-TRAP4	Trap—The source of these signals is the attenuator hybrid. These analog signals represent the power dissipation of the 50 ohm input resistors.	2, 12
TRIG VIEW OUT	Trigger View Output—The Trigger View output signal to the display channel switch on the Amplifier Board.	7
TRIGEN	Trigger Enable—A control signal which enables the trigger logic output and releases reset to the A THEN B flip flop.	7, 8
$\overline{\text{TRSH1-TRSH4}}$	Threshold 1-Threshold 4—Address decoded write lines (active low) used to write the trigger threshold DACs.	5, 9, 12
TS1	Time Slot One—7K-series readout.	10
TSX	Time Slot X—This signal is the result of diode ORing Time Slot lines one through ten.	10
$\overline{\text{UP READ}}$	Upper Readout—An address decoded write select which clocks the upper readout latch.	4, 10
$\overline{\text{WRKB}}$	Write Keyboard—An address decoded write select (active low) to keyboard controller IC.	1, 9
$\overline{\text{WRMD}}$	Write Mode—An address decoded write select line (active low) used to clock the trigger mode latch on the Trigger Board.	8, 9, 12
$\overline{\text{WRTL}}$	Write Trigger Logic—An address decoded write line (active low) used to clock the trigger function into the trigger control shift registers.	8, 9, 12
$\overline{\text{XBUSX}}$	External Bus Exercise—An address decoded select (active low) used to determine if the XBUSX strap is installed.	9
$\overline{\text{XWR}}$	X Write—A system write strobe which becomes a read strobe during signature analysis.	9

DETAILED CIRCUIT OPERATION

Complete schematic diagrams are provided in Section 7, Diagrams and Circuit Board Illustrations. The number inside the diamond preceding a heading in the following discussions refers to the schematic diagram for that circuit. The schematic diagrams contain wide shaded borders around the major stages of the circuit to conveniently locate the components mentioned in the following discussions. The name of each stage is given in a shaded box on the diagram, and appears as a subheading in the discussion of that schematic diagram.

All logic functions are described using the positive logic convention. Positive logic is a system of notation where the more positive of two levels (HI) is called the true or 1-state; the more negative level (LO) is called the false of 0-state. The HI-LO method of notation is used in this logic description. The specific voltages that constitute a HI or LO state vary between individual devices. Whenever possible, the input and output lines are named to indicate the function that they perform when in the HI (true) state.

1 FRONT PANEL DISPLAY AND CONTROL

KEYBOARD DECODER

The keyboard decoder IC decodes the keyboard switch array, informs the MPU (Microprocessor Unit) when a key is pressed, and sends a binary code to the MPU indicating which key was pressed.

The keyboard is continually scanned by U205. When a key is pressed, U205 interrupts the MPU (via RST 6.5) and loads the corresponding eight-bit code onto an internal first-in/first-out register which is then read by the MPU.

Detailed information about the internal functioning of the keyboard decoder IC may be obtained from the manufacturer's data books.

CHANNEL STATUS AND SWITCH LED DRIVER

The 7218 LED driver (U320) accepts binary data from the MPU and drives the Channel Status LEDs and the Switch LEDs. The 7218 LED driver is set in 'no decode' mode to drive the LEDs directly with the binary data from the MPU. Refer to the manufacturer's data for detailed information on the internal functioning and programming of the 7218 LED driver.

THRESHOLD DISPLAY DRIVER

The Threshold Display Driver (U110) accepts BCD data from the MPU and drives the Threshold Display array. The 7218 LED driver is configured to store and decode the input data from the MPU and produce the appropriate outputs to drive the seven-segment LED displays.

MATRIX LED DRIVER

The Matrix LED Driver circuit (U105) is essentially the same as the Channel Status and Switch LED Driver (U320) described above, except that the output of U105 drives the Matrix LEDs. (Also, U105 is designed to drive a common-cathode array, where U320 drives a common-anode array.)

2 ATTENUATORS AND CONTROL

ARMATURE RELAY DRIVERS

Figure 2-2 shows a simplified block diagram of the Armature Relay Matrix used in the 7A42. The relays are arranged in this matrix to minimize the total number of drives and interconnects.

Each series pair of coils represents a single relay. The nomenclature beside each coil shows the function invoked when current is pulsed in the indicated direction.

The KPU (Pull Up) and KPD (Pull Down) drive lines are unidirectional. The KPUD (Pull Up Down) lines are bidirectional (able to source or sink current).

While idle, all outputs of AT COL latch (ATtenuator COLumn latch) A7 U421 are high, as are pins 15 and 16 of AT ROW latch (ATtenuator ROW latch) A7 U420. This results in all relay drive lines being high impedance.

To activate a relay, the drive signal must be present for about 15 ms.

As an example, the following is the sequence of events which take place to insert the CH1 2.5X attenuator. ($ indicates a hexadecimal number.)

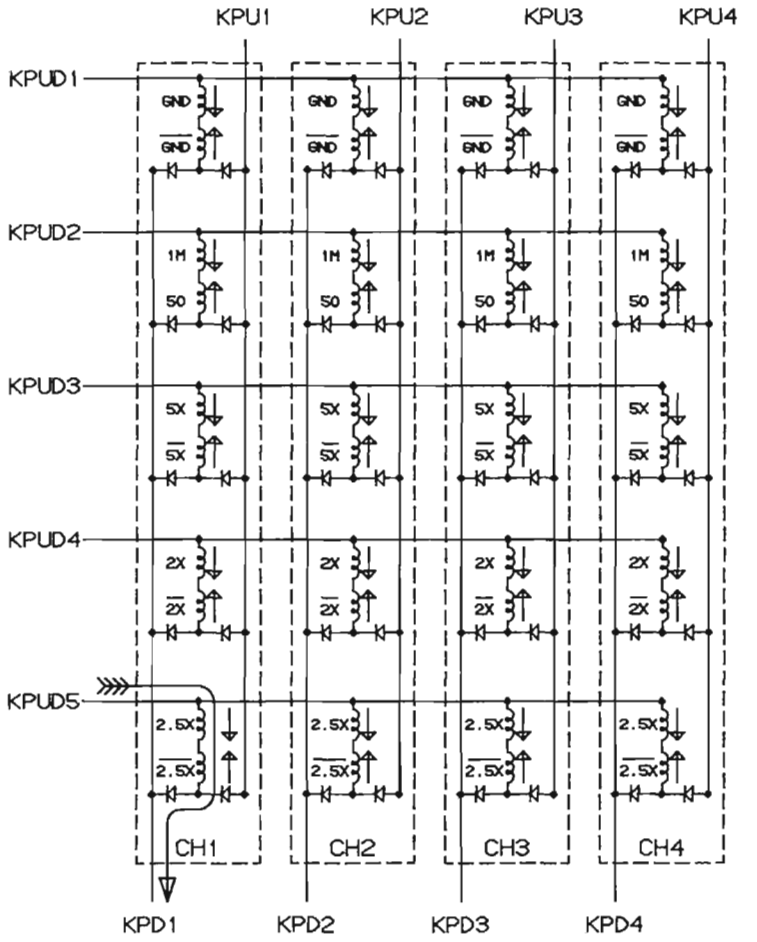


Figure 2-2. Armature Relay Matrix (Actuating the CH1 2.5X attenuator).

1. Write $FD to AT COL latch: selects KPD1 (only one output of this latch will be low at a time to insure that KPU and KPD drives are never activated simultaneously).

2. Write $70 to the AT ROW latch: set PUST/$\overline{\text{PDST}}$ low to enable KPD1; select KPUD5 to pull up, all other KPUD lines to pull low; $\overline{\text{PUST1}}$, $\overline{\text{PUST2}}$ are set high (same as idle state).

3. Write $10 to AT ROW latch: same data as step 2, but this time with $\overline{\text{PUST1}}$ and $\overline{\text{PUST2}}$ set low to enable KPUD drives.

4. Wait approximately 15 ms.

5. Write $FF to the AT COL latch: disables all KPU, KPD lines.

6. Wait 5 ms for transients to decay. (see below)

7. Write XX11XXXX (binary) to the AT ROW latch to disable the KPUD lines. Diodes CR520, CR521, CR530, and CR630 on the KPU lines protect the 75325 from voltage spikes when these lines turn off. There is similar protection internal to the 75325's on the KPD lines. Step 6 above insures that relay coil current has decayed before releasing the KPUD drive.

Jumper A7 J401, RELN, is provided to disable the relay drives in times of trouble (e.g., processor out of control).

The dc resistance of the relay coils is about 40 ohms each. This resistance along with the 18 ohm collector resistance on pin 1 of the 75325's results in about 12 volts across the pair of relay coils being activated.

OVERLOAD COMPARATORS

Four identical voltage comparator circuits are used to monitor the TRAP lines from the Attenuator hybrids. Their open collector outputs are wire-ORed at pull-up resistor R236. If any of the four attenuator 50-ohm termination resistors is over-dissipated, it's associated negative temperature coefficient sensing network will drive the comparator's + input below the reference voltage set by R234, R235, CR230, and CR231. This drives the output low, which is inverted through U830 to cause a high priority TRAP interrupt to the processor. The processor then disconnects all inputs using relay control.

The feedback resistors, along with the 1K resistors and 0.1μF capacitors provide hysteresis and noise filtering.

Trigger Pickoff

The attenuator modules send the trigger output signal through the attenuator control board and a series resistance to the trigger board comparators.

CHANNEL SWITCHING AND AMPLIFIERS

CHANNEL AMPLIFIERS

Channels 1 through 4 each have an independent amplifier stage which provides voltage gain between the attenuator output and the channel switch input. All four of these stages are identical, therefore, only channel 1 will be described.

The input signal from the attenuator module enters the amplifier board through two interconnect pins. The single ended signal (with an offset of -5 volts) then goes through a small balun transformer to convert the high-frequency component into a true differential signal. The -5 volt offset was chosen at this point so that no further level shifting in the amplifier path would be necessary. The balun output is connected to the input bases of a differential amplifier IC. After looping through the bases it is terminated by R1011. Capacitors integral to the ECB and the inductance of the amplifier IC leadframe and bondwires form bridged, tee-coil peaking, at the bases to offer a resistive load impedance to the attenuator and improve the bandwidth of the stage.

The amplifier stages use hybrid thick-film resistor networks as bias and 'long tails'. The resistor networks are placed between the channel amplifiers and are shared between adjacent channels. A total of five networks are needed; the networks above channel 1 and below channel 4 are only partially used. Within the network are three resistors in a series divider configuration from ground to -5 volts. Taps at -3 volts and -4 volts set the bias inside the amplifier to ensure that the signal is sent through the proper pair of output transistors. For a given amplifier IC, the network located physically below that IC provides these bias voltages.

The resistor network located above an amplifier IC serves as a long-tail current source to the amplifier emitters. The long tail is divided into two sections by a tap. Low-frequency (thermal) compensation is connected between the taps. High-frequency compensation is connected directly between the emitters. The total resistance is set to provide a 12.5 mA current source at each emitter.

The outputs of the amplifiers are connected to the channel switches through 75-ohm microstrip transmission lines on the ECB. The individual channel gain adjustment is made with a trimmer potentiometer that shunts a portion of the differential signal. Diodes to ground provide protection to the channel switches if the amplifier IC inadvertently becomes disconnected.

Position Control

The position control circuit provides 6.5 mA of the 12.5 mA standing current needed by the amplifier stage. The

trace is positioned by adding additional current to one side and taking an equal amount from the other. For each channel, the two PNP transistors serve as these position control current sources. They are controlled by the front-panel POSITION control and a long-tail network chosen to minimize the common mode positioning current variation over the entire position range. Diodes CR900 and CR910 protect the channel switch inputs if the position control potentiometer should inadvertently become disconnected.

The position control circuit is isolated from the analog signal lines by series resistors R910 and R911 and balun transformer T800 that has been installed backwards. The transformer will pass common mode signals but will reject differential signals. Series resistor, R800, and capacitor, C700, shunting the position control transistors, provide mid-frequency compensation.

CHANNEL SWITCHES

The 7A42 uses three hybrid channel switches. Channel switch U600 combines the channel 1 amplifier output with that of channel 2. Channel switch U640 combines the outputs of channels 3 and 4. The outputs of U600 and U640, after passing through delay lines, are combined by a third channel switch, U240, which also introduces the trigger view signal.

The channel switches select one output signal from four input signals. The desired input signal is selected via four TTL-compatible control lines (pins 13, 14, 24, and 25). The output is intended to drive a 150-ohm load and provide reverse termination for a delay line.

Inputs A and B require a current source drive and have a transimpedance of 300 ohms from input to output. Inputs C and D require a voltage drive from a 150-ohm source and have a voltage gain of 0.75.

The control lines are active low, i.e., when low the associated input signal will appear at the output.

The outputs from the channel 1 through channel 4 amplifier stages are connected to the A and B inputs of the first two channel switches. These inputs supply the remaining 6 ma of standing current required by the amplifier stage output.

Two bias networks are required to support these channel switches. The 1.24 K resistor provides an accurate 4 mA bias, while the variable resistance to ground is used to optimize the front corner of the step response. The pair of 75-ohm resistors connect an unused portion of the circuit to ground.

The channel switch output impedance is 75 ohms per side. The outputs drive two matched 15.5 ns, 150-ohm delay lines, DL600 and DL640. The delay lines are terminated by the third channel-switch's inputs (C and D). The trigger view signal is injected through input B.

The resistor network across the channel switch outputs, along with the channel switch output impedance, provides a 50-ohm reverse termination (per side) and a small amount of front-panel gain adjustment.

The trigger view signal arrives at the A5 Amplifier board as a differential signal. The associated resistors set the trigger view display amplitude, and the TRIGGER VIEW POSITION control allows it to be moved to any location on screen.

4 DISPLAY CONTROL

ADDRESS DECODER AND LATCH

The QWR (Qualified WRite) and processor address lines A9, A10, and A11 are used to generate eight write strobes on the A7 Digital board using an LS138 address decoding chip. The write strobes are the same width as the processor $\overline{WR}$ signal (700 ns) and are active low.

DISPLAY CONTROL

Channel switching is predominantly controlled by U800, a PAL16R6, which contains a fuse pattern configuring it as a synchronous state machine. Channels to be displayed are presented to the PAL as the input vector via Display Control latch outputs D1 through D5. Here D1 corresponds to CH1, D2 to CH2, etc. and D5 to Trigger View.

With each clock to the PAL on pin 9, the output vector on pins 14 ($\overline{CH5}$) through 18 ($\overline{CH1}$) advances to display the next channel. The outputs are active low and mutually exclusive.

As an example, assume that the desired display selected from the front panel is CH1, CH3, and Trigger View. With each clock pulse to the PAL the outputs would change as follows:

D1	D2	D3	D4	D5	CH1	CH2	CH3	CH4	CH5
1	0	1	0	1	0	1	1	1	1
1	0	1	0	1	1	1	0	1	1
1	0	1	0	1	1	1	1	1	0
1	0	1	0	1	0	1	1	1	1
					etc.				

The PAL is clocked on both rising and falling edges of either the Chop Drive or Alt Drive signals which are supplied by the mainframe and selected through analog switch U820.

The voltage levels of CHOP and ALT Drive are typically -0.6 to 1.1 volts and are not suitable to drive the TTL inputs of the PAL directly. Transistors Q810 and Q811, and their surrounding components, form a comparator with hysteresis and variable reference level to decrease propagation delay from Chop Drive's edge to channel switch settling time. The varying reference level is necessary because of the slow rise and fall times of Chop Drive.

In "test" mode, when TEST is high on pin 7 of the PAL, the PAL's internals are reconfigured so that it can be tested using Level Sensitive Scan Design techniques. Psuedo random data is entered to the PAL by the processor on D1 of the Display Control latch, and clocked in with $\overline{\text{BUSCK}}$ of the Display Test latch. Output data from the PAL is read back by the processor via TB1 and entered into a Signature Analysis routine.

Other outputs on the Display Test latch include $\overline{\text{HORN}}$, used to activate the piezo speaker; MODE, used as an input to U110 and U320 when writing their control words, $\overline{\text{POG}}$ and $\overline{\text{POR}}$; Probe Offset Green and Probe Offset Red LED drivers.

The negative bias for U820 is set by CR810, CR811, and R811.

HORN

Timer U730 is wired as an astable multivibrator which freeruns at about 4 kHz. The oscillator is disabled by pulling the Discharge line, pin 7 to ground. The software controls the horn through the Display Test latch and saturating switch Q720D. It is also disabled at power up by Q720B, until the processor has initialized the hardware.

5

TRIGGER COMPARATORS, BOOLEAN LOGIC, AND FILTERS

THRESHOLD DACs

The trigger threshold voltages for channels 1 through 4 are determined independently by threshold DACs U1020, U1030, U1022, and U1032 respectively. The DACs are controlled by the buffered data bus, BD0-BD7, which passes through series resistances to form the filtered data bus, FD0-FD7. Slower transition times on the filtered data bus requires that writes to the A6 Trigger board include a wait state. A low level on select lines $\overline{\text{TRSH1}}$-$\overline{\text{TRSH4}}$ latches data into the DACs. The analog output voltage range of the DACs is from 0 volts to +2.55 volts. A resistive divider network shifts this range down to -0.48 volts to +0.48 volts at the comparator inputs and provides gain and offset adjustment.

COMPARATORS

The channel 1 through 4 comparators, U200, U210, U220, and U230, convert the analog signals from the channel 1 through 4 attenuators to ECL level complementary digital signals. The 24.3K resistors from the inverted output to the negative inputs supply positive feedback and provide a fixed amount of hysteresis. The comparator outputs drive the Boolean Logic and Edge Detectors.

BOOLEAN LOGIC

The Boolean Logic is divided into two parts, function A and function B. Each function consists of two products of four bits (CH1-CH4). Each product is implemented with AND gates from U300, U302, U332, and U330 which select the channels forming the product, and with EXOR gates from U400, U410, U420, and U430, which set those channels to be active high or active low. The AND function which forms the product is a negative logic wired-AND of the EXOR gate outputs. The Boolean Logic gates are controlled by 32 lines from the Trigger Control hardware.

There are several rules regarding the control of the Boolean Logic gates. The ON lines (1AXON, 3BYON, etc.) must be low for any unused channels in a product. The $\overline{\text{INV}}$ lines ($\overline{\text{1AXINV}}$, $\overline{\text{3BYINV}}$, etc.) must be manipulated depending upon the state of the rest of the channels in the product. If any channel in a particular product is used, the $\overline{\text{INV}}$ lines of unused channels in that product (if any) must be set low. If the entire product is unused, $\overline{\text{INV}}$ must be set high for at least one channel. If a given product is edge sensitive and contains no level sensitive channels, $\overline{\text{INV}}$ must be set low for all channels in that product.

TRIGGER FILTERS

The signal path is from the wired-AND of each product through gates U402A, U412A, U422A, and U432A where the two products of each function are wire-ORed together forming signals FNA and FNB. These signals are active high (high when the function is true). The function A and B trigger filters are separate but identical, and provide amounts of time delay which track one another. The trigger filter for a given function is not operational if either product in that function contains an edge-sensitive channel or if the trigger filter is turned off. The following description for function A applies to function B as well. If both products in function A are level sensitive and the trigger filter is turned on, the control lines STAX, and STAY will be low; $\overline{\text{SYNCAX}}$ and $\overline{\text{SYNCAY}}$ will be high. The output of U500A will be high until either product becomes true. At that time it will begin to go low at a rate determined by the 470 pF capacitor and the current source from U532. As soon as it is low enough to cross the switching threshold of U500D, positive feedback from U500Ds output speeds the transition and sends a positive going signal to U402B and U412B and then a negative going signal to

U402A and U402B. This negative level enables that gate and allows the waiting signal at the other input to pass through. The principal of the trigger filter is that if the delay time caused by the capacitor between U500A and U500D exceeds the time that the product is true, the resultant function, FNA, will not become true.

When the products become false (both high), the output of U500A will go high and rapidly charge the capacitor, readying it for the next cycle.

When the trigger filter is turned off from the front panel, the lines STAX and STAY from the edge detectors will go high. This presents low levels to U402A and U412A, enabling them continuously.

If, for example, the first product contains an edge sensitive channel and the second does not, $\overline{\text{SYNCAX}}$ will go low, $\overline{\text{SYNCAY}}$ will remain high. The trigger filter is now prevented from working with the first product by U500B. The signal STAX will strobe high corresponding to the edge sensitive channel transition in the first product. The level sensitive portion of that product will be gated through at this time only.

Transistor array Q532A-E provides twin tracking dc current sources to the function A and function B trigger filters. Each current source is twice the magnitude of the current flowing into the circuit through the 330 ohm resistor and therefore dependent upon the position of the front panel potentiometer. The base-emitter voltage for U532A, B, D, and E is set by U532C. Since all transistors are closely matched, their collector currents will be equal with equal base-emitter voltages.

6 EDGE DETECTORS

There are four independent edge detector circuits, one for each product in functions A and B. The following description for the one associated with the first product of function A applies to all the others as well. The channel 1 through 4 signals and their complements are presented to the input of the multiplexer, U310. If the product contains an edge sensitive channel, the control line $\overline{\text{MENAX}}$ will be low to enable the multiplexer output; lines MS0AX, MS1AX, and MS2AX will be high or low to select the proper channel and polarity so that the multiplexer output will make a negative going transition corresponding to the channel edge to which sensitivity has been programmed. Since $\overline{\text{MENAX}}$ is low, the output of U800B is low as is pin 3 of U700B. The signal $\overline{\text{SYNCAX}}$ goes low to disable the trigger filter. With BEXTCLK high, output of U510A is low, allowing U402C and U402D to be driven by the output of U310. Before the qualifying edge comes along, the output of U310 will be high, setting the output of U402C low. When the edge arrives, U310 output will go low and the output of U402D will go high momentarily until a high level has propagated to U402C's output, at which time it will return low. The width of this pulse is determined by the propagation delay of U402C and the added delay of the series resistor and shunt capacitor between U310 and U402C. This pulse becomes the STAX signal which strobes the level sensitive portion of the trigger function on to the output. When the output of U310 goes high, the circuitry is restored to its initial state.

All four edge detectors work in unison when the external clock circuitry is activated. In this mode, $\overline{\text{MENAX}}$, $\overline{\text{MENAY}}$, $\overline{\text{MENBX}}$, and $\overline{\text{MENBY}}$ are all high but the signal $\overline{\text{EXEDGEN}}$ is low. The external clock comes in with the signal BEXTCLK. When BEXTCLK goes high the output of U510A goes low and produces a STAX pulse and the falling edge of BEXTCLK restores the circuitry as above.

When the trigger filter is turned off from the front panel, the signal FILTER OFF goes high. If, for instance, function A contains no edge sensitive channels and the external clock is not being used, $\overline{\text{SYNCAX}}$ and $\overline{\text{SYNCAY}}$ will be high. With FILTER OFF high, the outputs of U700A and U700B will go high forcing the outputs of U510A, U510B, U402C, and U412C low, and therefore STAX and STAY will be high to prevent the trigger filter from functioning.

The function B edge detectors have several minor differences from those in function A. The outputs of U422C and U432C are not wire-ORed with signals from the reset circuitry as is function A. Finally, a test bit is picked off the output of U322 through a relatively high resistance for use in self test and extended diagnostics.

7 A THEN B LOGIC AND TRIGGER I/O

A THEN B LOGIC

The A THEN B Logic passes the trigger signal from the trigger filters to the trigger outputs in one of three modes: A mode, B mode, or A THEN B mode. The mode is determined by the control lines $\overline{\text{A THEN B}}$ and $\overline{\text{A MODE}}$. In A mode, $\overline{\text{A THEN B}}$ will be high and $\overline{\text{A MODE}}$ will be low. The FNA signal from the function A trigger filter can propagate through U600B and U610D to the trigger outputs. This is possible because U520B's output is high, U520A and U610B's outputs are low, preventing U600A from latching. In B mode, operation is similar

except the signal propagates from FNB through U600C and U610D to the trigger outputs. Both control lines must be high in this mode. FNA is blocked from getting through by U600B.

In A THEN B mode, control line $\overline{\text{A THEN B}}$ will be low and $\overline{\text{A MODE}}$ will be high. An occurrence of function A will arm the trigger. The next occurrence of function B causes a trigger output pulse and resets the armed condition. In this mode, the output of U610B is initially held high. When FNA goes high, this high state is latched by U600A. Gate U600B prevents this signal from reaching the trigger outputs. However, U600C becomes enabled so that when FNB goes high, a trigger output occurs. When this happens, the output of U600C goes high, causing the outputs of U520A and 610B to go low, and resets latch U600A in preparation for the next cycle. The width of the resulting trigger output pulse is set by the propagation delays of U520A and U610B. In this mode the A THEN B GATE OUTPUT is also active. Pin 15 of U600D goes high when high when function A occurs and back low again when function B occurs. By moving a jumper on the A6 Trigger Board, a representation of the A THEN B GATE will be piped to the Front-panel TRIGGER OUTPUT connector via U610A and U620B.

TRIGGER OUT AMPLIFIER

The trigger output signal is sent to a front-panel bnc connector (as well as to the time base). With its pin 7 normally low, U620A makes the trigger output signal into complementary ECL level signals to drive the front-panel Trigger Output Amplifier. The circuit consists of one differential amplifier stage with a single-ended output whose levels are about 2 volts high, and 0 volts low from a 50-ohm source impedance.

RESET BUFFER

The function of RESET differs slightly if the 7A42 is in A THEN B mode rather than A mode or B mode. In the latter modes, when the reset input is driven high, the trigger output is simply inhibited. In A THEN B mode, in addition to inhibiting the trigger output while high, RESET causes the armed condition to be reset if it has previously been set by function A being true. After reset terminates, normal triggering can resume.

A reset input signal more positive than about 0.5 volts causes the comparator stage (Q720, Q620) to switch, pulling signals RSAX, RSAY, and pin 10 of U520D high. When the collector of Q720 goes low, trigger output is immediately inhibited by U610D. That same signal propagates through U610B to reset the A THEN B latch U600A, assuming that the signal FNA is low. This is assured by RSAX and RSAY which act on U402C and U412C to force signals STAX and STAY low. The low signal at the collector of Q720 also forces $\overline{\text{EXEDGEN}}$ low and $\overline{\text{SYNCAX}}$ and $\overline{\text{SYNCAY}}$ (on diagram 6) low to disable the trigger filter path and guarantee a false FNA.

EXT CLOCK

If the external clock is active, the control line EXT CLK SYNC will be high to present an ECL low level to U520C which enables the external clock buffers, a low to U610C which enables the edge detectors, and a low to U630 which allows the trigger view multiplexer to pass the external clock signal to the A6 Amplifier Board.

The external clock can be selected to either TTL or ECL logic levels by an internal jumper. The TTL threshold is about +1.4 volts where the ECL threshold is about −1.3 volts. The external clock signal from the front-panel bnc goes to the TTL buffer and the internal jumper. If the jumper is in the TTL position, the ECL buffer (U520C) is disconnected. The TTL buffer consists of a differential amplifier stage with some positive feedback and hysteresis. The input to the stage is clamped to +5 volts and ground to prevent overdrive. The output has ECL level voltage swings. With the ECL buffer disconnected, the output of U520C is not pulling high so the TTL buffer can drive U620A. If the jumper is in the ECL position, the external clock input is now terminated by about 50 ohms to −2 volts to be compatible with ECL logic levels. Since the ECL high and low levels are both more negative than ground, the TTL buffer is always clamped in its low input state which results in a low output from Q724, thus allowing U520C to drive U620A. The input of U520C is clamped to ground and −5V to prevent damage from overdrive. The control line EXT CLK EXER is used in self test and extended diagnostics to synthesize a low level TTL clock level. If the jumper is in ECL, the input level is already low, so EXT CLK EXER will have no effect.

The slope of the external clock is controlled by line EXT CLK SLOPE. The edge detectors are sensitive to a rising edge of the signal BEXTCLK, so U620A is set to either invert or not invert to select the desired clock edge. EXT CLK SLOPE is set high for a rising clock edge and low for a falling. If EXT CLK SYNC is not active (low), the output of U520C is forced high, and EXT CLK SLOPE is set high to assure that BEXTCLK will be high so as not to interfere with the edge detectors in channel edge sensitivity. The BEXTCLK signal is driven into the edge detectors by U510A, B, C, and D on diagram 6.

TRIGGER VIEW SELECT

If the trigger view is turned on at the front panel, the trigger view trace will be a representation of the trigger out signal sent to the time base and to the front-panel output connector, unless the external clock is active. If the external clock is on, the trigger view trace will display a representation of that signal. The selection is made by multiplexer U630D which is controlled by the EXT CLK SYNC line. If the external clock is active, the signal on route to the multiplexer is delayed by U630A, B, and C to make the external clock trace on screen line up with the other analog traces.

TRIGGER CONTROL

TRIGGER CONTROL LATCH

The trigger control latch is set by the filtered data bus FD0-FD7 on a rising edge of select line $\overline{\text{WRMD}}$. In most cases, its outputs are level shifted to drive ECL inputs as described above. The only exceptions are EXT CLK EXER and TRIGEN. When TRIGEN is driven low it causes an internal reset. This is used to inhibit false trigger outputs during the loading of trigger functions into the trigger control shift registers. After the load is complete, TRIGEN is returned high.

TRIGGER CONTROL SHIFT REGISTERS

The trigger control shift registers consist of a serial string of 48 bits which are loaded from FD7 of the filtered data bus on a rising edge of select line $\overline{\text{WRTL}}$. The TTL outputs of the registers are level shifted down to ECL levels by resistive-divider networks and sent on to the Boolean Logic and Edge Detectors. The output of the register string is buffered and sent back to the A8 MPU Board as a test bit for self test and extended diagnostics.

CPU

The 7A42 contains two separate data bus structures; an internal bus, and an external bus. The internal bus is located completely on the A8 MPU Board, and is the main data bus for the 8085A microprocessor. The external bus is used by the rest of the 7A42 and is accessed as a block of memory-mapped I/O ports. The data buses are separated in this way to minimize noise propagation through the instrument by isolating the bulk of the data I/O (i.e., RAM and ROM access) to the A8 MPU Board. This data 'traffic' is blocked from the rest of the instrument by the External Bus Buffers. The external bus also provides fault isolation so that the MPU can still run diagnostic routines if there is a fault on the external bus.

DIAGNOSTIC CONTROL

The diagnostic control circuit determines the operating mode of the 7A42; diagnostic mode (for signature analysis), or normal operation. In normal operation, the jumper selects the readout mode.

The Mode selector jumper (P540) should be in the Norm position when the 7A42 is used with any 7000-series mainframe except the 7854. If the 7A42 is being used in a 7854 mainframe, the jumper should be in the 7854 position due to the particular readout requirements of the 7854.

The other three positions of the jumper are for diagnostics purposes only; their use is described in the Maintenance section of this manual.

MPU

The 7A42 uses an 8085A microprocessor to control the low-frequency functions of the instrument (e.g., attenuator control, readout, etc.). A detailed description of the functions and command set of the 8085A microprocessor is beyond the scope, and intent, of this manual. Please refer to the appropriate data books for detailed information.

On power up, R531 and C337 hold the $\overline{\text{RESET IN}}$ input of U305 low until the power supplies have stabilized. Diode CR530 discharges C337 quickly when the $\overline{\text{RESET IN}}$ line is pulled low by the Auto Restart circuit, or in case of momentary power failure.

ADDRESS LATCH

The address latch de-multiplexes the lower eight bits of the address information from the address/data lines of the 8085A. The information on the address/data lines is latched and transferred to the lower eight address lines by the ALE signal from the 8085A.

ROM DECODER

The ROM Decoder generates the chip-select signals for the ROMs.

ROM

The ROM consists of three 8k-byte EPROMs and a socket for an additional 4k-byte EPROM (for future expansion).

RAM

The two RAM ICs provide 1k-byte of static read-write memory. This memory has an associated battery backup circuit to maintain it's contents when the mainframe power is off.

BATTERY BACKUP

This circuit ensures that valid data is maintained in the RAM by disabling the chip-select signal to the RAM chips as soon as a power-down condition is detected, and providing power from the rechargable battery to the RAM until normal power is restored.

A fully charged battery will provide back-up power to the RAM for at least 200 hrs.

EXTERNAL BUS BUFFERS

The external bus buffers provide a data path between the internal and external data buses. Latch U300 allows data on the internal bus to be transferred to the external

bus, and latch U320 transfers the data on the external bus to the internal bus. When the external bus is not being addressed, the output of U320 is disabled (three-state output) and U300 latches the external-bus data on it's output to reduce the number of transitions on the external data bus. Latch U300 also provides the extra current drive required by the additional load on the external bus.

ADDRESS DECODER

This circuit produces various enable signals based on the addresses and control signals generated by the MPU.

I/O

The I/O circuit is an eight-bit latch which holds control signals for use during the diagnostic routines.

POWER-UP RELAY DRIVE DISABLE

The output of U900A ($\overline{\text{RELN}}$) is set high on power-up or reset to disable the armature relay drives until the MPU and relay drive signals have been initialized.

AUTO RESTART

This circuit causes a hardware auto reset to the microprocessor whenever it detects that Real Time Interrupts are not being serviced in a regular manner. This should occur only when there are hardware or firmware problems in the kernel.

Refer to Figure 2-3 during the following discussion.

During normal operation, Real Time Interrupts are generated when the rising edge of astable multivibrator A8 U815 clocks D flip flop A8 U900. Shortly after the RST 5.5 interrupt is recognized by the processor, the Interrupt Acknowledge line is pulsed low to reset the flip flop.

Gates A8 U927A and U927B are cross coupled to form a set-reset flip flop. Because the output duty factor of U815 is 50%, the outputs of the set-reset flip flop will also be 50% data factor. Components R924, R925, C1000, and C1005 take the average value of the Q and Q outputs which are then diode OR-ed, and presented to the comparator. With the $\overline{\text{ARST}}$ link-plug removed (auto restart circuit enabled), the noninverting input rests about 0.7 volts above the inverting input, so that $\overline{\text{RESET IN}}$ is high, and RESET OUT is low.

If a failure or temporary fault occurs, Interrupt Acknowledge will no longer match the frequency of the astable. It may be locked low, or locked high, or occur too frequently, but in any case, the average value of either the Q or Q output of the set-reset flip flop will begin to rise. When the V- input becomes greater than the reference voltage on the V+ input, the open collector output of the comparator will pull low to −15 volts, and cause the processor to be reset.

The RESET OUT signal is fed back to the inverting input of the comparator through R1002 (for hysteresis) to ensure stable operation.

With RESET OUT high, C1005 eventually charges to a voltage greater than the V- comparator input, and $\overline{\text{RESET IN}}$ returns to a high level.

If the fault persists, the above sequence repeats, and will continue to cycle at about a 2 Hz rate until the fault is removed.

WAITSTATE GENERATOR

The waitstate generator provides a low pulse of one CLK period (approximately 0.5 μS) duration on the READY line to the MPU. This circuit is enabled (by U630, pin 11) only when the filtered data bus is addressed.

REAL TIME CLOCK

Timer U815 is wired as an astable multivibrator with a period of approximately 15 ms. The output of U815 clocks D flip flop U900B to produce the RST 5.5 signal to the MPU.

GENERAL INPUT LATCH

Latch U605 provides a means to latch signals from other circuits, and transfer them to the external data bus for inspection by the MPU.

PROBE OFFSET ACQUISITION

During probe offset acquisition, an analog-to-digital conversion of the TIP voltage is performed by the processor using successive approximation. See Figure 2-4. The processor makes a first guess at the TIP voltage by setting the output of D/A converter (U600) to it's midrange value. This is done by setting the MSB of the DAC equal to 1, and all other data bits to 0. Whether the guess is too high or too low is determined by comparator U505A, and the outcome is read by the processor on data bit 4 of the General Input Latch (U605). If the D/A output is too high, the MSB (bit 7) of the DAC is reset to 0; if it was too low, it will remain set.

Next, bit 6 is set high, with all lower-order bits remaining low, and the comparison is again checked by the processor. Bit 6 will remain set, or be reset, according to the same criteria as above.

This continues for the remaining bits, and after 8 iterations, the processor will have the 8-bit digital representation of the TIP voltage.

The usable input range at the TIP jack is ±5 volts, which is attenuated to approximately ±3.75 volts at the comparator by a resistive divider.

The output range of the DAC is 0 to 10 volts. This is level shifted and attenuated to give a range of approximately ±3.75 volts at the comparator.

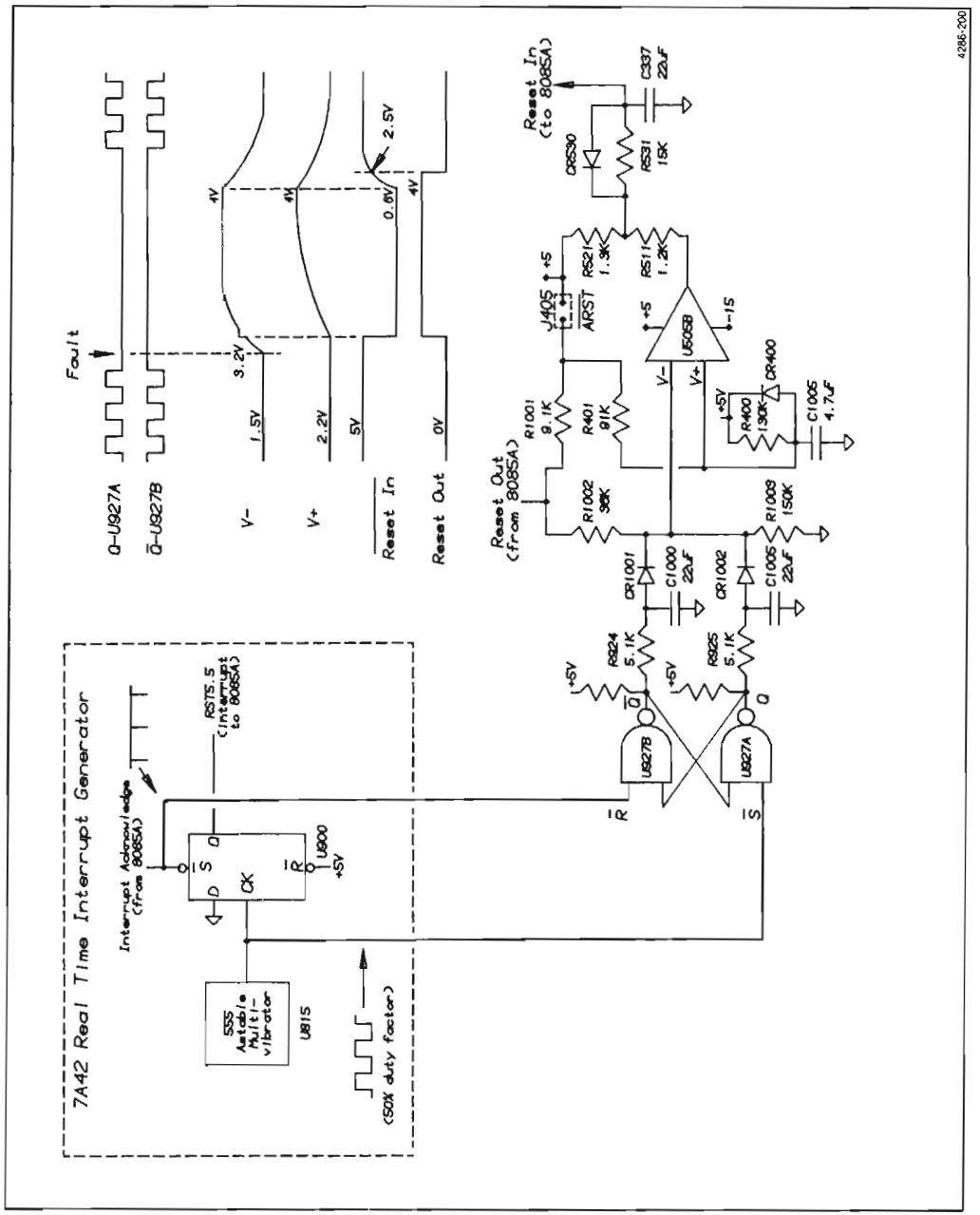


Figure 2-3. Partial A8; Auto Restart Circuit.

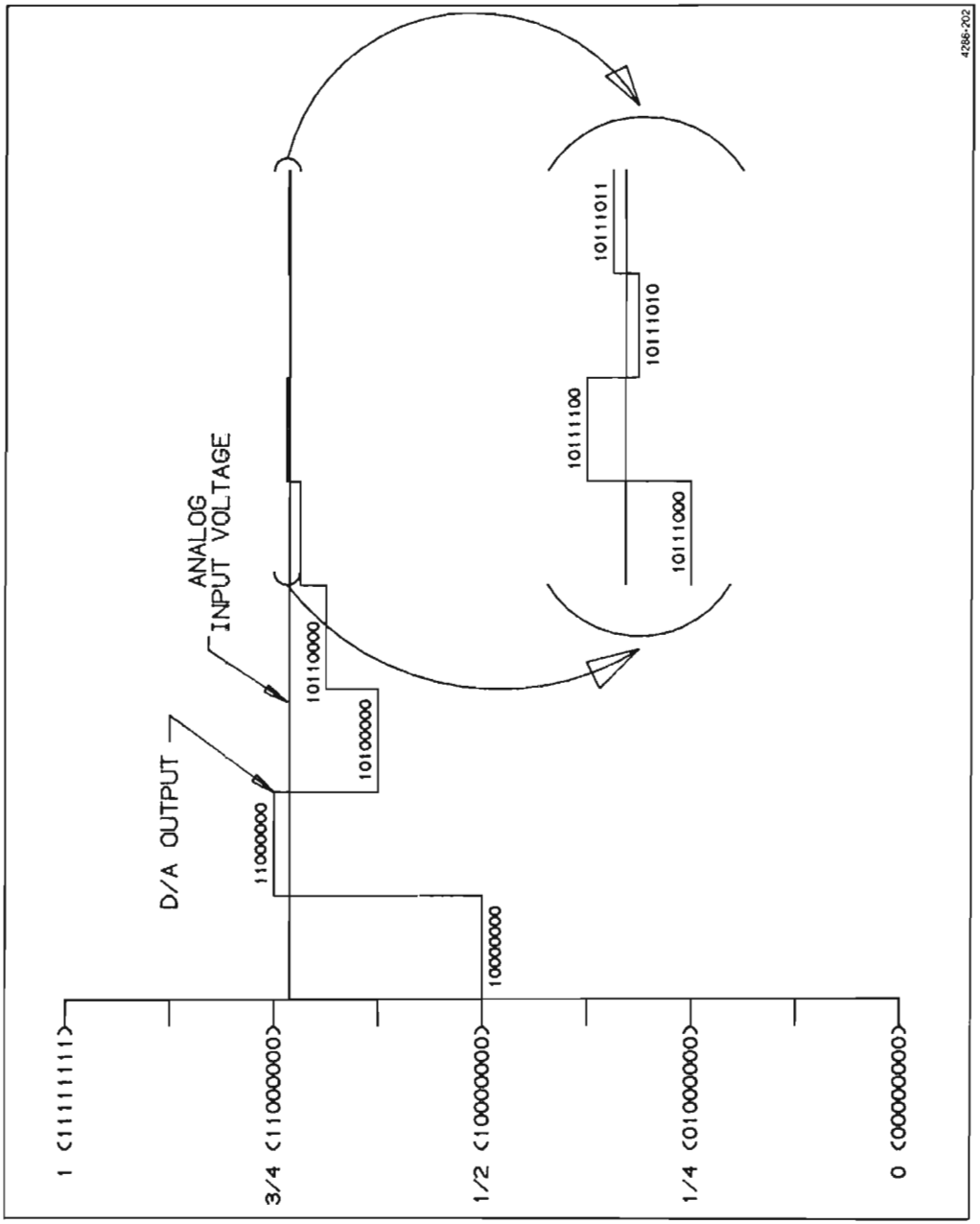


Figure 2-4. Successive Approximation Example.

Diodes CR505 and CR508 protect the comparator against over voltage. Zener diode VR510 shifts the comparator output to TTL levels.

PROBE CODING AND DIAGNOSTIC HOOKS MUX

Multiplexer U700 selects one of eight input signals to be connected to pin 13 of U605 (General Input Latch).

DIAGNOSTIC HOOKS

Quad op-amp U800 acts as a low-speed ECL-to-TTL signal translator while the diagnostic routines are running.

10 READOUT

This discussion assumes an understanding of the 7000-series readout system. Refer to a suitable mainframe service manual for background information.

The 7A42 uses the CH1 and CH2 mainframe readout positions associated with the left side of the plug-in to display vertical deflection information and error messages.

Figure 2-5 shows a timing diagram of the 7A42 readout signals.

The CH1 and CH2 readout circuitry are identical; only CH1 will be discussed here. TSX is the result of diode OR-ing the ten timeslot lines together on the A5 Amplifier board. With each falling timeslot edge, a 1.5 μs pulse (RST 7.5) is produced at the output of U830A.

The rising edge of RST 7.5 interrupts the processor, and a short time later data for the next timeslot is written to data registers U601, U600, U401, and U400. As an example, the RST 7.5 at the beginning of timeslot 9 signifies to the processor the time has come to write timeslot 10 data. This scheme of writing the next timeslots data instead of the current timeslot's data is necessary because of the high rate at which timeslots occur, relative to processor speed.

Timeslot 1 is transformed into TTL levels by Q720C and wired to the SID (Serial Input Data) input of the processor where it is used for synchronization. It is also used as an address line to the registers, and to synchronize the WA1, RA1 flip-flop.

With the exception of timeslot 1, data is always alternately written to and read from locations 0 and 1 of the registers (WA2 and RA2 = 0). Addressing is performed by D flip-flop U630 which is wired so that RA1 and WA1 will always be 180 degrees out of phase.

A complication arises when a "jump" is issued either by the mainframe or by another plug-in unit. Rather than timeslots occurring in an orderly manner, timeslot 1 may repeated up to 4 times, if three consecutive jumps occur. The 7A42 accommodates this in the following way.

During timeslot 10, the processor writes timeslot 1's data into location 2 of the registers by lifting WA2 via latch U500. With RA2 wired to SID, anytime timeslot 1 occurs, data will be read from register location 2.

The processor keeps a history of the SID line so that new timeslot data (timeslot 2 data) is written only on the first occurrence of timeslot 1 (i.e., it checks for a low SID line before writing timeslot 3 data).

Digital to Analog converters present the analog row and column currents to the mainframe.

11 POWER SUPPLY AND DISTRIBUTION

The 7A42 uses a switching power supply to develop output voltages of +5 volts, -2 volts, and -5 volts from the mainframe ±50-volt supplies. This type of power supply is used because of it's compactness and high efficiency.

POWER STAGE

This section is composed of the flyback transformer T1, and the Darlington switch (Q402 and Q500).

For high efficiency, the transistor combination must exhibit low storage time, low current rise and fall time, and low saturation voltage.

At turn-on time, Q402 saturates, Q500 is held at the edge of saturation, and approximately 100 volts is applied to the primary of T1. Current ramps-up at a rate determined by the applied voltage and the transformer primary inductance, which is about 2 mh. Switch closure duration is typically 20 μs, giving a peak current of 1 ampere.

When the switch is opened, the collector current falls and the collector voltage rises according to the transformer leakage inductance and the snubbing network. The final value of the voltage on the primary side of the transformer is the output voltage reflected through the transformer by the turns ratio.

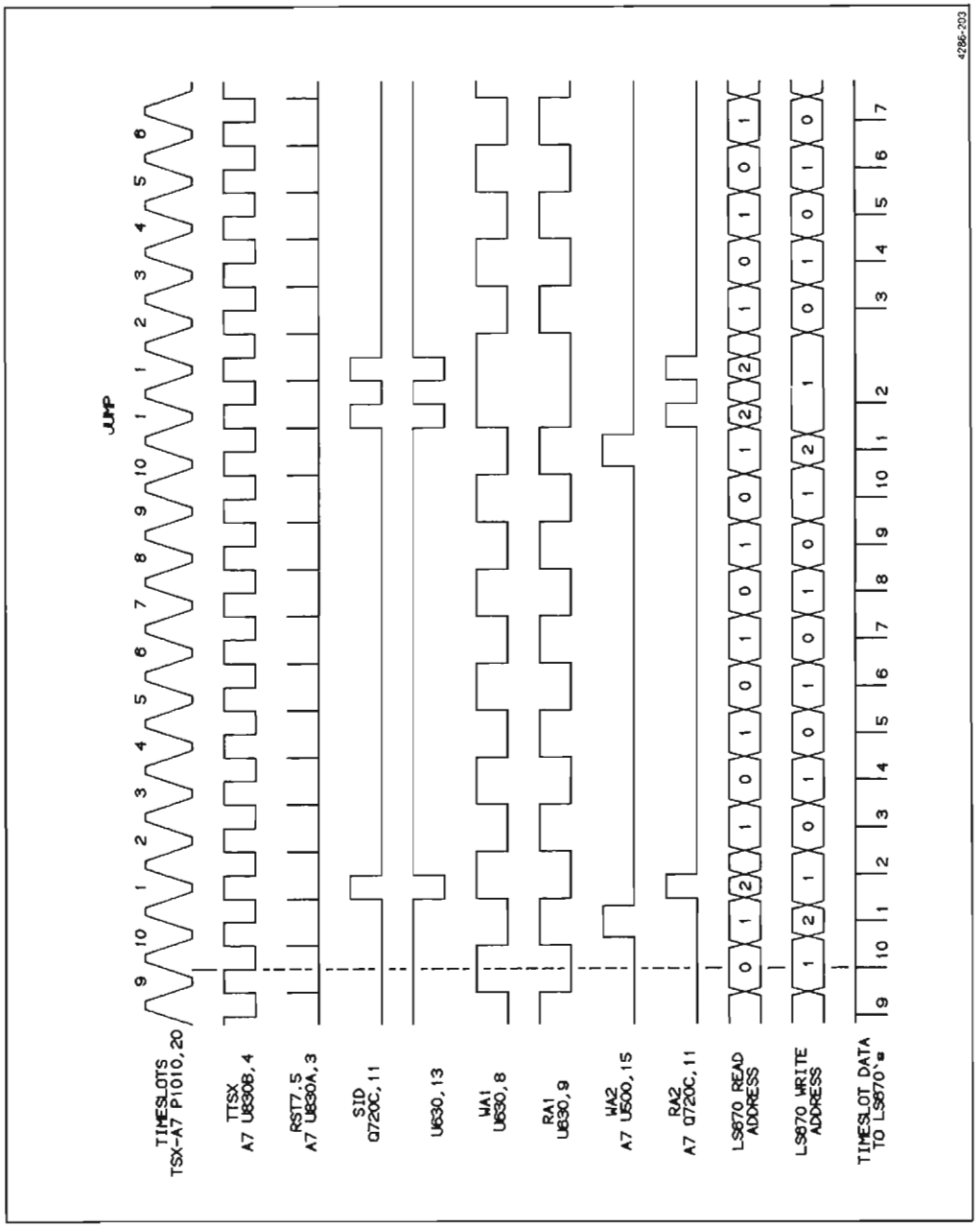


Figure 2-5. 7A42 Readout Timing.

Resistors R405 and R401 discharge the base storage capacitance of Q402 and Q500 to reduce turn-off time.

RECTIFIERS AND FILTERS

Diodes CR410, CR520, and CR620 are used to rectify the square-wave output. Schottky diodes are used here because of their low forward-voltage drop and low storage time.

The output pi filters reduce the ac component of the rectifier output voltage and reduce supply output impedance at higher frequencies where regulator loop gain begins to fall.

Special consideration is given to the selection of C410, C530, and C630 regarding equivalent series resistance (ESR). Peak current values of 1 to 5 amperes are typical and without low values of ESR, excessive heating will occur.

CURRENT LIMIT

The current limit circuit senses excess primary current. When a fault is detected, it clamps the PWM comparator input to ground, causing the supply to shut down for about 100 ms. It then releases the comparator and allows the supply to attempt to recover. With a short circuit on the secondary side, the Current Limit will cycle at about 10 Hz.

Current limiting occurs when the primary current through R410 exceeds about 1.2 amperes. Transistors Q100 and Q200 are turned on by Q313 and Q317 when the maximum primary current is exceeded. When Q100 turns on, Q300 also turns on, pulling the base of Q100 high. This keeps Q200 saturated, and the supply down, while C200 charges.

INPUT FILTER

Because the transformer primary current is discontinuous and contains some high-amplitude, high-frequency harmonics, the ±50-volt mainframe power supplies are decoupled from the 7A42 switcher by C220, C330, C325, and L220.

Due to the highly capacitive load on the ±50-volt supplies, surge current may cause the mainframe power supply to current limit when the instrument is turned on initially. Diode CR230 keeps C220 from discharging between attempts to start the mainframe power supply.

PULSE WIDTH MODULATION (PWM) CONTROLLER

The primary function of the PWM integrated circuit is to monitor the -5 volt output and adjust the duty cycle of the power stage so that the secondary output voltages are maintained at constant values under varying load conditions.

The -5 volt output is level shifted through R119, R122, and R125 to +2.5 volts and presented to the noninverting input of the error amplifier where it is compared to the +2.5 volt reference level. The reference is determined by the +5 volt reference from the PWM IC and the 2X divider R120 and R121. The output of the error amplifier is compared to the 20 kHz free-running oscillator output which is a ramp whose frequency is set by R218 and C105. It is the output of this comparator which determines the duty cycle of the power stage. Under normal operating conditions, the duty cycle is about 38 percent. (The Darlington switch is ON about 38% of the time, and OFF about 62% of the time.)

Stability of the regulator is ensured by R109 and C108 at the error-amplifier output.

Components R105, C115, CR110, and CR111 are used to "soft start" the switcher when mainframe power is initially applied. This prevents excessively high current in the power stage.

When power is initially applied to the 7A42 through it's host mainframe, C115 is fully discharged and the output of the error amplifier is clamped to ground through CR110, thus disabling the regulator. As C115 is charged through R105, the duty cycle slowly increases until it reaches it's steady state value. The capacitor is charged to a final value of +5 volts and under normal operation is disconnected from the error-amplifier output by CR110. In the event that mainframe power momentarily drops, or cycles, CR111 quickly discharges C115 to ensure soft start when power returns.

DRIVERS

These three transistors provide the necessary current drive during ON and OFF times to control the power stage.

At turn-on, the PWM output transistor saturates, resulting in C2 (pin 13 of U210) and E2 (pin 14 of U210) being at about 3 volts. Transistor Q315, in a common base configuration, supplies about 15 ma of base drive to Q402 throughout ON time. Additional current drive is provided by Q305 through C301 to quickly turn the Darlington on. Resistor R301 discharges C301 to 0 volts during the OFF time.

Previous to the turn-off signal from pin 13 of U210, Q312 is off, and it's collector is biased to approximately -42 volts by divider R225, R226. Capacitor C122 is charged to about 7 volts through CR406 and CR407. When turn-off occurs, Q312 saturates and the base of Q402 is pulled to about -55 volts through the capacitor. This causes the stored charge in the base of Q402 to be removed quickly, decreasing the total turn-off time. The capacitor is tied to the base of Q402 through CR121, which prevents the divider from turning the Darlington on during the OFF time.

SNUBBER

Because the transformer is non-ideal and contains leakage inductance, some means to protect the Darlington pair, Q402 and Q500, against avalanche and secondary breakdown is needed. The reactive snubber is used to limit the flyback voltage to prevent breakdown, and to shape the switch's load line during current fall time to minimize it's power dissipation.

First, assume Q402 and Q500 are saturated and receive a turn-off signal at the base of Q402. A storage-time delay later, the collector current begins to decrease and the current in C405 begins to increase an equal amount. Over this time frame, the transformer's primary current remains approximately constant. As the collector of the Darlington rises to a peak value of approximately 150 volts, C405 is charged to about 100 volts and remains at that value until turn-on time. Note that during the time C405 is charging, not only does the snubber control the manner in which the collector voltage rises, but also, a portion of the energy stored in the transformer's leakage inductance, which would otherwise be lost, is returned to the +50V supply.

At the switch's turn-on time, C405 and L310 are paralleled through Q500 and the voltage at the cathode of CR402 is -150 volts. This voltage rises to a peak value of nearly +50 volts when the current through L310 and C405 attempts to reverse, but is blocked by CR402. During this portion of the cycle, the voltage on C405 is always restored to a value of something less than 100 volts.

Notice that, had the voltage stored on C405 during flyback been greater than 100 volts (at the switch turn-on time), the LC tank would have tried to ring higher than +50 volts but would be clamped by CR400.

ATTENUATOR SUPPLIES

Operational amplifiers U300 and U310 form an individual set of -5 and -11 volt power supplies for each of the four attenuator modules. The supplies are separate from each other to help minimize crosstalk, and to provide individual offset adjustment as needed.

The -5 volt supply is generated at the output of an operational amplifier with a gain of -1, by using +5 volts as a reference. The -11 volt supply is adjustable to compensate for any variations in the +5 volt and -5 volt supplies. This is done to prevent drift in the attenuator impedance converter, caused by power-supply variations. Since all the supplies track each other, drift from this source is reduced.