CIRCUIT DESCRIPTION

Introduction

This section of the manual contains a description of the circuitry used in the SG 503 Leveled Sine Wave Generator. Individual descriptions are separated into the following parts: Oscillator Circuits, Output Buffer Amplifier and Filter, Leveling Circuitry, Display Flash Multivibrator, 50 Ohm Wideband Attenuators, and Power Supplies. Diagrams 1 and 2 are segmented with gray-tint blocks according to circuit function. Circuit block titles correspond to those listed in the Block Diagram. Refer to appropriate diagrams in the Diagrams section of this manual while reading the circuit description.

Oscillator Circuits ◇1◇4

Both oscillator sections, Q130 and Q140, are common-base Hartley configurations with inductive feedback (tapped coils for each frequency range). Amplitude control is accomplished by varying the dc emitter currents. Q300 operates as a variable current source, with its collector current controlled by the output of operational amplifier U280.

The oscillators operate in a non-linear mode (Class C) and the collector current for Q130 or Q140 is a series of pulses at the operating frequency. This series of pulses contain a large number of harmonics and a high Q parallel resonant tank circuit is required to obtain a good sine wave output. The tapped coils allow the highest possible operating Q factor at a given supply voltage and collector-base breakdown rating for the transistors. Spurious oscillations are reduced by the L/R combinations in the collector lead for each transistor.

For those coils that have tuning slugs, the slug position determines the inductance, coupling between windings (leakage inductance) and the Q factor for the oscillating circuit. All of the above factors combine to determine the frequency range, harmonic suppression and maximum available output amplitude.

Output Buffer Amplifier and Filter ◇1

Signals from the oscillator sections are applied via a 100 ohm strip line to the base of Q190. The output of Q190 feeds a low-pass filter which has a cut-off frequency of about 300 megahertz.

Harmonic distortion is generated in the oscillator circuits and also in the Output Buffer Amplifier. At low frequencies, the Output Buffer Amplifier is practically ideal and contributes negligible distortion. However, at higher frequencies distortion increases and becomes more critically dependent on the collector current operating point for Q190. By choosing a frequency where the oscillator signal is fairly clean, most of the observed distortion will be due to the Output Buffer Amplifier. The collector current can then be set for minimum distortion by the adjustment of R175. Distortion is also somewhat dependent on the drive level to Q190. The final adjustment of R175 should result in minimum distortion over the full amplitude range from 0.5 volt to 5.5 volts, establishing a collector current operating point which falls in the 80 to 110 milliamp range.

Leveling Circuitry ◇1

The leveling circuitry is composed of a reference voltage divider, a hybrid peak-to-peak detector, temperature compensation diodes CR216-CR218, and error amplifier U280 with its associated components.

The major components of the hybrid peak-to-peak detector (U225) are diodes CR225A and CR225B with their associated storage capacitors, C225A and C225B, coupling capacitor C225C and output resistor R225A. The peak-to-peak detector produces a dc output across C225A and C225B that is approximately equal to the peak-to-peak voltage at the leveling point (junction of C225C and R225A).

To aid in understanding operation of the peak-to-peak detector, assume perfect diodes, 10 volts peak-to-peak at the leveling point and the reference voltage (set by R260) disconnected. C225A would charge by normal rectifier action to −5 volts dc and C225B to +5 volts dc. If the reference voltage level set by R260 is −10 volts and now applied to C225A (series opposing) the dc levels on C225A, C225B and coupling capacitor C225C will shift by an amount equal to one half the peak-to-peak amplitude at the leveling point. There will now be zero volts dc across C225B, −10 volts dc across C225A, and coupling capacitor C225C will be charged to −5 volts dc. The sinewave at the junction of the two diodes is now centered at −5 volts dc. For an actual complete circuit with non-ideal diodes, the potential difference between C225A and C225B is about equal to the peak-to-peak amplitude at the leveling point.

Because the reference voltage and the dc output of the peak-to-peak detector are connected series opposing, any algebraic difference between these two voltages will be applied to the input of error amplifier U280. When the generator output is leveled, equal dc potentials (about −.7 volt dc) exist at the − and + input terminals of U280 and the system is stabilized.

If the peak-to-peak output amplitude from an oscillator section changes for any reason, a corresponding change in detector output produces an error signal at the − input terminal of U280 which is converted into a collector current change in Q130 or Q140 in such a direction to restore the original peak-to-peak amplitude at the leveling point.

The high-gain leveling system (closed loop) establishes a steady state impedance point at the junction of C225C and R225A which approaches zero ohms. R225A, therefore, sets the generators output impedance and reverse terminates a 50 ohm coaxial cable.

CR200, CR202, VR200 and VR202 reduce transients which can be caused by sudden load changes, while R278, R276, CR276 and CR274 reduce switching transients when changing frequency ranges.

Display Flash Multivibrator ◇1

Q296 and Q290, with their associated components, is a multivibrator circuit that is held in a normally stable state as long as the sine-wave output amplitude is leveled. If the output is not leveled, pin 6 of U280 swings positive with respect to ground and turns on CR280. The multivibrator then operates as an astable circuit with a period of about 2 hertz. The waveform at the collector of Q290 is applied to pins 6 and 7 of U490 (State Generator). This signal causes binary zeros to be supplied to the Display Drivers, which turns off the display. The result is a visible flashing of the front panel LED display.

50 Ohm Wideband Attenuators ◇1

In the X1 position of the AMPLITUDE MULTIPLIER switch, the output signal bypasses the hybrid chip attenuators.

The hybrid chip attenuators (U245 and U240) are labeled on the circuit board as "X.1 & X.01" and "FIRST ÷ 10, X.01".

In the X.1 position of the AMPLITUDE MULTIPLIER switch, U245 divides the generators output by 10.

In the X.01 position of the AMPLITUDE MULTIPLIER switch, U240 divides the generators output by 10 and then U245 divides again by 10 for a total division of 100.

In the X.1 and X.01 positions of the AMPLITUDE MULTIPLIER switch, the 50 ohm attenuators provide additional isolation between the oscillators and a large mismatched load.

Auto-Ranging Counter ◇2 ◇3

(For Instruments SN B060000-above.) The input circuit to the Auto-Ranging Counter is through emitter-follower Q320, which provides a low impedance drive to Q350. Transistors Q350-Q360 and Q330-Q340 is a dual-differential amplifier that provides high gain in two stages. R351-R361 and R332-R334 are the constant-current sources for the respective amplifier, while C340 and C350 serve to stabilize the operating points of the amplifiers. The output signal amplitudes on pins 6 and 7 are constant-amplitude square waves, regardless of the input amplitude to Q320.

A 1-volt peak-to-peak square-wave signal from Q340 is applied to a divide by 8 prescaling circuit consisting of U390, U400A, and U400B (each IC divides by 2) and to the base of Q410. The positive-going edge of the signal at pin 7 of U390 and the negative-going edge of the signal at the base of Q410 are significant to the counting operation. Signal prescaling does not occur for the 50 kilohertz reference frequency or for other frequencies up to and including .999 megahertz.

(For Instruments SN B059999-below.) The input circuit to the Auto-Ranging Counter is through emitter-follower Q320, which provides a low impedance single-ended drive to U350. U350 is a dual-differential amplifier that provides high gain in two stages. R335 and R342 are the constant-current sources for internal emitter connections and the output voltage on pins 6 and 7 start to limit at low input amplitudes. The emitter currents are set for about 8 milliamps, providing symmetrical output signal amplitudes of about 800 millivolts across R358 and R362. L362 is used to boost the high-frequency signal amplitudes to the prescaling circuitry.

Signals from U350 are applied to a divide by 8 prescaling circuit consisting of U390, U400A, and U400B (each IC divides by 2) and to the base of Q410. The positive-going edge of the signal at pin 7 of U390 and the negative-going edge of the signal at the base of Q410 are significant to the counting operation. Signal prescaling does not occur for the 50 kilohertz reference frequency or for other frequencies up to and including .999 megahertz.

A self-biasing arrangement is provided for U390 to ensure that the input bias level on pin 7 is always centered in the hysteresis window. The average of the complementary outputs on pins 2 and 3 is obtained from the junction of R396 and R398 and fed back to pin 7 through L365 and R365 to automatically compensate for any internal temperature drift.

Four counters, U430, U435, U436 and U437 are used for the counting process, but only three decimal digits are displayed on the front panel after the bcd data has been decoded by the bcd-to-Seven Segment Decoder Drivers. U430 frequency divides the input by 10 and its output is used to round off the count held in the remaining counters, allowing a more accurate three-digit display.

The 1 MHz reference clock circuit, U460A and U460B, with inverter U460D, drives U465, which produces two functions. Frequency division by 16 and frequency division by 2 produces a clock signal with a period of 16 microseconds on pin 11 and a clock signal with a period of 2 microseconds on pin 12.

U455B, U455C, U455D, and U460C are positive NAND gates. The logic levels at pin 5 of U455B and pin 10 of U460C determine whether a clock signal with a period of 16 microseconds or 2 microseconds appears at the output of U455D. These logic levels are determined by the output level of positive NAND gate U455C and inverter U455A.

When the FREQUENCY RANGE (MHz) control is in the REF ≈ .05 position, pin 1 of U445A and pin 13 of U445B are held LO (= 0) by the closure of S100-2. This clears U445A and U445B, setting both Q terminals (pin 6 of U445A and pin 8 of U445B) to a HI (= 1) level. A HI level is established on pins 9 and 10 of U455C, setting its output to a LO level. A LO on pin 5 of U455B locks out the clock signal with a 16 microsecond period, while the HI level on pin 10 of U460C allows the 2 microsecond clock to be gated through to the output of U455D.

The HI level on pin 10 of U460C is also transmitted through VR475, reverse biasing CR410 and disabling the divide by 8 signal prescaling circuitry. The 50 kilohertz signal is then processed by Q410 and Q420 with the positive-going edge of the signal at pin 1 of U425A significant to counting operation only during the time that pin 2 of U425A is HI (gating signal).

For 50 kilohertz counting, the 10^{-1} decimal source point (anode of VR475) is always HI and the 2 microsecond clock signal is frequency divided by 1000 by Gate Time Clock Dividers U480, U481, and U482. Positive NAND gates U475A, U475B and U475D are locked out due to the LO levels set at the output of inverting input AND gates U450B, U450C and U450D. With pins 10, 9 and 13 of U485B set to a HI level by the Q terminals of U445A and U445B, a 2000 microsecond clock signal is gated through U485B and U485A to pin 1 of U490.

(Refer to Fig. 5-1 for waveform time relationships involved with the State Generator circuits.) If the leveling circuitry is operating properly, a HI level is set on pins 6 and 7 of U490, allowing it to count. U490 frequency divides by 5 from pin 1 to 11 and frequency divides by 2 from pin 14 to pin 12. This frequency division produces a signal with a period of 10 milliseconds at pin 11 and a square wave with a period of 20 milliseconds at pin 12. The square wave signal (50% duty cycle) on pin 12 is the reference waveform for the counting period, display time and counter reset time.

The square-wave signal on pin 12 of U490 is applied through inverter U432A to pin 2 of positive NAND gate U425A with the positive half of the square wave acting as a gating signal that allows the counters to count for 50% of the total period (10 milliseconds for 50 kilohertz counting).

If the sine wave output amplitude from the SG 503 is not leveled, pins 6 and 7 of U490 goes negative at approximately a 2 hertz rate. The result is a blinking front-panel display because U490 is cleared to zero. Zeros supplied to pin 10 of the Display Drivers (U510, U520, and U530) causes them to blank the display for about 0.25 second.

The Auto Ranging circuits operate when S100-2 is open to change the output levels of U455C, U450B, U450C, and U450D at the proper time to set the decimal point in its proper location and to select the proper gate time intervals for the counting, display, and reset process.

Only one decimal point shift (from .999 megahertz to 1.00 megahertz) will be discussed as the operation is similar for other decimal point shifts. Overflow Detector U440A detects when it is necessary to shift the decimal point as frequency is increased, while U440B detects when it is necessary to shift the decimal point as frequency is decreased.

U445A and U445B operate as a 4-bit shift register (memory). Exclusive—OR gates U438A and U438B act as control devices to determine whether the register shifts right or left to produce the proper output data, thereby speeding up the Auto Ranging process.

Frequencies from .250 megahertz up to and including .999 megahertz do not cause the output data from U445A and U445B to change state. Consequently, the output level of U455C remains LO for these frequencies and the gating signal at pin 12 of U490 is the same as for 50 kilohertz counting.

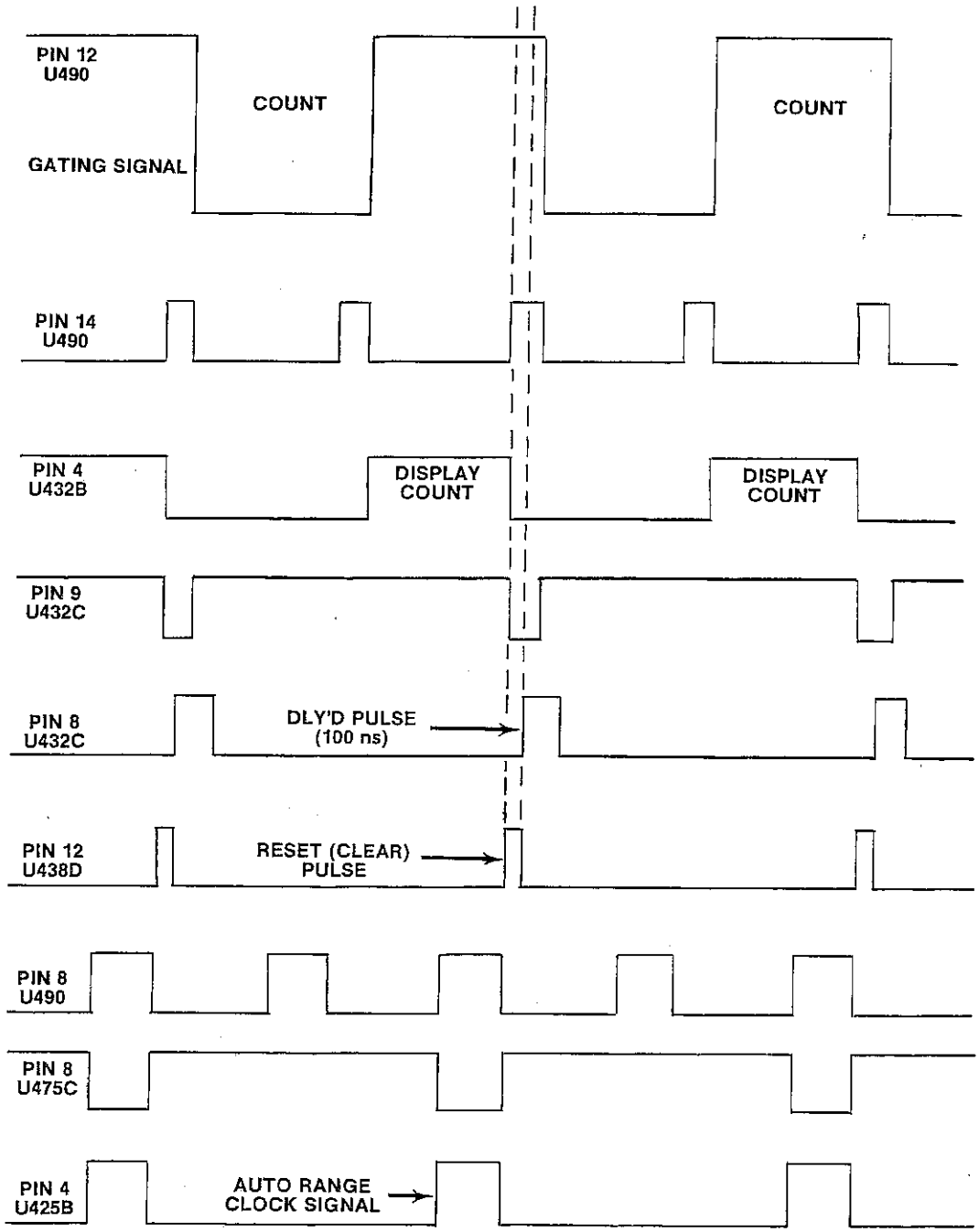

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Fig. 5-1. State Generator waveform time relationship.

When U436 and U437 contain binary data equivalent to decimal 99, the next input count to U435 causes pin 11 of U436 to go negative and triggers U440B to force pin 9 of U440B to a HI (= 1). When U435, U436 and U437 contain binary data equivalent to decimal 999, the next input count to U435 causes pin 11 of U437 to go negative and triggers U440A to force pin 13 of U440A to a LO (= 0). At the transition point from .999 megahertz to 1.00 megahertz U440B and U440A have been triggered and set.

A HI on pin 9 of U440B along with a HI on pin 6 of U445A and a LO on pin 9 of U445B results (through the action of U438A and U438B) in a HI (= 1) being transferred to the D input terminal (pin 2) of U445A and a LO (= 0) to the D input terminal (pin 12) of U445B. Pin 5 of U425B (Auto Range Clock Enable) has also been set to a HI through the action of U425D.

On the next Auto Range Clock signal from U450A, pin 6 of U425B goes LO and this negative transition triggers both U445A and U445B, transferring the data from the D terminals to the Q terminals. After data transfer, pin 6 of U445A will be LO (= 0) and pin 5 will be a HI (= 1); pin 9 of U445B will be a LO (= 0) and pin 8 will be a HI (= 1). These logic levels are decoded by U455C, U450B, U450C and U450D to shift the decimal point one place to the right, select the proper gating signal from the Gate Time Clock Dividers, and enables the signal prescaling circuitry.

For the logic levels given, the 2 microsecond clock signal is locked out from U460C and the 16 microsecond clock signal is gated through to the output of U455D. After frequency division by 100, a 1600 microsecond signal is gated through U475D and U485A to appear at pin 1 of U490. U475D is enabled because the output of U450B is HI and all other decoding gate output levels are LO. Although new gate time intervals are selected for Auto Ranging, the waveform time relationships remain the same as illustrated in Fig. 5-1.

Due to the change from a HI to a LO on pin 6 of U445A, the output level of U438B goes HI during the count interval. The output of U440A is now at a HI level because it was reset by the clear pulse and not triggered during count time. This results in a LO level at pin 5 of U425B, which locks out the Auto Ranging clock signal, preventing U445A and U445B from being triggered. U445A and U445B will not change their output data unless it again becomes necessary to change the decimal point location.

For the next decimal point shift (for example, from 9.99 megahertz to 10.0 megahertz), the same sequence of events occur with Exclusive-OR gates U438A and U438B sensing the previous output data of the 4-bit register. The proper binary code is then set at the outputs of U445A and U445B (when triggered by the Auto Ranging clock signal) to shift the decimal point one more place to the right. U475A is enabled by the output level of U450C going HI and a 160 microsecond clock signal is gated through to pin 1 of U490.

Power Supplies 3

The −22 V supply is referenced to ground with a reference voltage point established on pin 5 of voltage regulator U695 by the voltage divider action of R697 and R698. The voltage divider composed of R693, R694 and R695 establishes a voltage sensing point at pin 4 of U695. U695 regulates its output by comparing the voltage level on pin 4 with an internal reference. R694 (−22 V ADJ) sets the quiescent level at the base of Q685 which, in turn, sets the quiescent current level through the PNP series-pass transistor located in the power module mainframe. If the −22 volt output level starts to go positive, this change is sensed at pin 4 of U695 and pin 9 of U695 goes negative. This voltage change is transmitted through emitter-follower Q685 to the base of the PNP series-pass transistor, causing it to increase conduction through the load and return the output level to −22 volts. Q690 operates as a load current limiter with R680 acting as the current sensing element.

The +5 V supply is referenced to the −22 V supply with the reference voltage point established at pin 3 of U610 by voltage divider R610-R612. This reference level is about −5 volts. In a quiescent state, the voltage on pin 2 of U610 is also about −5 volts. If the +5 volt output level goes more positive, the voltage change appears at pin 2 of U610 which amplifies and inverts the signal to apply a negative change at the base of Q610. VR610 operates only as a dc level shifter. A positive voltage change at the base of Q600 causes the base of the NPN series-pass transistor located in the power module mainframe to decrease conduction through the load, returning the output level to +5 volts. Q620 is for current over-load protection. If the load current exceeds about 1.8 amps, R624 acts as a current sensing element to turn on Q620. If Q620 turns on, its collector goes positive, turning on CR612. A positive voltage change at pin 2 of U610 turns off the NPN series-pass transistor. The non-polarized connections for C620 and C619 integrate T^2L spikes which may occur on the +5 volt level, preventing them from turning on Q620 and shutting down the power supply during current surges.

CR640 prevents the +5 V supply from going more negative than about −0.7 volt if F620 opens. Q640 protects the load from over-voltage conditions that could occur if the NPN series-pass transistor shorted. If the output level exceeds about 6.2 volts, VR640 conducts, developing a SCR gating signal across R640. This gating signal turns on Q640, clamping the output level to about +0.2 volt.