Microwave Technology at Tektronix

A High Performance Transportable Microwave Spectrum Analyzer

Digital Storage for a Microwave Spectrum Analyzer

A Phase Lock Stabilization System for 30 Hz Resolution at 12 GHz

Two New Graphic Display Modules for the OEM System Designer

Volume 9
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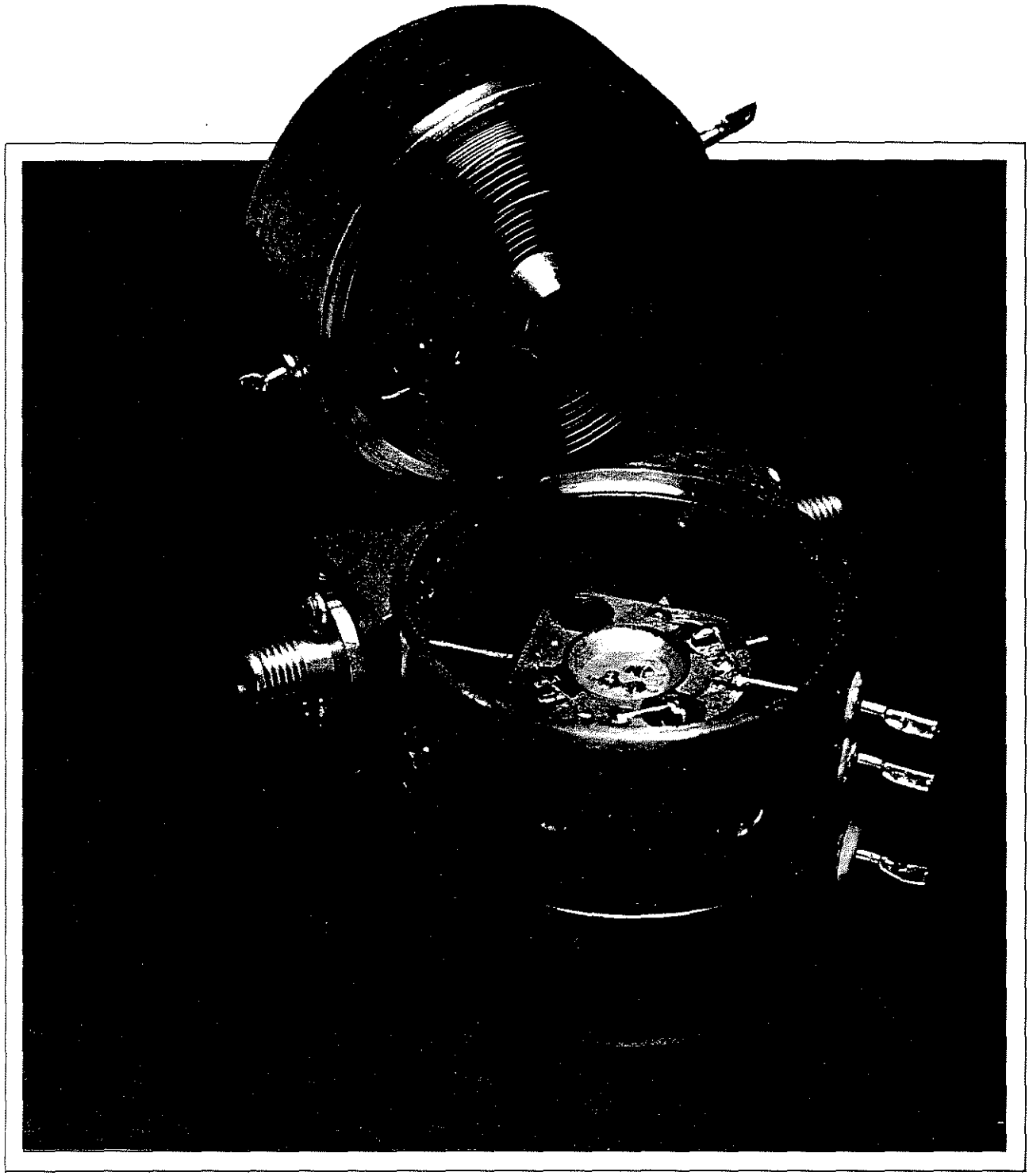
Tekscope



Tektronix®

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Tekscope

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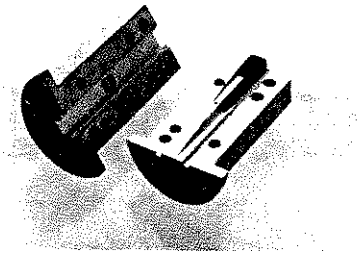
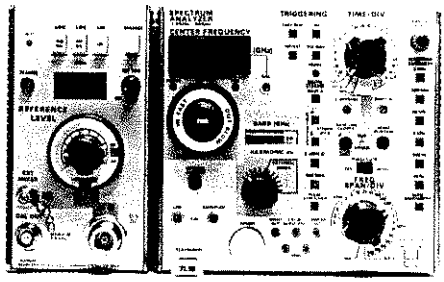
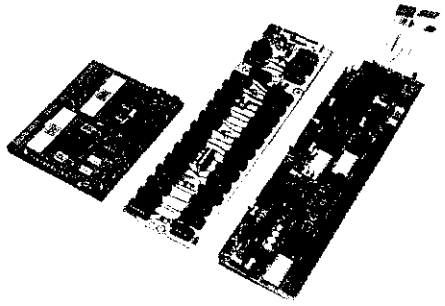
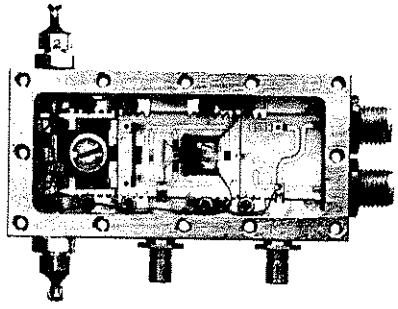
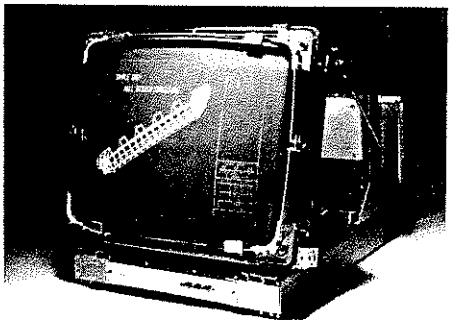










Tekscope is a bimonthly publication of Tektronix, Inc. In it you will find articles covering the entire scope of Tektronix' products. Technical articles discuss what's new in circuit and component design, measurement capability, and measurement technique. A new products section gives a brief description of products recently introduced and provides an opportunity to request further information.

To better serve customers who maintain their TEKTRONIX instruments, the service information formerly appearing in Tekscope will be expanded and published in a publication dedicated to the service function.

COVER

The three-sphere YIG preselector in the 7L18 provides spurious-free performance from 1.5 to 18 GHz and allows accurate amplitude measurements while still in the signal path.

Tektronix®
COMMITTED TO EXCELLENCE

Microwave Technology at Tektronix

Some thirty years ago, when Tektronix started in the instrument business, most oscilloscopes were indicating devices. With the development of regulated power supplies, triggered calibrated time bases, and integral calibrated signal sources, the oscilloscope was transformed from an indicating device into a measurement device.

Standard components were used to build the unique circuits designed by the engineers, and about the only parts fabricated by Tektronix were the chassis, cabinets, and front panels.

It soon became evident that if oscilloscope performance was to continue to advance, improvement in the components available was essential. And so we set about designing and building better cathode ray tubes, developing more stable timing capacitors, winding highly reliable low- and high-voltage transformers, developing low reactance potentiometers for attenuators, and designing distributed terminations for wideband amplifiers. Special coaxial cable with a high resistance center conductor was conceived to stretch the bandpass of passive probes. And new devices and techniques for mounting components shortened manufacturing times and improved serviceability. Innovation continued until, today, the state-of-the-art oscilloscope is vastly different from that of thirty years ago.

Progress in spectrum analyzers and other microwave products at Tektronix is following much the same pattern. State-of-the-art performance is being achieved through innovative circuit design and the development of new and improved microwave components.

Working with frequencies in the microwave region requires special skills. Materials exhibit a different set of characteristics at gigahertz frequencies, and physical dimensions and surface conditions become important design considerations.

A very capable team possessing the unique skills needed, is involved in the development of new microwave devices at Tektronix, from the concept stage through manufacturing and evaluation of the finished product. Their design skills are augmented by modern computer technology employing programs such as COMPACT, SPICE, and GLUMP—a TEK-developed program.

Sophisticated processing facilities are required to implement the exotic designs of the microwave engineers. Precision machining, chemical milling and plating, advanced thin and thick film hybrid technology, and integrated circuit design and manufacturing all contribute to the success of the effort. Innovative people in each of these areas regularly respond with unique solutions to difficult problems.

Thin film technology at Tektronix is exemplified by the thin film assembly shown in figure 1. Resident on the 3″ x 3″ quartz substrate are fifty circuits, each containing three capacitors and two resistors. Metal conductors are laid down on the quartz substrate using a proprietary process which yields low-resistance, well-defined conductors that can be soldered, wire bonded, die attached, or gap welded. The deposited resistors are heat treated in a high-temperature bake to achieve the desired resistivity within ± 5%. Laser trimming is not used as it disturbs the pattern–an undesirable situation for geometry-sensitive microwave devices. Passivation is performed using a pinhole-free organic material that provides a high voltage dielectric for the capacitors deposited on the substrate. Breakdown voltage is in excess of 500 volts, and dielectric losses at microwave frequencies are substantially less than can be achieved with silicon passivation.

New techniques for mounting microwave substrates have also

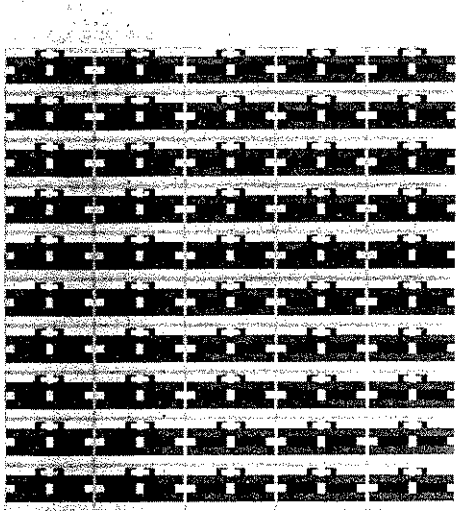


Fig. 1. Thin film technology at Tektronix is exemplified by this 3" by 3" quartz substrate which contains fifty circuits, each consisting of three capacitors and two resistors. Resistors are brought to the desired value by high-temperature bake rather than by laser trimming.

been developed. Microstrip (conductor above ground plane) becomes very lossy above about 8 GHz. A suspended substrate technique is used that completely encloses the substrate with ground, thereby greatly reducing rf losses. This technique is merged with stripline to produce a balanced distributed transmission medium that can be designed to create complex microwave assemblies such as mixers, amplifiers, oscillators, etc.

Augmenting the device development and processing areas is a well equipped and competently staffed microwave component assembly area. Electrical performance is directly related to tolerances on most mechanical parts used in microwave assemblies. An excellent example of this is the three-sphere YIG-tuned preselector that gives the 7L18 its excellent wide-band spurious-free calibrated performance. YIG-tuned filters are not new; what is unique is the precision with which the elements of the filter are assembled, and processing of some of the materials.

Optimizing frequency tracking between the three filter sections requires extreme care to ensure that the pole pieces are parallel and the YIG spheres are equidistant from the axial centerline of the pole pieces. Another important consideration is the orientation of the YIG spheres to minimize the effects of temperature and magnetic field variations. A mechanically complex fixture is required to attach a YIG sphere to a beryllia rod so the sphere can be rotated about the 100 crystallographic axis. This allows the sphere to be rotated so the best possible axis, the 0, 8, 13, can be aligned parallel to the applied magnetic field.

Other considerations such as minimizing spurious modes and coupling variations call for special attention to the design and orientation of the coupling loops and cavities associated with each sphere.

The external waveguide mixers that allow 7L18 users to perform accurate measurements to 60 GHz

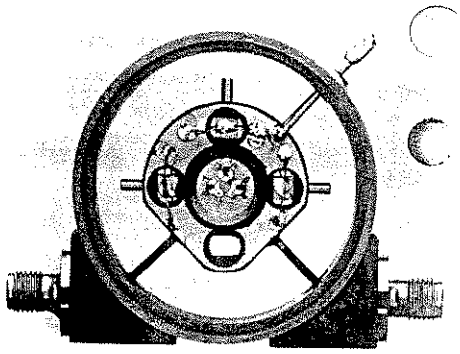


Fig. 3. Advanced YIG-tuned filter design yields wide-band spurious-free operation. Critical alignment and orientation of the YIG spheres and coupling loops are essential in achieving the best performance.

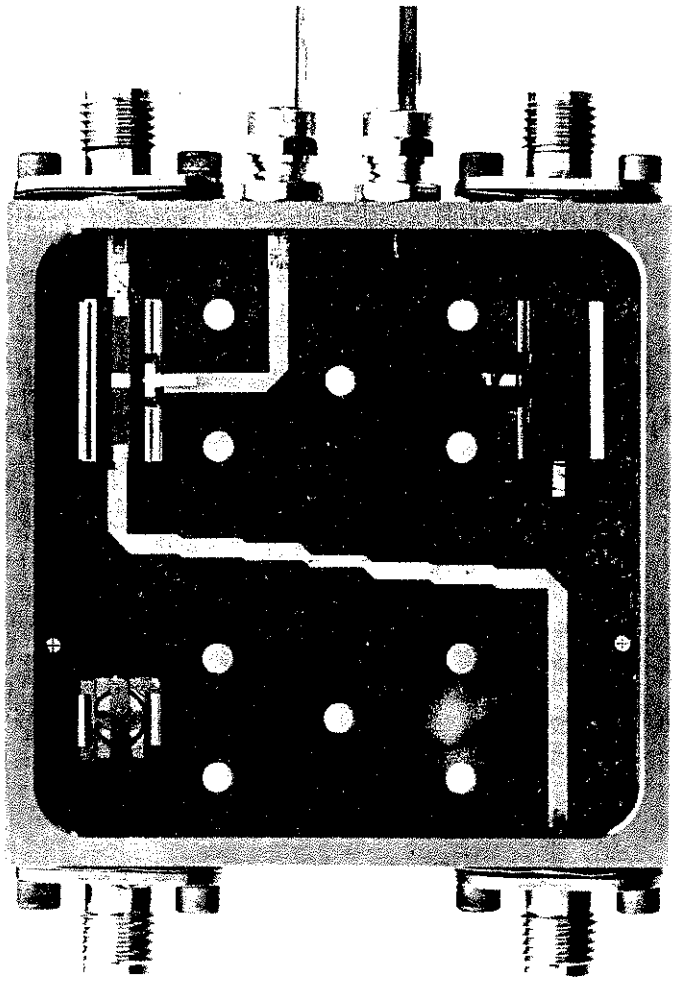


Fig. 2. This stripline directional coupler couples the 2-4 GHz first L.O. signal to both internal and external mixers. The coupler uses a suspended substrate completely surrounded by ground which greatly reduces rf losses. Visible in upper left corner is thin film circuit pictured in Figure 1.

p— excellent examples of the value
ghly integrated electrical and mechanical design.

The basic approach to the design of a high-performance broadband harmonic mixer is to minimize the unwanted parasitic inductances and capacitances associated with the mixer diode mounting system, and to provide as much rf energy as possible to the mixer diode. Achieving these two goals will result in optimum broadband flatness and conversion efficiency.

The 7L18's external mixers use a very small Schottky-barrier diode and tungsten "cat's-whisker" type probe mounted directly across the high-fields region of a ridged waveguide. Mixers of this type are not new. They were built twenty years ago using standard waveguide and older style silicon point-contact diodes. The use of a tungsten "cat's-whisker" probe dates back even
her, finding wide use in devices
ing World War II.

New technology in the fabrication of silicon wafers is the primary factor contributing to the high performance of the 7L18 waveguide mixers. An array of hundreds of 4.7 μm diameter Schottky-barrier diodes on a 0.010" X 0.010" silicon wafer was developed by Tektronix specifically for use in these mixers (figure 5). Newly-developed metallurgical processes are used to produce a diode which can survive in unpackaged environment and withstand the pressure of the tungsten probe. These extremely small diodes and the smaller still (0.001" diameter) probe provide minimal junction capacitance and probe inductance, thus eliminating in-band parasitic resonances and minimizing reflections. The tip of the tungsten probe is etched by an electrochemical process to produce a sharp but rounded tip. This is important in maintaining ohmic contact against oxidation of the tungsten, without damaging the metallization and destroying the diode.

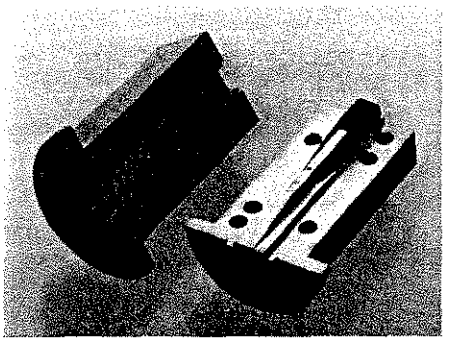


Fig. 4. An internal view of the 40-60.5 GHz mixer showing the ridged waveguide construction. The diode matrix is mounted on the small disc in the left portion and the tungsten "cat's whisker" protrudes through the small hole in the ridged portion. The black wedge is a carbon block termination.

In addition to the careful design of the special mixer diode assembly, refinements in the mixer housing further improve broadband flatness and conversion efficiency. Conversion loss is minimized by using ridged waveguide. This type of structure concentrates the rf energy in the gap between the top of the ridge and the adjacent waveguide wall, where the mixer diode assembly is located. Therefore, the diode can become saturated with rf energy at power levels as low as −30 dBm, but can easily withstand up to 10 mW without damage.

Further improvements in flatness are achieved by designing a standard-to-ridged waveguide broadband transition into the mixer body preceding the mixer diode, and a tapered waveguide load beyond the diode to terminate the rf line.

Summary

This has been just a brief glimpse into the microwave capability at Tektronix. The key element, of course, is people. Dedicated, innovative people not content with the current state-of-the-art. Supporting the innovators are craftsmen operating in many disciplines, and extensive research and manufacturing facilities to transform their "dreams" into realities. Realities in the form of instruments like the 7L18 that help you make microwave measurements with greater ease and convenience, and confidence in the accuracy of the end result.

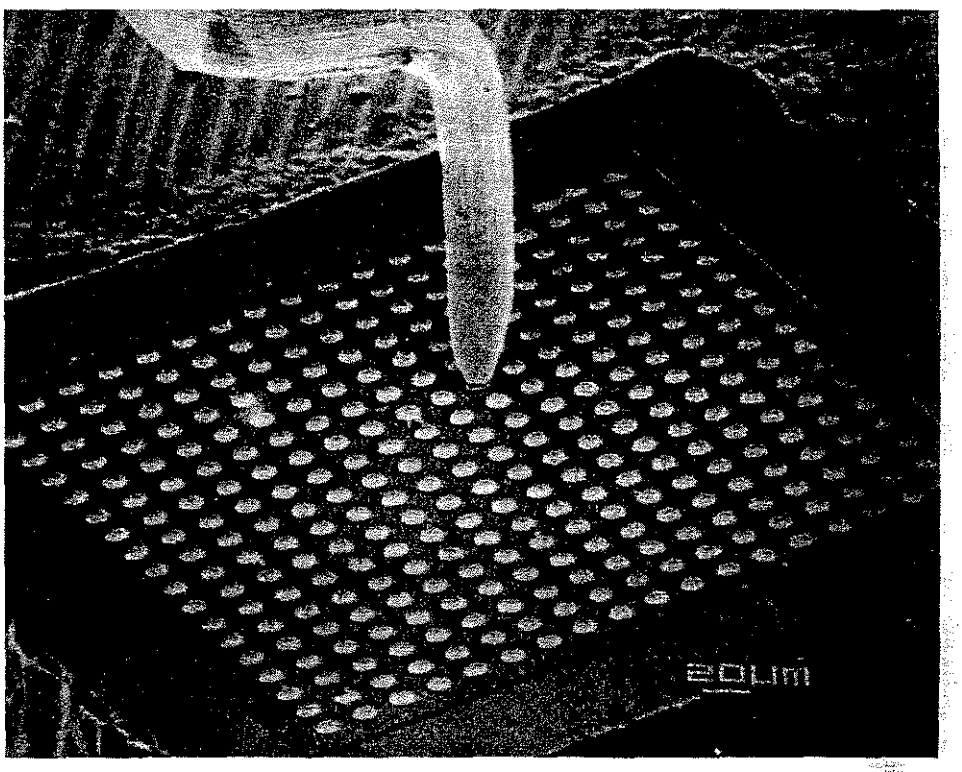
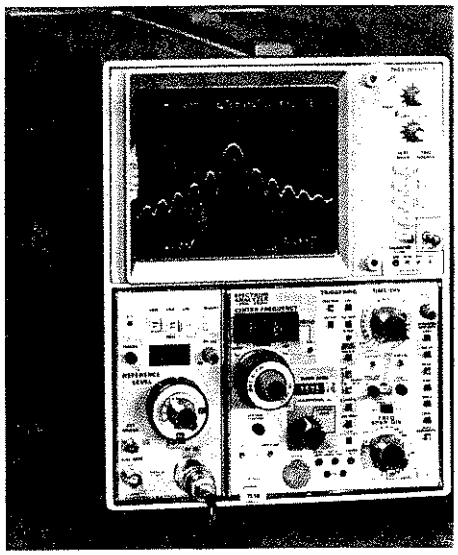


Fig. 5. External mixer diode consists of a silicon wafer containing an array of hundreds of 4.7μm Schottky-barrier diodes. Tungsten "cat's whisker" probe is 0.001 inch in diameter.

A High Performance Transportable Microwave Spectrum Analyzer



Precision microwave measurements typically are difficult and time consuming to make and usually limited to a laboratory setting. Now a new microwave spectrum analyzer, the 7L18, offers substantial improvement in the speed and convenience of making such measurements, and can be hand-carried to the site.

Covering the spectrum from 1.5 GHz to 60 GHz, the 7L18 extends the 7000-Series user's choice of high performance analyzers over the range of 20 Hz to 60 GHz. The 7L18 can be used with any 3- or 4-wide mainframe including the militarized USM-281C.

Several technological innovations contribute to the ease and accuracy with which measurements are made. Advanced YIG-tuned filter design gives spurious-free displays from 1.5 GHz to 18 GHz. External millimeter-wave harmonic mixers of improved design provide specified calibrated flatness from 18 GHz to 60 MHz. Advanced phase lock techniques yield a usable resolution capability of 30 Hz through X-band (12 GHz) and 300 Hz resolution to 60 GHz. Custom LSI signal processing chips provide split-memory storage, computation of average value, display of maximum signal level, and comparison of reference and incoming signal levels for rapid analysis of differences. We will discuss some of these innovations, with others covered in detail elsewhere in this issue.

Microprocessor based control system

One of the major design goals for the 7L18 was to achieve a quality we call "transparent." Transparent means the controls have been human engineered so the operator can use the instrument without conscious effort, and the instrument gives accurate, unambiguous results. This goal was realized by implementing a microprocessor-based control system.

The microprocessor has changed the basic concept of how test instruments are organized. Before, instruments were organized much like a spoked wheel, with the front panel being the wheel's hub. The spokes were the various assemblies directly controlled by front-panel knobs and switches. The rim of the wheel was the various assembly interconnection of both signals and interacting controls. Now, the microprocessor is the wheel's hub, the front panel is relegated to being one of the spokes, and only signals travel the rim of the wheel.

Before, instrument designers were forced to compromise many aspects of their design because of the difficulties of controlling a complicated system with a limited amount of logic. Now, this barrier has been removed. The designer is free to optimize his design, knowing that with a microprocessor he can devise a control system.

The span attenuator circuit in the 7L18 is an example of this process (see figure 1). Previous microwave analyzer designs required two, and sometimes three, attenuators: one for the span knob, and one for the band switch, to attenuate the sweep for harmonic conversions, all in cascade. Some phase lock techniques require another that is proportional to the first local oscillator frequency. This multitude of attenuators caused signal-to-noise degradation of the sweep signal but made it possible to control the oscillator sweep width with a series of user-operated switches.

Only one span attenuator is used in the 7L18. The microprocessor sets it to the proper value which is computed from the span per division knob setting, the band switch setting, and the local oscillator frequency (in the phase locked setting only). A complex algorithm chooses the attenuator setting and determines when to go into phase lock. The result is simplified design and improved signal-to-noise ratio.

Other functions performed by the microprocessor include: computation of center frequency from a digital voltmeter reading that is proportional to the oscillator frequency and band switch setting; reading the IF gain switch, RF attenuator, and band switch settings and computing the proper IF control settings and the reference level; reading the time per division, span per division, and resolution bandwidth settings and performing the appropriate control functions when automatic time and resolution bandwidth functions are selected; and sending information to the crt readout for Center Frequency, Reference Level, Resolution Bandwidth, and Span per Division.

The microprocessor used in the 7L18 is the Intel 4004, a 4-bit processor well suited to this use. The control bus consists of four address lines, four data lines, a data input strobe line, and a data output strobe line. This bus is carried throughout the 7L18, touching on most of the major circuit board assemblies.

To get an overall picture of how the 7L18 functions let's consider the simplified block diagram

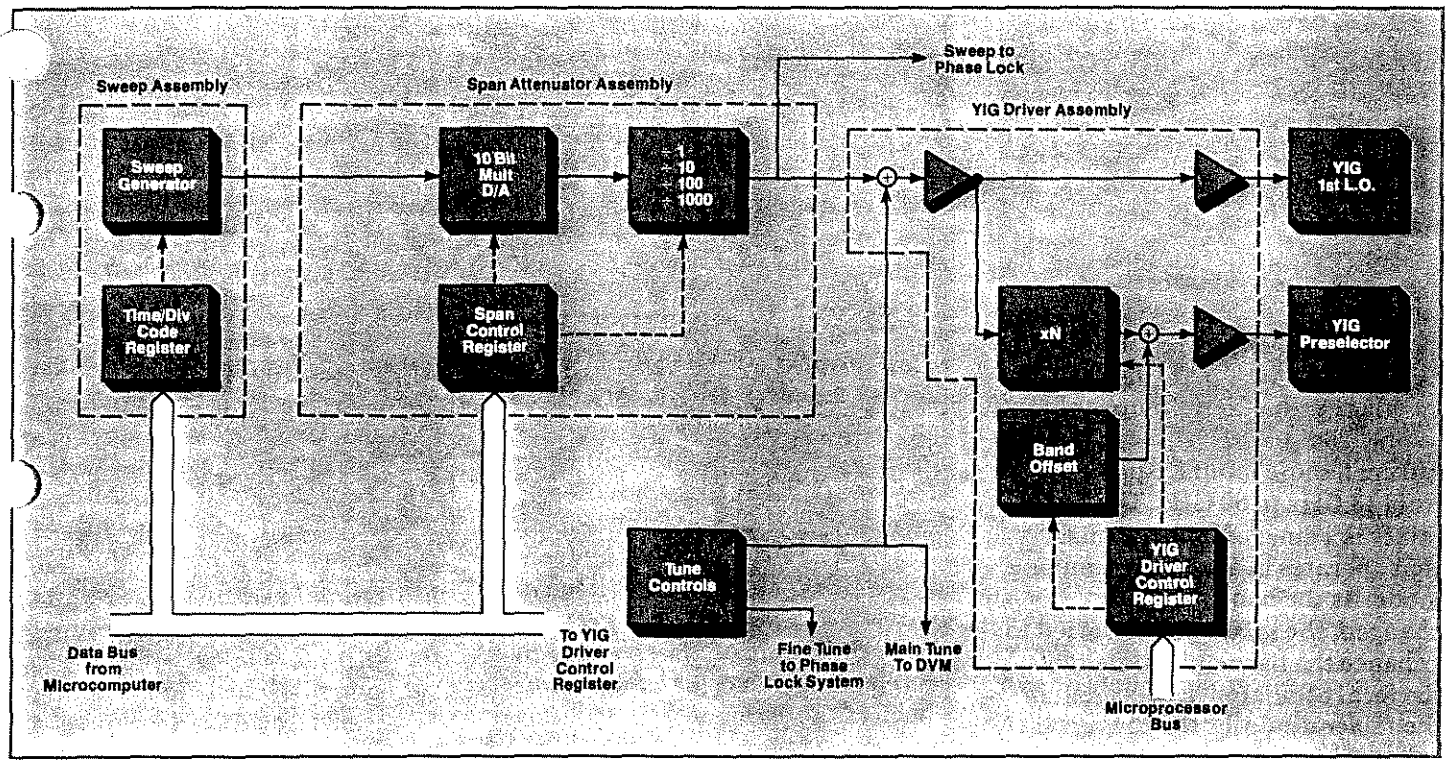
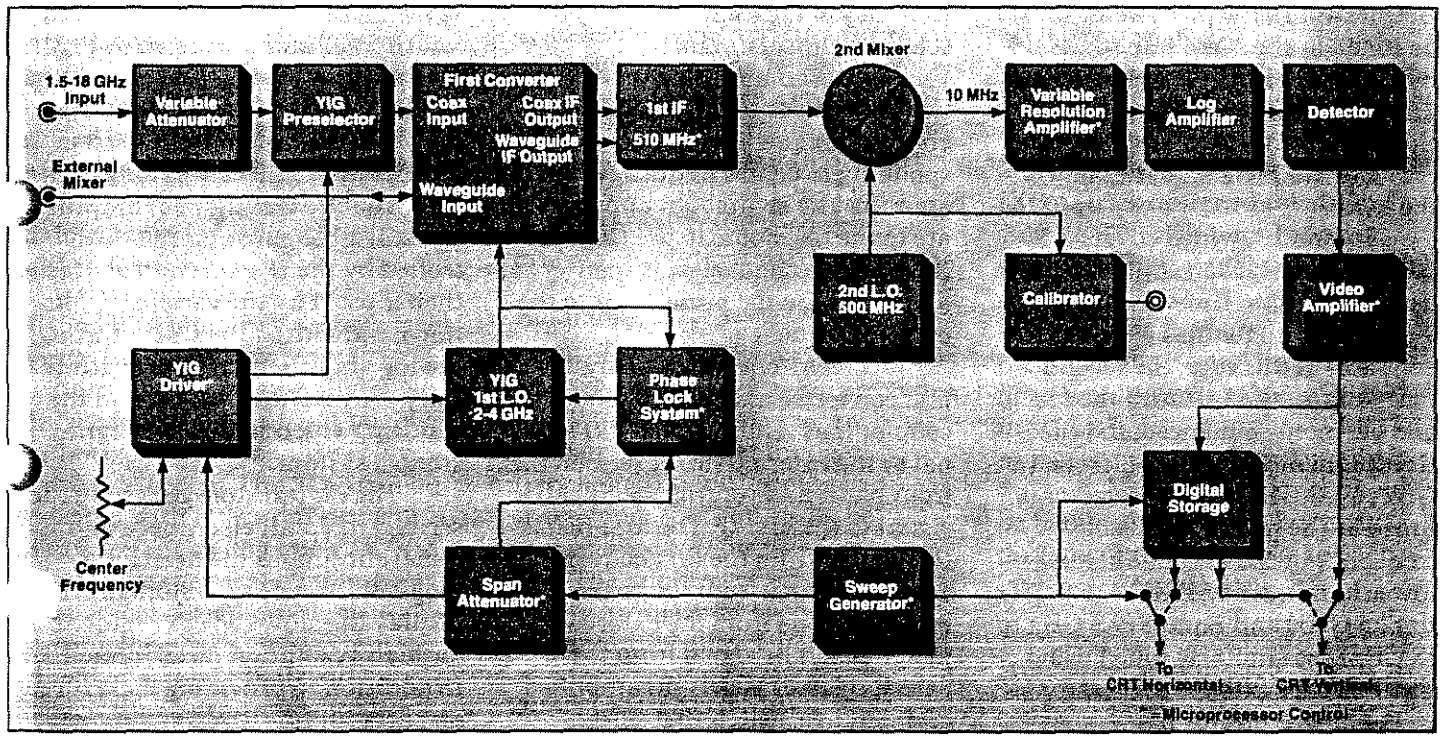


Fig. 1. Special attention was given to minimizing the number of connections between assemblies as evidenced in the block diagram of the 7L18 span control system.

Fig. 2. Simplified block diagram of the 7L18. Note the elements that are affected by microprocessor control.



shown in figure 2. A signal entering through the coaxial input filter first passes through the RF attenuator and is then sent to the YIG-tuned preselector. The 3-sphere YIG filter (described elsewhere in this issue) provides a voltage-tuneable band-pass filter that selects which signal is to be applied to the first converter.

The first converter assembly contains the first mixer and a coupler for the external mixer input on the front panel. (Three external mixers handle input frequencies from 18 GHz to 60 GHz. The first mixer is a singly-balanced mixer that operates in a harmonic mixing mode. As the band switch is changed, the mixer bias is varied to enhance the harmonic content of the local oscillator (LO) current in the mixer diode for the conversion in use. This optimizes mixer performance for each band.

The first LO operates in a frequency band of 2.0 to 4.0 GHz. The first IF frequency is 510 MHz. To pass a signal from the input to the first IF, the preselector must be tuned to an appropriate frequency with respect to the first LO. For instance, if it is desired to pass a signal in the range of 1.5 GHz to 3.5 GHz (Band 1), the preselector must be tuned at the same rate as the LO but 510 MHz lower. Band 2 covers 2.5 GHz to 4.5 GHz. On this band the preselector tunes at the same rate and 510 MHz higher than the LO.

In Band 3, which covers 3.5 GHz to 7.5 GHz, harmonic mixing is used for the first time. As noted previously, the mixer bias is varied to enhance, in this case, the second harmonic of the LO. With the second harmonic enhanced, the effective frequency of the LO is from 4.0 GHz to 8.0 GHz. The preselector is tuned at the rate of the effective frequency of the LO but 510 MHz lower in frequency. Band 4 (6.5 GHz to 12.5 GHz) and Band 5 (9.5 GHz to 18 GHz) are similarly tuned using the third and fifth harmonics.

The preselector has a bandwidth of about 50 MHz but

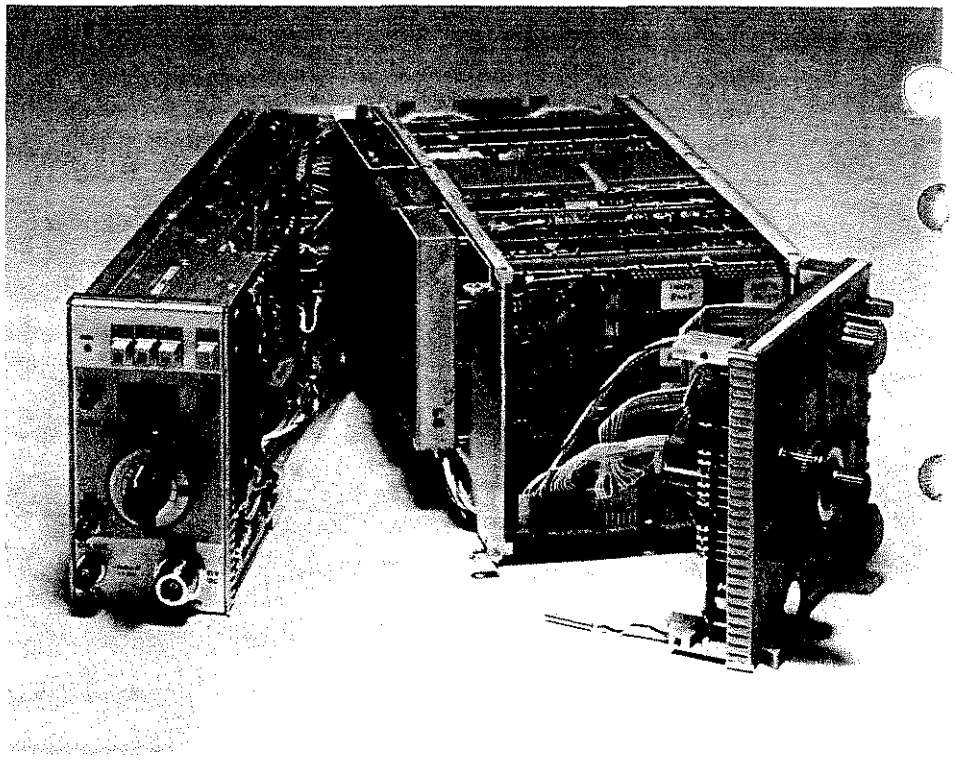


Fig. 3. The vertical section and front panel module are hinged for easy access to circuitry. An extender extrusion gives access to individual circuit boards. The 7L18 can be operated outside the mainframe in this configuration by means of a flexible extender cable.

significant unflatness will result unless the preselector is tuned to within about 2 MHz of the correct frequency. Special attention was given to temperature and drift compensation to maintain the accuracy of the oscillator and preselector control circuitry.

The oscillator tune voltage, which includes both the sweeping component and an offset corresponding to center frequency, is amplified by an amount appropriate to the harmonic in use (X1, X2, X3, X5). A second offset is then added to tune the preselector to the correct frequency.

As mentioned previously, the first converter assembly includes a coupler that sends the first LO signal to the external mixer jack on the front panel and returns the 510 MHz signal to the first IF. The first IF has two inputs from the first converter assembly—one from the coaxial mixer and one from the external mixer jack. The signal from the external mixer jack is preamplified and sent to a switch that selects between this signal and the coaxial mixer input signal. The amplifier following the switch is variable gain to compensate for the wide range of conversion losses caused by the use of harmonic mixing.

The amplified 510 MHz signal is then filtered with a 3 MHz band width filter and converted to 10 MHz by the second mixer and the second LO at 500 MHz. The second LO is amplitude regulated and the harmonics used as a calibrator signal.

The 10 MHz signal is amplified by a variable gain amplifier controlled by the IF gain control. It is then filtered by the various resolution bandwidth filters, sent through the log amplifiers to be logarithmically converted, detected, and the resulting video sent to the digital storage system.

The digital storage system (described in detail else-where in this issue) eliminates the need for a long-persistence type storage crt to display the slow sweeps required for high-resolution measurements. In addition to providing flicker-free displays, the digitized video signal is processed further to provide sev-

eral computed signal parameters ch as average value—ideal for iminating the effects of noise, comparison of a reference signal and an incoming signal and display of only the differences between the o, and the display of maximum incoming signal level over an extended period of time.

Mechanical design

In microwave design, mechanical innovation is often as significant as circuit innovation. This is particularly true in the 7L18 where the al was to package the electronics r a state-of-the-art microwave spectrum analyzer in a 3-wide 7000-Series Plug-In. Easy access to internal modules to facilitate adjustments, maintenance, and occasional repair was a must—all to be accomplished without compromising RF performance.

After extensive consultation with the electrical design team, precise space allocations were greed upon for each of the circuit nctions. The bulk of the circuitry resides on 4" by 5" printed circuit boards fitted into U-shaped extrusions. These extrusions interlock with extrusions on either side of the unit providing mechanical stability and a means of shielding between adjacent modules. Any module can be removed without disturbing the structural or functional integrity of the other modules. An extender extrusion is available to give access to individual circuit boards while the 18 is operating outside of the mainframe using a flexible extender cable.

Further access is accomplished by a hinge between vertical (signal input) and horizontal sections, and the front-panel module (see figure 3). The front panel of e horizontal section also is hinged provide access. The 7L18 can be operated with either or both of these sections swung open.

One of the most challenging echanical design problems was housing the phase-lock system which gives the 7L18 its outstanding stability. Several assemblies had to be well isolated to ensure spurious free response, yet located in close proximity.

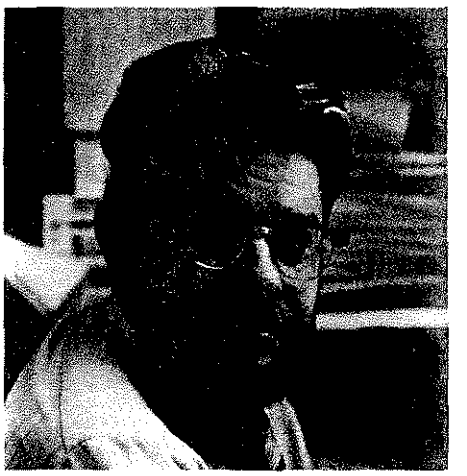
The needed isolation was achieved by housing the critical phase-lock circuitry in an aluminum milling. The milling utilizes solid bottom wells into which the individual circuit boards are mounted. Compartment to compartment interconnections are made by jumpers that pass through slots cut in the top of the side wall. To enhance the isolation further, each circuit board has an individual cover that fits under the outer cover.

To reduce incidental hum modulation by stray line related magnetic fields, the master sweeping oscillator is shielded in two layers of magnetic shielding. The resonator itself is shielded in a small mu-metal enclosure and the entire oscillator circuit is shielded within another mu-metal can. This reduces hum modulation to a very low level.

Numerous other mechanical design innovations in the 7L18 include direct input to the front-end attenuator; a 40:1, two-position, center-frequency control with a proprietary detent system that locks it firmly into the selected position; and a compact front-panel readout drum that indicates both the selected band and its associated harmonic. Precision bending of semi-rigid coax to eliminate reflection and minimize transmission losses was achieved with special tooling that controls bend curvature within 0.5° and assures accurate plane relationships.

Summary

State-of-the-art performance and state-of-the-art packaging are combined in the 7L18 to give you new measurement capability and unparalled operating ease in an instrument that can easily be transported to your measurement site. The addition of this microwave spectrum analyzer to the 7000-Series family allows you to make measurements over the spectrum of 20 Hz to 60 GHz with a high degree of confidence in the results.



nley Gumm is Project Leader for the 7L18 rogram. He designed trigger circuits for e 454, 7B50/51 and 7B70/71 time bases efore joining the spectrum analyzer group. e has a B.S.E.E. '64 from Washington ate and M.S.E.E. '70 from the Univ. of ashington.

Acknowledgements

As Project Manager for the 7L18 I would like to express my thanks to those who contributed so much to the success of the project. Bob Bales worked on the sweep, span attenuator, YIG driver, and instrument-interconnect; Russell Brown and George Maney did the microprocessor programming; Carlos Beeck and James Wolf mechanical design of the microwave assemblies, with Dave Shores and Philip Snow providing the electrical design; IF design was done by Wesley Hayward; Jack Reynolds was involved in the early design of the phase lock circuitry with Steve Morton completing the work; Don Kirkpatrick designed the digital storage IC's with Dennis Smith doing the front panel and digital storage board; Al Huegli was responsible for the outstanding job of mechanical design. Virginia Morehead was indispensable in providing prototype support, as were the plant support people during introduction. Many other names should be included in this list but space doesn't allow. My thanks to each of you for a job well done.

The 7L18 will be introduced outside the United States during the first quarter of 1978. For further information, please contact the nearest Tektronix Field Office, Distributor, or Representative.

Digital Storage For A Microwave Spectrum Analyzer

Dennis Smith, at left, did the readout board design for the 7L18 and assisted with the storage board and front-panel design. He has his B.S.E.E. '74 and M.S.E.E. '75 from Montana State. Don Kirkpatrick, at right, designed the storage circuitry for the 7L5, reducing most of it to two ICs for the 7L18. Before joining the spectrum analyzer group he worked on the 4012 and 4014 Graphic Display Terminals. He has his B.S.E.E. '69 and M.S.E.E. '75 from Oregon State.

Digital storage is a relatively recent innovation in spectrum analyzers and is usually found only in those covering the frequency spectrum below 100 MHz. Why, then, digital storage in a microwave spectrum analyzer?

The excellent stability made possible by state-of-the-art circuits and components permits resolution measurements of 30 Hz at frequencies up to 12 GHz and 300 Hz up to 60 GHz. To scan through and fully display a 10 kHz spectrum at 30 Hz resolution requires scanning at more than 20 seconds per sweep. The usefulness of storage at these sweep speeds is obvious—it lets you view such slow moving displays flicker free. A storage crt could accomplish much the same thing. But, in addition to simplified operation, digital storage offers other advantages; for example, signal averaging to reduce the effects of noise, capturing the peak level of a signal, displaying drift in a signal, and comparing an incoming signal to a previously stored reference signal.

In this article we will discuss some of the problems, and solutions, involved in developing a digital storage system for the TEKTRONIX 7L18 Microwave Spectrum Analyzer.

The average calculation

The first problem considered was the necessity of performing an averaging function for smoothing of the waveform. This is usually done in an analog manner using a low pass filter called a video filter. The major problem encountered in smoothing digitally is the wide range of sweep speeds over which the 7L18 operates (20 sec/div to 1 ms/div). This is a large dynamic range over which to do digital averaging.

The solution to this problem involved finding a practical method of performing division rapidly. After considerable research, we adapted a technique employed in an early hand-operated mechanical calculator—that of using a series of subtract and shifts to effect division. The numerator and denominator are justified left and subtractions are performed until the denominator is larger than the numerator. The denominator is then shifted one place to the right and subtraction continued until the division is completed. Using this technique allows us to perform a division of a 17-bit denominator into a 25-bit numerator and arrive at an 8-bit quotient in 18 microseconds—a speed adequate for our needs.

The technique was first implemented in the TEKTRONIX 7L5 Spectrum Analyzer. The circuitry occupied two printed circuit boards totalling about 60 square inches, used 60 integrated circuits, and consumed a moderately large amount of power. When the 7L18 was conceived, it was evident we would not have nearly the same space and power available so we set about making the necessary reductions.

Nearly all of the digital circuitry was put into two custom LSI circuits—one for the horizontal function, the other for the vertical. These two ICs, along with external D/A converters, operational amplifiers, switches and switch debounce circuitry, and connectors are contained on a circuit board of less than 20 square inches (see figure 2).

The two chips are tied together into one coherent unit by a major synchronizing pulse which occurs every 9 μs. Data is stored serially in the 8k X 1 random access memory. This simplifies some of the other chores to be performed and provides some unique operating features. For example, you may want to read out the memory contents into an external device. This is accomplished through the use of an external "handshake". When a BUS REQUEST signal is received, the address bus on the memory goes tristate once every 40 microseconds and gives an external device access to the memory for one 9 μs cycle. The external device must provide the addresses and whether the in-

formation is to be read or written. The entire memory contents can be read out in about two milliseconds.

Memory with a difference

The digital storage memory in the 7L18 is functionally (but not physically) divided into two sections—A and B. Several modes of operation are available to you. You can store data in A or B, or in both. There are 512 A values and 512 B values. When both are displayed, the origin of B is shifted such that the A and B coordinates are interlaced giving you a display of about 1024 increments.

When the SAVE A function is activated the data in A memory is held, and only that in B memory is updated. In this mode, all of A is drawn and all of B is drawn, each in a separate trace.

A third display mode is available, called B-SAVE A. (B minus SAVE A). In this mode the displayed values are the differences between the B and A values for the same X coordinate. This is a very convenient mode to use in aligning filters and other devices where you can tune for a null. However, an interesting problem arises if the device you are testing is active. The reference waveform is stored in A memory and the unknown is stored in B memory. If the device is active, the B waveform may be larger than A resulting in a shift in the zero reference line. Then, for a particular application, where should the reference line be positioned—center-screen, at the top, or at the bottom? (It is set near top-screen at the factory.) We resolved this problem by allowing you to select the position of zero reference through the choice of a digital word. We created the mathematical expression B-A+K, with the value of K set by the selected digital word, which you can program.

Now let's take a closer look at the two LSI chips developed for the digital storage system. As we pointed out earlier, the storage display system is partitioned into two sections—the Vertical Control Circuit and the Horizontal Control Circuit. The vertical chip contains circuits for vertical acquisition, vertical display, peak detection, signal averaging, Z-axis blanking, and special Y-value processing. The horizontal chip contains the horizontal acquisition address counter, horizontal display counter, ten-bit RAM address multiplexer and a program logic array system control matrix. External to the two chips are two 8-bit digital-to-analog converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8k bits of random access memory, and all required analog functions.

The vertical control circuit

A simplified block diagram of the vertical chip is shown in figure 3. The vertical analog voltage is converted to a Y-value binary number using an 8-bit successive approximation register. Eight clock cycles are required to perform the analog to digital conversion. For one clock period between each conversion the successive approximation register produces a low-going pulse called $\overline{\text{SYNC}}$. This is the synchronizing pulse mentioned earlier that ties the two chips together into one coherent unit. Nearly all functions of both chips are related to this pulse.

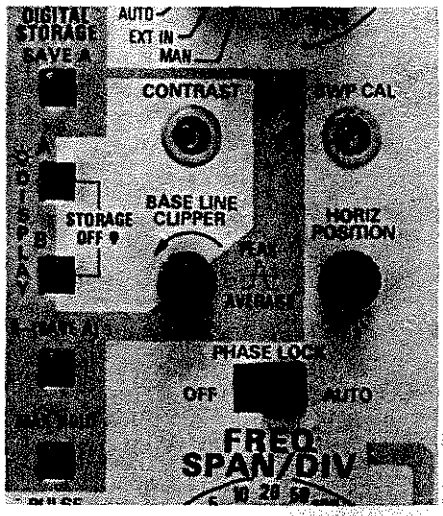
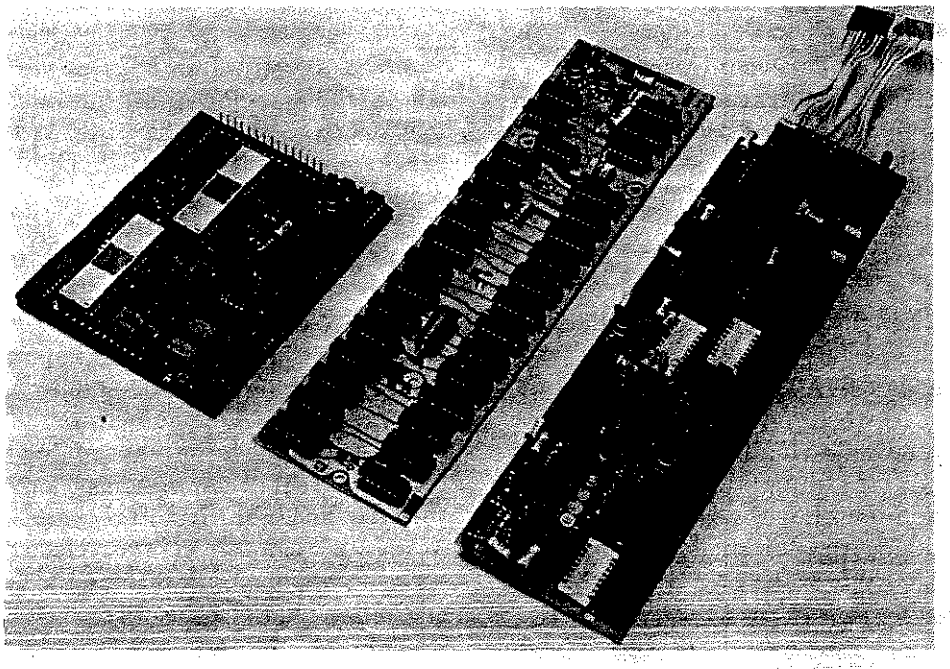


Fig. 1. Front-panel storage controls permit you to store one or two traces, or display the difference between the two.

The averaging circuit has three distinct parts: the grand total of all the Y values (for a given X coordinate), called the numerator; the number of samples comprising the numerator, called the denominator; and the subtract and shift circuit which performs the division. As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is simply counted by a 17-stage ripple

Fig. 2. The digital storage circuitry in the 7L5 occupies the two boards at right. The same function is performed in the 7L18 by the single board at left.



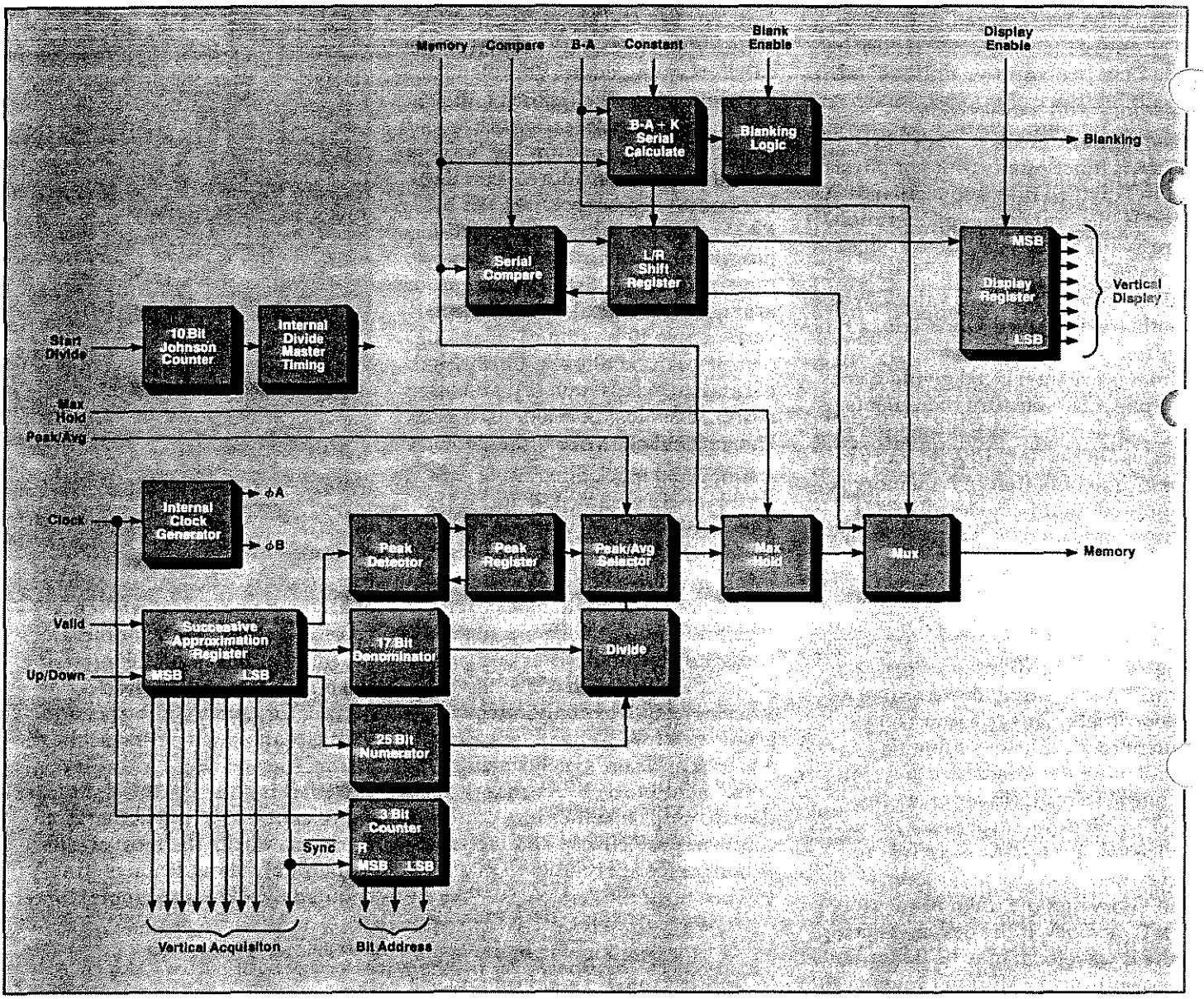


Fig. 3. Simplified block diagrams of the integrated circuit containing the vertical portion of the storage circuitry.

counter. This counter and the eight-bit sum are cascaded to form the 25-bit grand total. Each time a new sample is added to the numerator, a second 17-bit ripple counter is incremented, generating the 17-bit denominator.

A division cycle is started when the horizontal chip detects a change in the X coordinate. It sends a logic START DIVIDE signal to the vertical chip. Ten clock periods are required to load the divide circuit with the numerator and the denominator, with the actual divide taking an additional eight periods. The cycle starts on a $\overline{\text{SYNC}}$ pulse and the first bit of the quotient is available shortly after the positive edge of the first clock pulse following the next $\overline{\text{SYNC}}$. As we discussed previously, division is performed by repeated subtract and shift. The quotient is created serially with the most significant bit first. Since only eight-bit accuracy is required, the divide circuit is loaded with the eight most significant bits of the denominator and the sixteen most significant bits of the numerator.

The peak Y value reached during the last set of samples has been stored in an eight-bit shift register. At the start of a conversion cycle, a serial compare circuit is set to the state "don't know if the old or new number is larger". Each bit of the new and old value is then compared, most significant bit first, and when one number is found to be larger, a flip-flop is set and the larger number is stored in the shift register. A multiplexer circuit selects either the peak or average value to be routed to the memory, based on the setting of the front panel PEAK/AVERAGE control.

One of the special features of the 7L18 is MAX Hold. When this function is selected (by pressing a front-panel pushbutton), the larger of two values—the current memory value at this X coordinate, or the previously selected peak/average

value—is stored in memory. Because the memory cannot read and write simultaneously, the current memory value was read at the same time the divide circuit was being prepared, and was temporarily stored in the vertical display serial-to-parallel shift register. The circuit which selects the larger of peak/average or memory value is functionally identical to the peak detector.

Timing for setting up the divide and clearing the numerator, denominator, and peak circuit is controlled by a ten-stage Johnson counter. Nor gate taps are taken from appropriate stages to develop the necessary clear and latch timing pulses.

As we discussed earlier, all data enters and leaves the memory serially. Data read from the memory enters an eight-bit shift register and, timed by $\overline{\text{SYNC}}$, is transferred to the vertical display latch. This shift register is used for other purposes, so the DISPLAY ENABLE signal allows only display information to be transferred to the display latch. One example of data moving through this shift register is during a B-A display. The A value is first read from memory and stored in the shift register. As the B value is read, the subtraction is done serially and the answer is fed to the shift register. The subtraction must be performed least significant bit first so a set of exclusive OR gates change the order of extracting B from memory. The direction of shift for the shift register is reversed also to present the most significant bit to the proper display latch. The answer is transferred from the shift register to the display latch by the DISPLAY ENABLE signal.

The subtract network does more than just B-A. The actual expression is B-A+K where K is a serial input external constant specified by the user. This permits you to place zero reference at any point on the display. To avoid possible confusion, when B-A+K is off-screen the subtractor blanks the display.

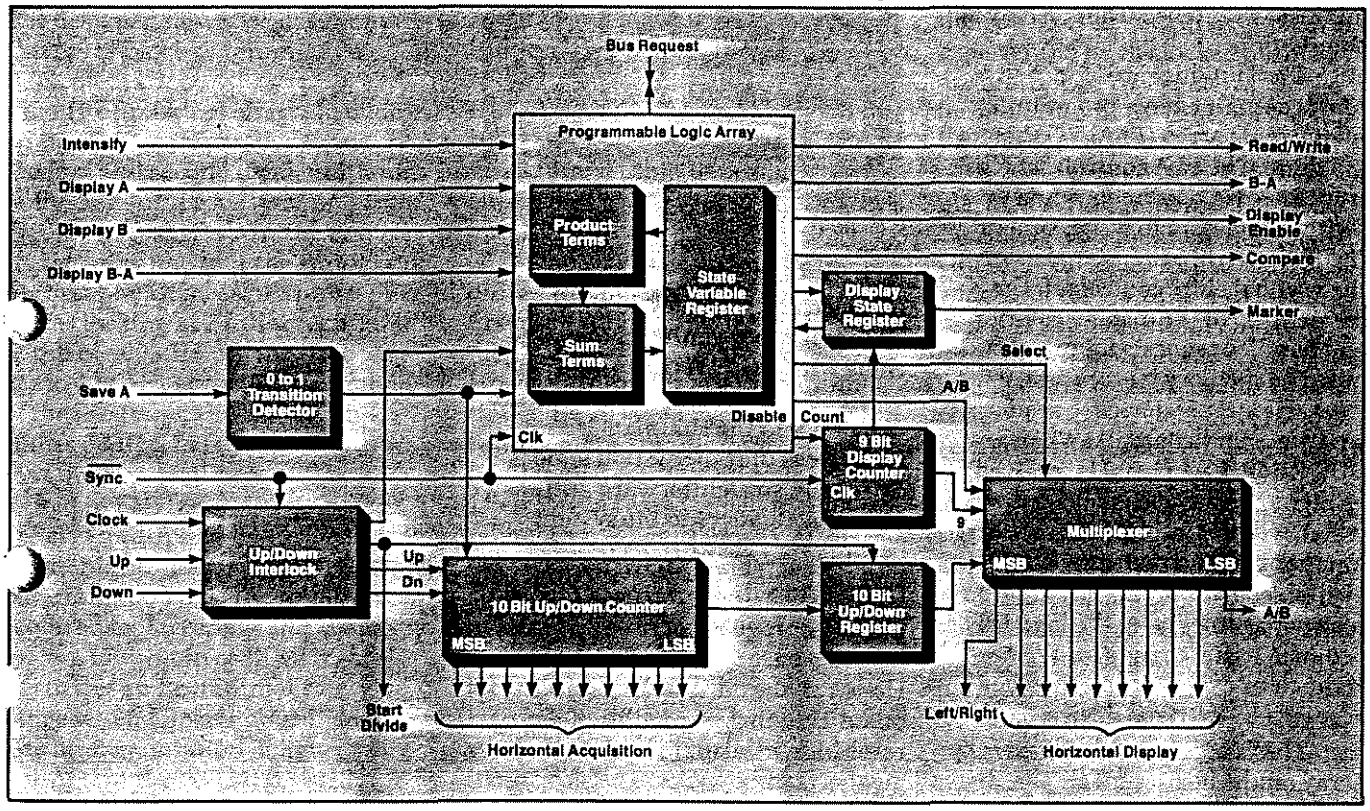
When SAVE A is disabled and both A and B are being displayed, maximum resolution of 1024 elements is displayed. If this display shows a very narrow pulse on the screen, it is possible that the top of the pulse is a single X coordinate wide. If this maximum value were in B memory, and SAVE A turned on then display B turned off, there would be an apparent drop in amplitude on the screen. For this reason, when SAVE A is turned on, a special circuit on the vertical chip compares all A and B values with the same X coordinate and stores the larger in the A memory.

The vertical chip also contains a three-bit synchronous counter which identifies which bit of the eight-bit vertical value is to be read or written by the memory. This is the only memory addressing done by the vertical chip; all other addressing is under the control of the horizontal chip.

The horizontal chip

The horizontal chip is considerably

Fig. 4. Block diagram of the integrated circuit containing the horizontal portion of the storage circuitry.



less complex than the vertical chip. A simplified block diagram is shown in figure 4.

The X analog voltage is converted to a horizontal address for memory by the use of a ten-bit tracking analog-to-digital converter. As the sweep moves to the right, the counter increments. As the sweep retraces, the counter decrements. Each time the counter is incremented, there is a new X coordinate, and a START DIVIDE is generated to start the storage cycle. When the counter decrements, no START DIVIDE is generated. The increment clock is $\overline{\text{SYNC}}$ and the decrement clock is the basic 1 MHz system clock. When SAVE A is activated, the counter skips every other binary number, thus only B coordinates appear as addresses.

The stored waveforms are recreated by reading from memory the Y value and converting this value and its X location to analog voltages. The counter which cycles through all the X locations is located on the horizontal chip. By the use of a multiplexer, the memory address is switched from display to acquisition.

The "intelligence" for the system is contained in a programmable logic array (PLA) ROM-state machine. The PLA controls which trace is going on-screen, when to switch from read to write, generates the B-A coordination signals with the vertical chip, controls the incrementing of the display counter, and handles requests for memory bus. The memory bus request allows an external device to read or write memory contents. When a BUS REQUEST signal is received, an eight-clock cycle is selected which will not interfere with other functions. When that time becomes available, all address lines and the read/write lines go to the high impedance tristate mode for the next eight clock cycles. It can then be accessed by external devices.

The Programmable Logic Array on the horizontal chip is modeled after the classic Huffman/Moore finite state machine with the PLA performing the combinational logic. The advantage to a PLA and the Huffman-Moore machine is that the system logic is extremely straightforward and easy to follow. Changes to the system become very easy to effect.

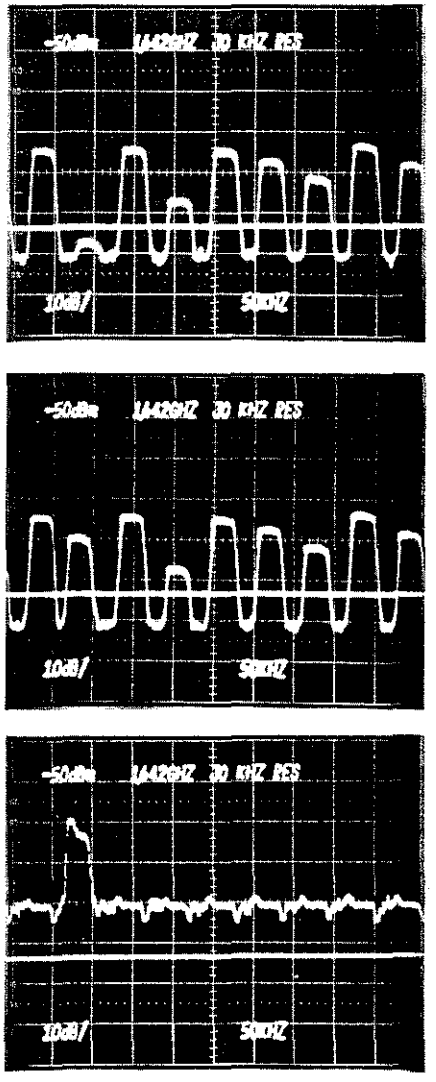


Fig. 5. This series of photos shows (top) display in SAVE A mode, (center) display in B mode, (bottom) display in B-SAVE A mode.

Conclusion

Digital storage is not usually found in microwave spectrum analyzers. However, the outstanding stability of the 7L18 makes possible 30 Hz resolution measurements at gigahertz frequencies. The slow sweeps necessary for such measurements make storage a valuable adjunct.

The power and space available for the storage circuitry in the 7L18 provided an engineering challenge that was successfully met, with new time-saving operating features added as a bonus.

A Phase Lock Stabilization System For 30 Hz Resolution At 12 Ghz

The first question when engineering was confronted with the 7L18 Spectrum Analyzer stability requirements was "is it possible?" Today we can easily say "yes". For a while, though, we were not at all certain that the 7L18 stability goals were attainable. Consider the fact that 30 Hz resolution at 12 Ghz is a ratio of 10^8. Consider further that this had to be attained in a sweeping system, with over 80 dB of display dynamic range, without introducing spurious responses. The implications of such specifications can be quite frightening. What follows is a discussion of some of these implications and the implemented solutions.

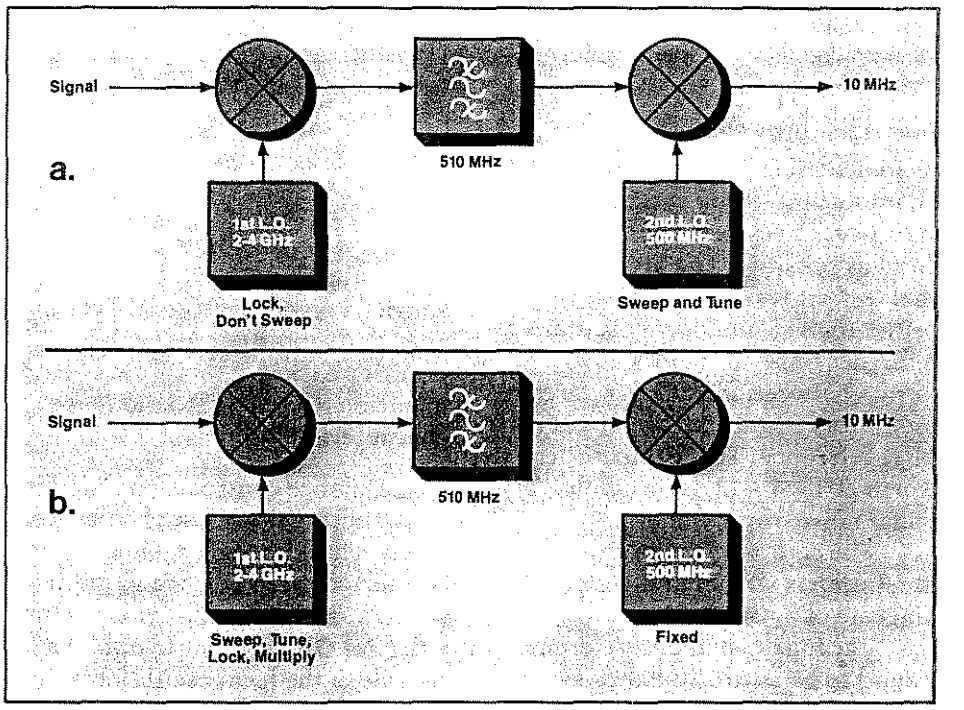


Fig. 1. (a) During phase lock operation, the First L.O. is locked and the Second L.O. is swept and tuned. In Fig. 1(b), the First L.O. is swept, tuned, phase locked, and multiplied, while the Second L.O. is fixed.

A balance of compromises

All frequency stabilization phase lock systems comprise certain basic elements such as a sampler, reference oscillator, error amplifier, etc. The designer, however, has many choices of block diagram implementation.

The first block diagram choice on the 7L18 was whether to sweep the first and second local oscillators or the first local oscillator only. Figures 1A and 1B show the two choices. Assume that the stability of the first (2-4 GHz) oscillator requires locking at a full screen span width of 500 kHz. By the time we get to 40 GHz, at the 10th harmonic of the oscillator, the 500 kHz becomes 5 MHz. Let us assume also that the first oscillator will be locked in 1 MHz steps. These steps are also multiplied by the operating harmonic number, assumed ten for our example. Thus, the total range required for sweeping and centering is a minimum of 15 MHz. Adding to this some minimal safety range we end up at about 17 MHz. The implementation of figure 1A requires that the 500 MHz oscillator sweep 17 MHz.

This system has the advantage that stability is virtually independent of operating harmonic number so that the same specifications apply at all input frequencies, and it avoids such complicating features as a conversion harmonic attenuator. The difficulty is that 17 MHz is a very large percentage of 500 MHz resulting in a loss in stability. Furthermore, this requires a nearly-impossible-to-design sharp cutoff, flat, 17 MHz-wide filter in the first IF.

One way of reducing the required tuning range is to lock the first oscillator in smaller increments, for instance 500 kHz. However the reference noise is multiplied by 20 log M, where M is the ratio of locked oscillator frequency to reference oscillator frequency. Therefore, a two to one reduction in reference frequency means a 6 dB degradation in sideband phase noise; not a very attractive prospect.

Another technique of reducing second local oscillator tuning range is to lock the first oscillator in small synthesizer tuning increments. But room and power constraints prohibited this.

The compromises implicit in figure 1B are different. Basic sweep width requirements are not multiplied at higher operating harmonics since this happens automatically in the mixing process. But other difficulties creep in. All instabilities experienced by the locked oscillator are multiplied by the conversion harmonic number. Thus, incidental fm is dependent on frequency with a ten times degradation, for example, at 40 GHz compared to 4 GHz. The input reference and sweep oscillator are used to lock a relatively wideband oscillator (2-4 GHz) as opposed to an essentially fixed frequency 500 MHz oscillator. As we tune the first local oscillator to change input frequency, the ratio of reference and locked oscillator frequency changes. This means that the ratio of any movement or sweeping of the reference oscillator also changes. To maintain a constant relationship it is necessary to normalize the reference sweep voltage through a conversion harmonic attenuator.

Clearly the implementation of figure 1B is much more complicated. But, barring the use of a reference synthesizer, it also gives

better stability for the lower conversion bands. It is the technique, chosen for the 7L18.

Adding improvements

As indicated in the previous section, an important key in getting good stability is to sweep as narrow a band as possible. The first choice in this respect was to sweep the first rather than second local oscillator. A further improvement was to switch between four fixed reference oscillators to get 1 MHz steps at a 4 MHz reference. This is theoretically worth 20 log4 =12 dB in sideband phase noise improvement.

The complete basic implementation is shown in the block diagram of figure 2.

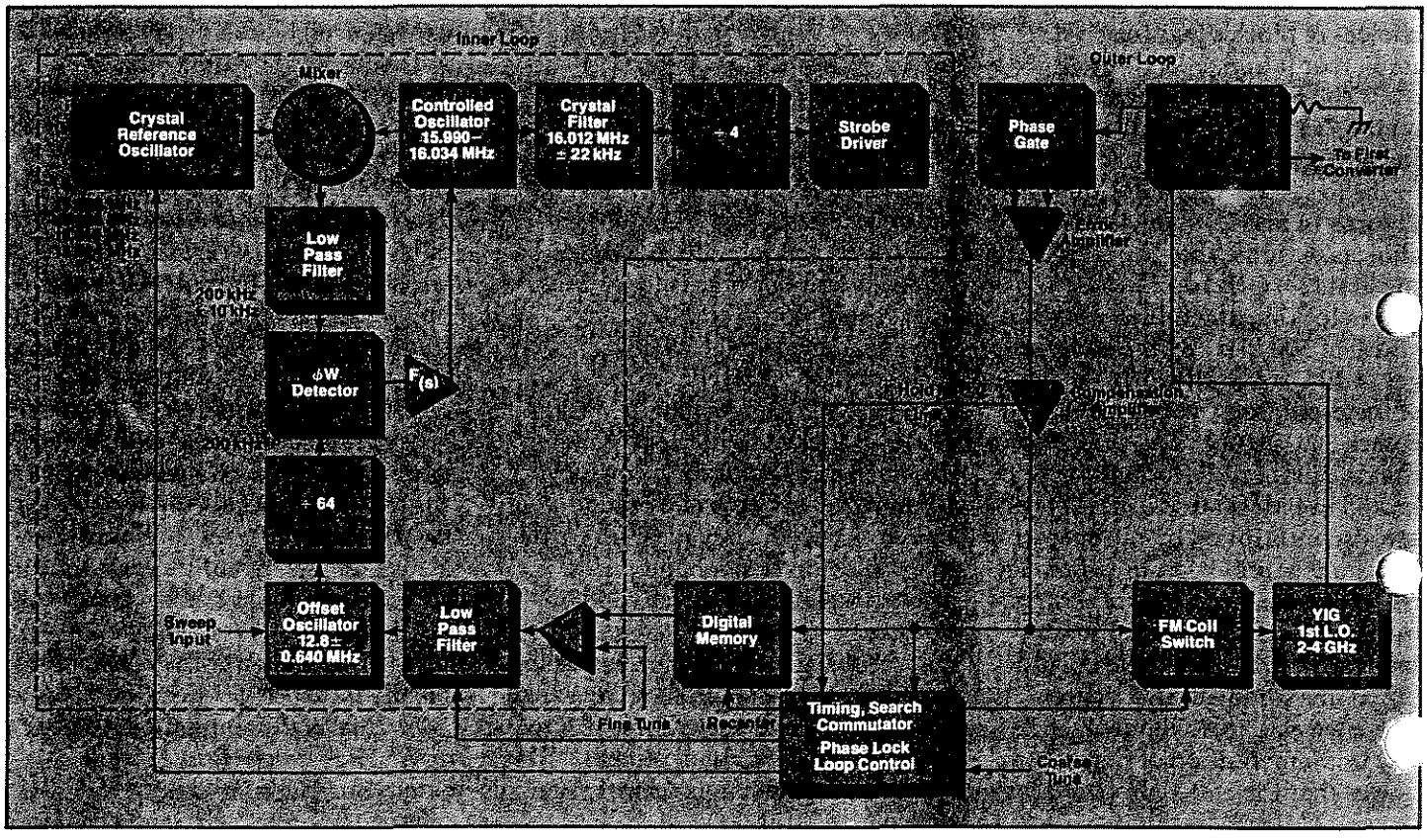
The four megahertz reference is used to generate 20-nanosecond wide, 4-volt strobe pulses which are further sharpened up to a 100 picosecond or less risetime in a snap diode circuit. This drives a sampling phase gate to generate the phase lock error signal. Phase gate characteristics are important in transferring the full cleanliness of the reference signal to the local oscillator. Precise balance between coupler arms, sampling diodes, and strobe pulse amplitude level has to be maintained to prevent reference strobe harmonics from getting into the local oscillator, thus creating spurious responses. Control of balance and amplitude level also permit phase lock loop gain optimization for best sideband noise characteristics.

Balance control is obtained by constructing the phase gate, as well as associated circuitry, on an interconnected array of three alumina substrates. These substrates include a flat 2-4 GHz coupler to obtain a sample of the local oscillator, a resistive power divider to separate the local oscillator input into two channels, two terminated sampling diode chips, a combiner and integrator to drive the error amplifier, a balanced snap diode driver with snap diode, and two couplers for coupling the snap diode generated strobe pulses into the sampling diode lines.

Defining stability

With all this fuss about getting things stable it might be useful to explain what it is that we are after. Figure 4 shows an illustration of the three elements which are affected by phase lock stabilization.
Drift—a gradual shift in center frequency with time, temperature, line voltage, etc. is a relatively slow phenomenon. Incidental fm on the other hand is a fairly rapid random frequency shift or perturbation. It can be analyzed as a narrowband fm modulation process. When this is due to power supply line related ripple, we get coherent sidebands. These can be quite troublesome for a high resolution instrument like the 7L18. The sideband noise pedestal shows the "far down" stability performance of the oscillator.

Fig. 2. Block diagram of 7L18 phase lock system. The inner loop serves as the frequency reference for the outer loop.



Unfortunately, the stabilization circuitry affects the three stability elements differently. The choice of performance is, therefore, a matter of compromise.

Drift and incidental fm are closely related to sweep or tuning width and to the isolation of the oscillator from the environment. A wide tuning circuit must, by it's very nature, have elements which greatly affect frequency. If uncontrolled environmental factors such as voltage or temperature get into the frequency sensitive elements of the oscillator, then we have drift and incidental fm. The solution is two fold—reduction of frequency sensitivity and isolation from the environment.

Frequency sensitivity is reduced by locking the main oscillator to as narrow a tuning reference as feasible. Some of the efforts at reducing reference sweep and tuning range have already been discussed. In addition, many not so obvious steps have been incorporated. Observe from figure 2 that the basic crystal reference oscillators differ from each other by only 8 kHz, i.e., 15.800 MHz and 15.808 MHz. Eventually, of course, this small difference is multiplied to become 1 MHz steps (2 GHz/16 MHz=125, 8 kHz X 125=1 MHz). The offset oscillator moves 640 kHz/64=10 kHz. This gives extraordinarily little overlap when switching between the four reference crystals. Oversweep, false locks, failure to switch crystals, or failure to lock to the right crystal can all cause annoyances or worse. The usual procedure is to have plenty of oversweep range for safety. Not so in the 7L18. Here extra effort in the lock, search, and control circuitry was traded for a narrower sweep range.

Once the main oscillator is locked to a reference, the sideband phase noise characteristics are determined mainly by the reference oscillator and lock loop bandwidth. Obviously, great care must be taken to make the basic reference oscillator as clean as possible. This involves choice of crystals (type of cut, Q, mounting etc.), choice of circuit, and isolation from the outside environment. But even the best reference has a wideband noise floor and the sideband noise level comes up as 20 logM (M=multiplication ratio). Therefore, the higher the reference frequency the better. For the 7L18, the basic reference frequency is 4 MHz (16 MHz÷4). This is multiplied by 500 times to get to 2 GHz, producing a 54 dB increase in apparent reference sideband noise. Had we used a 1 MHz reference the increase would have been 12 dB worse.

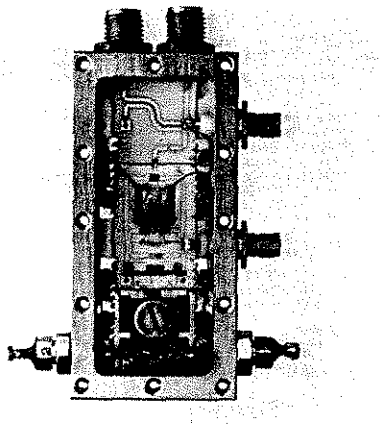
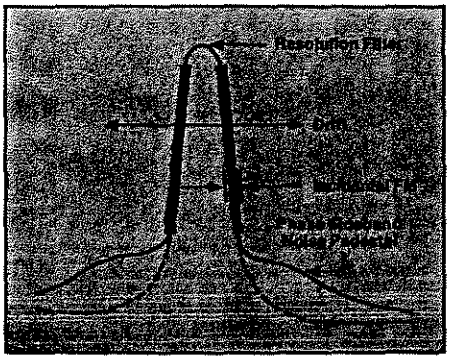


Fig. 3. Phase gate assembly includes a 2-4 GHz coupler, a resistive power divider, two terminated sampling diode chips, a combiner and integrator to drive the error amplifier, and two couplers to couple the strobe pulses into the sampling diode lines.

Fig. 4. An illustration showing the three elements affected by phase lock stabilization — drift, incidental fm, and phase sideband noise.



This performance area is accentuated in the 7L18 because of the sharp 4:1 resolution shape factors. More gradual resolution bandwidth roll off permits use of a dirtier lock reference since the phase noise can not be resolved. As a consequence it was considered worth the complexity to go to a four crystal reference system in order to save up to 12 dB on phase noise.

Finally, it is essential that sensitive circuits be well isolated from undesirable outside influences. The crystal oscillators are separated from the offset VCO by a mu-metal housing. The reference oscillator system sits in a separate compartment of a multicompartment milling. Other elements of the phase lock system are mounted in the remaining compartments of the milling. As a final measure, all compartments are enclosed on both sides by mu-metal plates. Input and output connections are handled through special feedthrough capacitors to create the highly isolated compartment shown in figure 5.

A closer look

Now let's take a closer look at how the phase lock circuitry does its job. It is easier to understand if we discuss it in two parts. The first covers the generation of the strobe, or reference frequency, to which the YIG oscillator is locked. This is called the inner loop. The second part discusses the circuitry necessary to lock the YIG oscillator to the strobe; we call this the outer loop (see figure 2).

The inner loop

As you can see from the block diagram in figure 2, the inner loop consists of three oscillators: a stable crystal reference oscillator (referred to as the reference oscillator), a moveable reference oscillator (referred to as the offset oscillator), and the controlled oscillator, which is phase locked to the sum of the reference and offset oscillators. The controlled oscillator frequency is divided by four and used as the

source for the strobe driver. This strobe is used as the reference to which the YIG tuned (2-4 GHz) first LO of the 7L18 is phase locked.

The reference oscillator is comprised of four crystal resonators at 15.800, 15.808, 15.816, and 15.824 MHz. A 1 Hz change in this oscillator moves the strobe 125 Hz at 2 GHz and about 250 Hz at 4 GHz when the offset oscillator is centered at 12.8 MHz. Therefore, the 8 kHz spacing between crystal frequencies moves the strobe lines in increments of 1 MHz at 2 GHz. Both the positive and negative supplies of the reference oscillator are zener referenced to reduce the affects of power supply variations and coherent side bands from other circuits in the 7L18.

We use the offset oscillator to sweep the controlled oscillator for interpolating between lock points, and to provide fine tuning. The offset oscillator frequency is divided by 64, then added to the reference oscillator frequency, and again divided by 4 for a total division ratio of 256. When locking the YIG oscillator at 2 GHz, the strobe signal is multiplied up about 500 times, depending on the reference oscillator frequency. This means that a 1 Hz change in the offset oscillator will move the YIG oscillator frequency about 2 Hz (500/256) when the strobe line is at 2 GHz. You will recall that the multiplication ratio depends on the YIG oscillator frequency, thus a 1 Hz change in the offset oscillator will cause a 4 Hz change in the strobe line at 4 GHz.

Because of noise consideration, limitations on the linear sweeping range of the offset oscillator, and the bandwidth of the 16.012 MHz crystal filter, the recentering range of the offset oscillator is only 1.2 MHz on-screen at 2 GHz. Consider that at 2 GHz, the strobe must also move 500 kHz (±250 kHz) to give a fine tuning range of one screen diameter in the widest phase lock position, plus provide a sweep of 500 kHz. This means that the strobe must move another 1 MHz. The total range of the YIG oscillator, therefore, must be 2.2 MHz at 2 GHz. Hence, the offset oscillator must move 1.1 MHz because of the 2:1 multiplication ratio discussed previously. In the offset oscillator circuitry, the varactor, zener diode and operational amplifiers must be carefully selected for noise to give good performance at an equivalent YIG oscillator frequency of 12 GHz. This is equivalent to looking at the 12th harmonic of the offset oscillator.

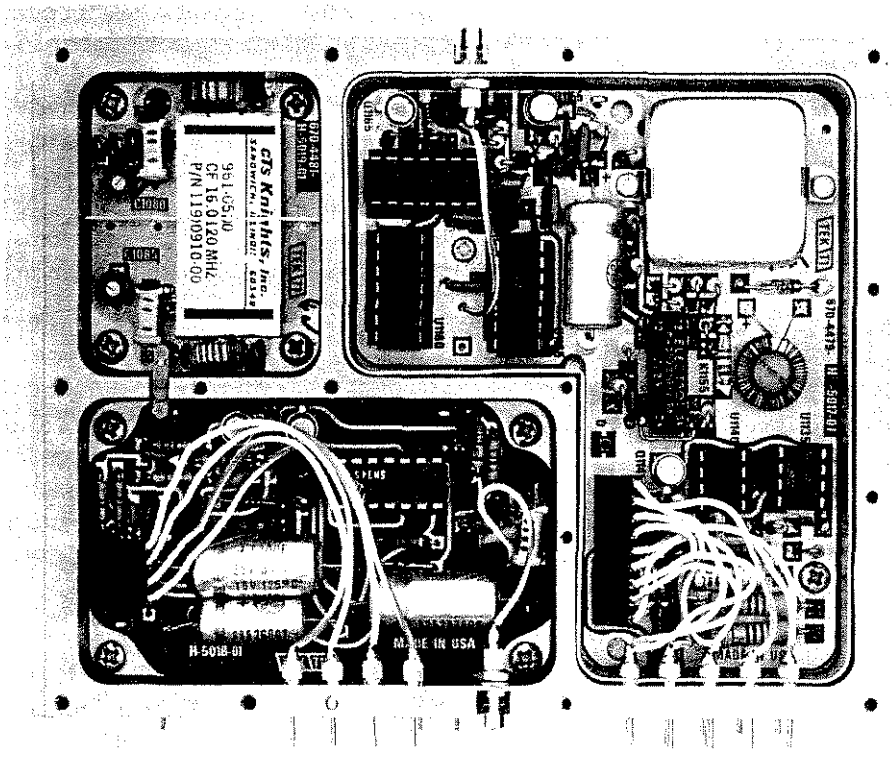
A mixer combines the reference oscillator, at about 15.8 MHz, with the controlled oscillator, at about 16 MHz. The difference frequency of 200 kHz is applied to the phase/frequency detector through a low pass filter which prevents the 15.8 MHz and 16 MHz signals from getting into the phase detector. These frequencies combine with harmonics of the 200 kHz to produce a family of crossover spurious responses which must be down 150 dB–no small task. Careful shielding is a must at this point.

A phase/frequency detector and compensation amplifier (Fs) lock the output from the mixer, to the offset oscillator. This lock loop has a bandwidth of about 10 kHz because it must be swept.

The output signal from the controlled oscillator is filtered by a 6-pole monolithic filter to remove the residual 200 kHz sideband (200 kHz being the update rate of the phase/frequency detector) before going to the strobe driver.

One final comment on the inner loop function. Since the strobe rate is about 4 MHz, there will be a strobe frequency line approximately every 4 MHz to some frequency greater than 4 GHz, (the upper end being determined by the bandwidth of the phase gate sampler). At 2 GHz, the strobe frequency increments in 1 MHz steps when a crystal in the reference oscillator is replaced by an adjacent crystal. The range allowed in the offset oscillator moves the strobe 1.2 MHz at 2 GHz to give a 20% overlap

Fig. 5. Milled housing contains phase lock system. Mu-metal shielding is used extensively to create highly isolated compartments.



(see figure 6). At 4 GHz, the minimum spacing due to incrementing a crystal is 2 MHz. However, the strobe harmonic at 4 GHz now moves twice as far, or 2.4 MHz, when the offset oscillator is varied before, thus no additional range is required from the offset oscillator.

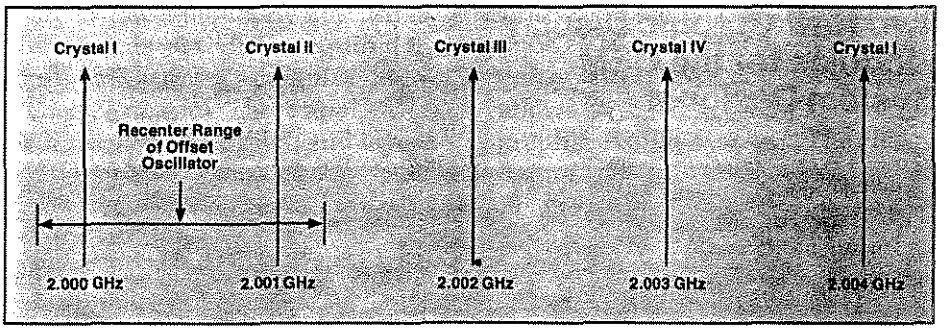


Fig. 6. The recenter range of the offset oscillator is ±20% to provide adequate overlap between adjacent crystals.

The outer loop

The discussion thus far has been concerned with the generation of the strobe reference. Now let's consider the loop that locks the YIG oscillator to this reference. The outer loop portion of the block diagram is shown in figure 2.

The outer loop performs a host of functions as follows:

- Connects the compensation amplifier to the YIG oscillator when in phase lock positions
- Provides search when not locked
- Delays connecting the error amplifier after the strobe is turned on
- Varies lock-in range as a function of tune voltage
- Commutates between crystals in the reference oscillator
- Locks the YIG oscillator to the strobe
- Senses when lock is achieved
- Moves the strobe reference to recenter the YIG oscillator
- Connects the sweep and offset oscillator filter after lock occurs
- Limits hold-in range

The compensation amplifier and search oscillator form a conditionally stable amplifier that requires the phase lock loop to have acquired, to become stable. When the loop is not locked, the compensation amplifier oscillates at about a 3 Hz rate. As the amplifier oscillates, the YIG oscillator searches an amount somewhat greater than MHz.

The search voltage moves the oscillator more than the distance between strobe lines to ensure that neither temperature effects nor dc balance errors from the phase gate will change the lock-in range. As we discussed earlier, the lock-in range when the YIG oscillator is at 2 GHz must be greater than 1 MHz, the spacing between crystals, and less than 1.2 MHz, the maximum recenter range of the offset oscillator. At 4 GHz these numbers are 2 MHz and 2.4 MHz respectively.

The output voltage of the search oscillator is monitored, and when this voltage exceeds an absolute value determined by the tune voltage, a lock inhibit command is given. In this manner, the allowable lock-in range is varied a factor of two as the oscillator is moved from 2 to 4 GHz.

When the allowable lock-in range is exceeded, it means the oscillator was not able to acquire lock with the crystal in use, and a new crystal is selected. The inner loop has time to settle before the search oscillator comes back into lock-in range and the new crystal is tried.

Eventually the YIG oscillator locks to the strobe reference and the search oscillator stops oscillating. When this happens, lock is sensed after a fixed period of time has elapsed to ensure that the lock is real. The crystals are then no longer allowed to change.

The next step is to recenter the YIG oscillator so that a signal on-screen will be in the same place as before the lock was initiated. This is done by applying a correction voltage to the offset oscillator from an 8-bit digital-to-analog converter, until the error voltage from the phase gate is zero. This D/A must be very stable to ensure low drift of the offset oscillator. If, for some reason, the D/A doesn't have enough range to recenter the oscillator, the lock sequence is started again, with provisions to ensure that the next crystal in the sequence is the first tried.

After the YIG oscillator is locked to the strobe reference and returned to the frequency it was before lock was initiated, the sweep voltage is connected to the offset oscillator to sweep the reference. The bandwidth of the outer loop must be wide enough to ensure that the loop remains locked during sweep and retrace. This bandwidth is about 10 kHz for the 7L18. The hold-in range of the loop is about 4 MHz to allow for the sweep, fine tune range, and drift of the oscillator.

Morris Engelson, at left, is the dean of spectrum analyzers at Tek having been with the analyzer program since its inception. He has a B.S.E.E. '57 and M.S.E.E. '64 from CCNY. Steve Morton, at right, has worked on the 7L5, 7L12, and 7L18 programs. He earned his B.S.E.E. '70 at Oregon State and M.S.E.E. '73 at the Univ. of Portland.

Two New Graphic Display Modules for the OEM System Designer

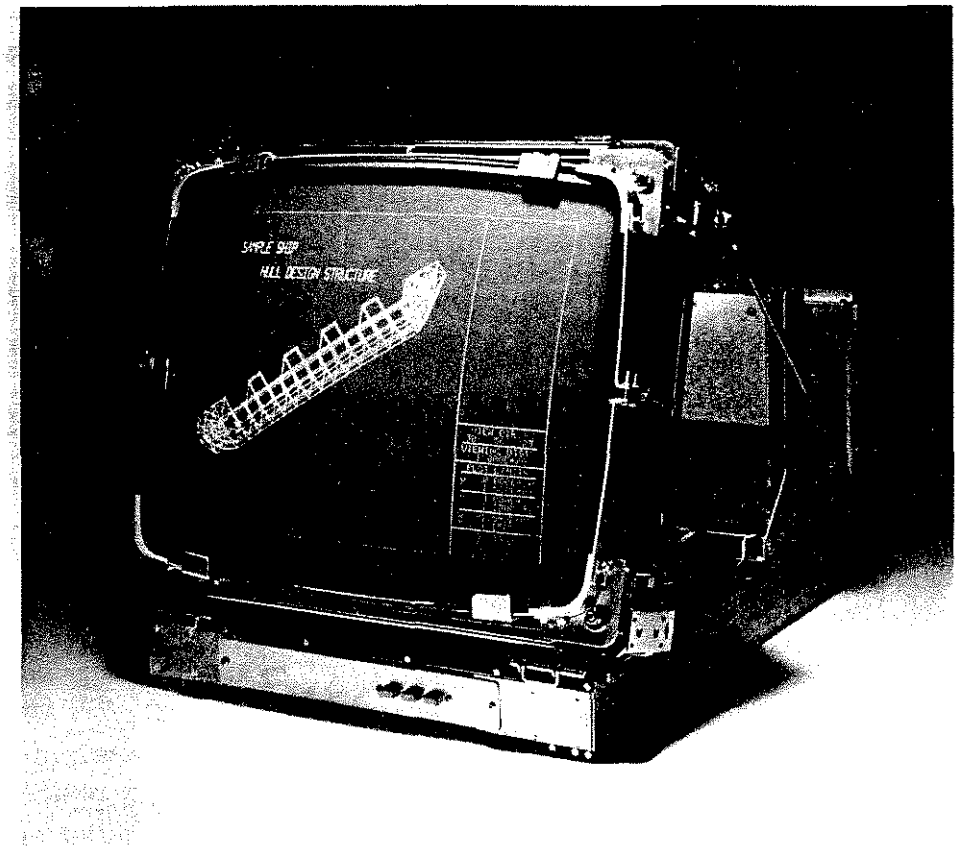


Fig. 1. The GMA101A Graphic Display Module designed specifically for the OEM market.

Business, engineering, science and education are all looking more and more to the computer to solve specialized problems. In the publishing field, large word processing systems with graphic display modules are used to layout and edit newspapers. Computerized circuit board layout systems are in use throughout the electronics industry. Programmed instruction systems can be found in elementary and secondary schools as well as in universities.

All these applications require the ability to interact with the system and graphically display words, images, or complex phenomena. Graphic displays are thus in increasing demand by system designers to help make these new, specialized computer systems more compatible with non-programmers and other "non-computer types," who will be using them.

To meet this demand, two new graphic displays, the TEKTRONIX GMA101A and the GMA102A, have been designed specifically for the OEM market.

Using its direct view storage tube (DVST) technology, Tektronix has for many years been a leader in the design and manufacture of high resolution, low cost graphic display modules and terminals. With this new OEM configuration, system designers can now tailor the DVST display to their specific system needs. In addition, the GMA series for the first time offers fully developed store-refresh capability, the ability to display stored and refreshed graphics on the DVST screen at the same time.

Lots of options

In designing the GMA series of graphic display modules for the OEM market, many packaging and performance options have been made available. Both the GMA101A and the GMA102A feature modular construction within a sturdy, wireform chassis. The 19-inch display screen can be oriented either horizontally (tv format) or vertically (page format), with a viewing angle of either 90° vertical or tilted back 15°. Each unit includes a power-supply, a vertical and horizontal amplifier circuit board, a high voltage and Z-axis board and a storage board. Space is available for three additional circuit boards, which can be selected from Tektronix' list of performance options or built by the OEM buyer. The list of performance options offered by Tektronix includes vector and character generator boards and extra current capacity for use by OEM-designed circuits. A hard copy interface is included as part of the standard display package. It can be removed, as an option, for OEMs who will never need hard copies directly from the display. Both basic display modules are all digital except for the X and Y inputs which are analog. With the interface options for both displays, the user also can drive the X and Y inputs digitally through use of a 16-bit, fully parallel, TTL-compatible format.

Low cost graphics

The GMA101A has the highest resolution for its price of any graphic display on the market. Since the image is stored on the phosphor of a DVST screen instead of in memory, is required with a refreshed display system, DVST displays allow high resolution, high density graphics to be displayed at a relatively low computer overhead. Over 3200 inches of vector or over 8500 alphanumeric characters can be stored on the 19-inch GMA101A splay screen.

The many peformance and packaging options available with the GMA101A make it usable in a wide variety of applications including word processing, graphic display terminals, and graphic work stations for computer aided design systems.

The best of both worlds

The GMA102A offers the same precision graphic displays offered by the GMA101A, with the addition of store-refresh. Along with stored graphics, up to 1500 inches of refreshed vector can be displayed with the GMA102A.

Combined storage-refresh displays have been made possible by the development of a DVST technique called write-through. Using write-through, intensity of the electron beam is slightly reduced to just below the storage threshold level. The beam then writes on the phosphor, but the image is not stored. By varying the beam intensity, information can be displayed in a combination of storage and refresh.

In the past, the chief disadvantage of DVST displays has been the inability to selectively edit the display without erasing the whole screen. With the development of store-refresh, the GMA102A offers the best of both worlds: the low cost, high resolution graphic displays obtained with DVST storage and the selective erase obtained with refresh.

This combined storage-refresh display will be useful in applications where a moderate amount of display interactivity is required in the creation of very complex, high density graphics. These applications include the design and layout of IC masks and printed circuit boards, newspaper page composition, and map making.

Costs versus refresh

Designers of graphic display systems have traditionally made heavy demands on display technology. Computer aided design systems like those used in map making, for example, require precise, high resolution, high vector density displays. Of the four presently available display technologies—DVST, plasma, video (raster) and directed beam—only DVST and directed beam have been able to meet these demands. Both DVST and direct beam provide high resolution (60 to 110 addressable points per linear inch) and high density (from 3,000 to 10,000 inches of displayed vector). Directed beam displays are by nature refreshed systems and thus also provide selective erase capability. DVST displays have traditionally been pure storage devices, with no refresh capability. The ability to store a display on the screen phosphor, eliminating the need for costly refresh memory, however, allows the design of very low cost graphic display systems. The choice between DVST and directed beam has thus always been one of cost versus refresh.

A new question

With the recent reductions in the price of refresh memory, it appeared that directed beam displays were gaining on DVST in this competition. Now that store-refresh has been added to the picture, DVST displays should continue to offer the most favorable cost/performance combination for many years to come. System designers no longer will ask, "Do I need refresh?" The question is now, "How much refresh do I need?"

A good example of an application of the combined storage-refresh capability of the GMA102A is its use in a computer aided circuit board design system. Displaying all the runs and pads of a six layer circuit board with a refresh display requires a considerable amount of refresh memory. Using the

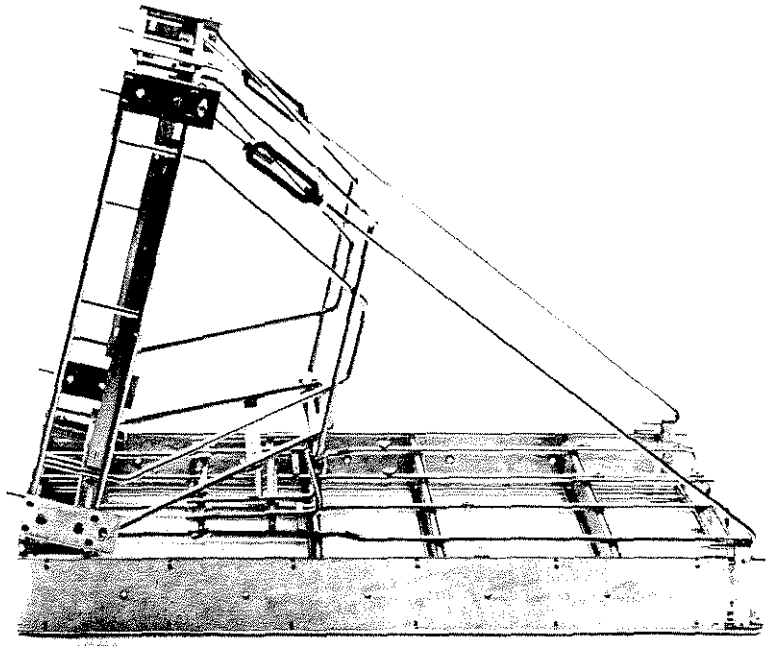


Fig. 2. The sturdy waveform chassis permits the 19-inch screen to be oriented vertically or horizontally with a viewing angle of 90 degrees vertically or tilted back 15 degrees.

High speed vector generation

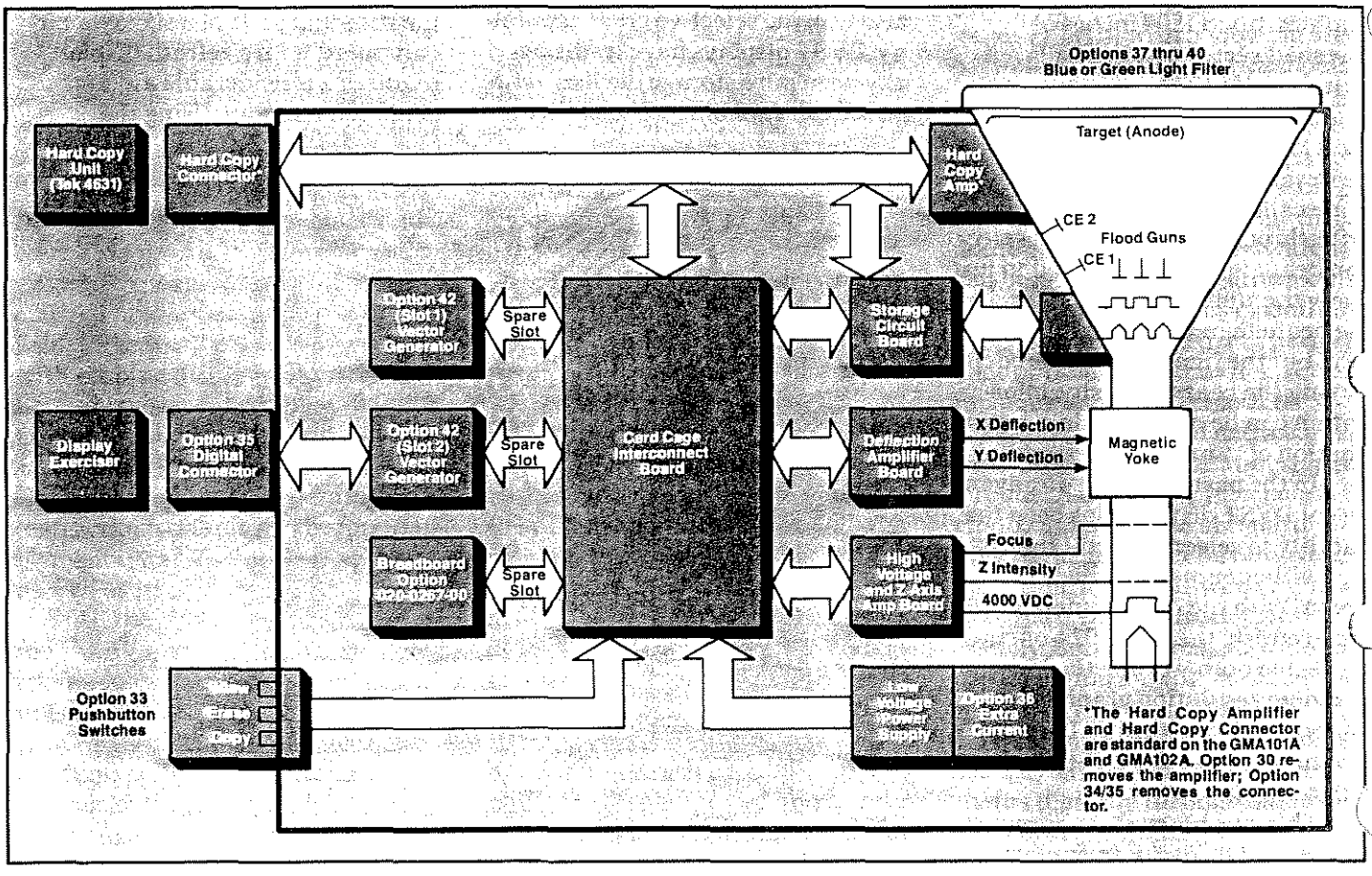
GMA102A, the circuit board layers can be designed and displayed one layer at a time in refresh. Once a layer has been brought-up and edited in refresh, it is stored on the display, and the next layer is started in refresh. This use of refresh and storage to build a circuit board allows selective editing of each layer, but requires only one-sixth the refresh memory (for a six layer board) of a directed beam display. To augment the write-through capability of the GMA102A, a high speed vector generator, option 42, and a high speed character generator, option 43, have been developed. These two options are available on separate circuit boards that plug into the spare circuit board connectors in the GMA102A. Complete digital interfacing to both these circuit boards eliminates the need for the OEM to design complex analog circuitry.

Option 42 utilizes a digitally based hardware vector generator algorithm and an active deglitching circuit to provide clear, high speed, repeatable graphic displays. With a writing rate of 90,000 cm per second, up to 1180 inches (3000 cm) of graphics refreshed at a 30 Hz rate can be displayed on the GMA102A using Option 42. Stored vectors can be drawn at up to 4000 inches per second.

This hardware vector generator provides theoretically 100% repeatability for each refresh cycle, with less than 0.05% of a full line length non-linearity. Fifteen different dash patterns and two line widths are provided. 12-bit positional resolution is used to achieve high precision positioning (absolute or relative) in 3.5 mil steps. The active deglitch circuit filters out noise at the digital-to-analog converter output to provide glitch free vectors. Besides drawing vectors to drafting-like standards, Option 42 draws vectors that are smooth. This is achieved by illuminated spot overlap—an outgrowth of the high addressability feature coupled with the essentially continuous nature of the GMA102A phosphor surface. Spot overlaps of 55%, worse case, are achieved on vectors written at even a 45 degree angle.

Option 43 provides four character fonts and the ability to create a display of over 400 refresh characters at a 30 Hz refresh rate. Both Opton 43 and Option 32 (a combined vector/character generator) feature interchangeable ROMs for alphabets and type faces. Made by Motorola, these ROMs can be purchased for different alphabets and type styles. The characters are created in a 7 x 9 dot matrix. In the

Fig. 3. Simplified block diagram of the GMA102A.



storage mode, Option 43 can generate up to 7000 small characters (90 x 110 mil) and 2000 large characters (160 x 195 mil) per second.

Option 32 is a storage-only vector/character generator circuit board for use with the GMA101A. It can draw stored vectors (absolute addressing only) at up to 3940 inches per second with 3.5 mil steps. It can generate 1000 large (160 x 195 mil) and 2000 small (90 x 100 mil) characters per second. A refreshed display cursor is also provided. As with Options 42 and 43, Option 32 features completely digital interfacing.

A practical, low cost, display exerciser is available as one of the support options. For OEMs, this exerciser is especially useful by their engineering group in verifying the display specifications and interfacing requirements. It is also useful by the OEM's manufacturing group in incoming inspection and quality control. In addition, a variety of other service devices and design aids, such as a breadboarding kit, are available for use by OEMs in making it easy for them to integrate the GMA displays into their systems.

Plenty of room for added value

The all-modular construction of the GMA series should be a welcome feature to OEM buyers. The wireform chassis construction method was selected because of its high strength-to-weight ratio, its openness, and the ease with which it can be modified. Cables can easily be threaded throughout the unit and card cage; additional modules can be added with little trouble.

The choice of vertical or horizontal display orientation is offered at no additional cost. Rackmounting is easily achieved.

The low voltage power supply module includes easy line voltage selection, fusing, appropriate heat sinks and a cable to distribute power to the circuit module. However, a line cord is not provided as OEMs desire the flexibility of connecting the unit directly into their console power distribution units.

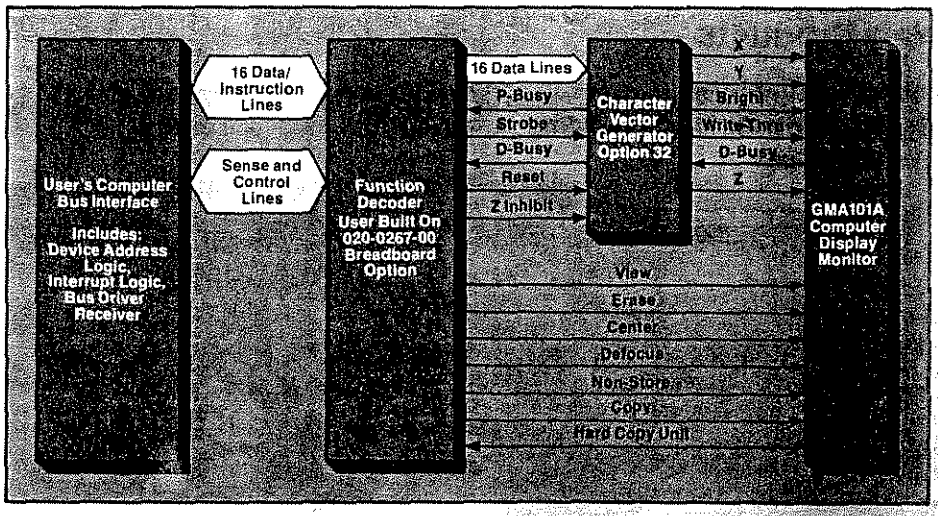
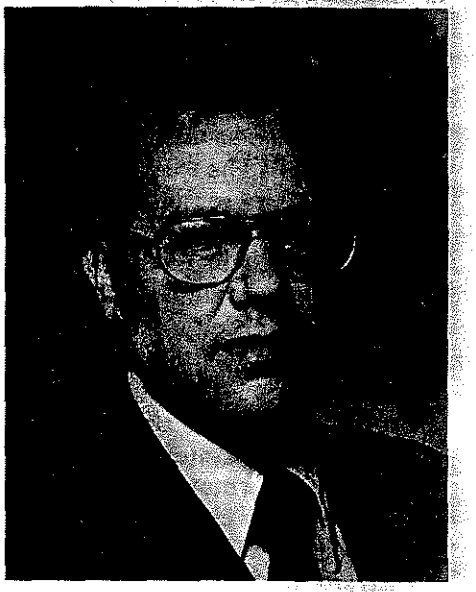


Fig. 4. Example of the GMA101A interfacing for use as a Graphic Work Station. Function Decoder is built by the user.

The circuit module provides an interconnect board with room for six plug-in circuit boards. Enclosed in a card cage, it offers easy performance modification and convenient access to components for service. The additional plug-in slots provide space for further product development by either the OEM or Tektronix. Besides the performance options already mentioned, this space could be used for a serial ASCII interface board, a keyboard interface, a microprocessor controller with local refresh memory, or a custom vector generator.

Graphics solutions for today and tomorrow

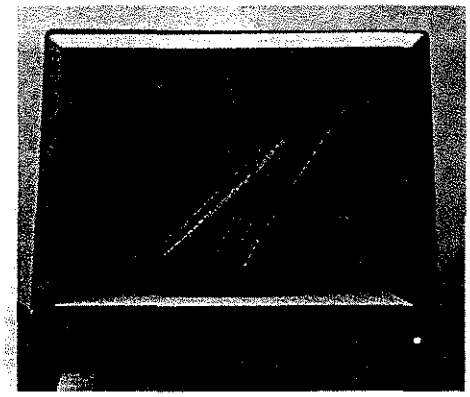
Tektronix has led the graphics display market for almost ten years in the development of low cost, high performance graphic display systems. With the development of store-refresh in the GMA series and a solid commitment to the OEM buyer, we believe that DVST technology will have a growing impact on the graphics display market for many years to come.



Dick Epler has been working in Marketing Product Development since coming with Tek in early '76. He has several years of marketing and sales experience in the computer field and five years as Instrument Research Engineer with Batelle Northwest. He received his B.S.E.E. '63 from Washington State University.

New Products

Finite Element Modeling System Reduces Model Building Time and Cost

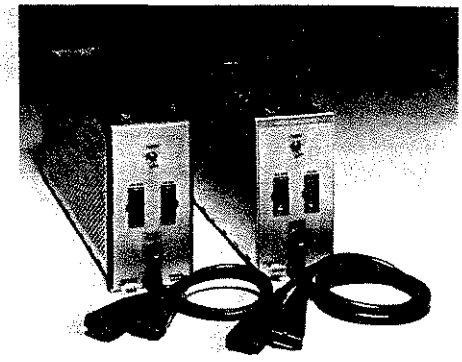


The TEKTRONIX FEM181 Finite Element Modeling System is designed to reduce the time it takes to build models and eliminate the time-share costs usually incurred by this activity. The FEM181 operates independent of the host computer. It allows the structural analyst to create models, for example, of a wheel or motor mount, wing or turbine blade; verify its accuracy, and format the model data into a form compatible with the input requirements of the host finite element analysis system. Once the data has been formatted, it is transferred to the host computer.

The basic system consists of a 19-inch storage-refresh cathode ray tube display, a terminal keyboard, a 10 megabyte disc memory, hard copy unit, and the flexible, finite element modeling software package. The software package is designed to speed model building, provide the analyst with a variety of modeling options, and make the system easy to learn.

For further information on the FEM181, use the inquiry card accompanying this issue.

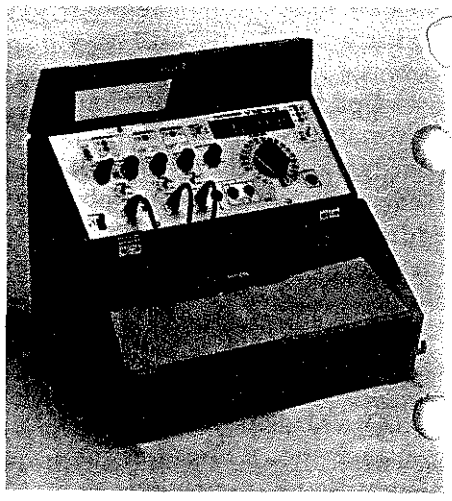
DL2 and DL 502 Digital Latches



Digital latching capability is now available for the 7D01 and LA 501W Logic Analyzers. The TEKTRONIX DL2 and DL 502 Logic Analyzer Digital Latches are designed to detect glitches in data that cannot be captured by the logic analyzer alone. Glitches as narrow as 5 ns can be latched and expanded for easy detection.

The DL2 is designed to plug into the 7000-Series Oscilloscopes and the DL 502 plugs into a TM 500 Mainframe. The latches enable the user to asynchronously capture pulses shorter than one sample interval, and both feature 16 channel latching capability.

A Versatile, New Digital Tester



The new TEKTRONIX 851 Digital Tester is a portable, easy-to-use digital tester ideal for field service and production testing. The 851 combines many of the functions of a DMM, counter, timer, logic probe, thermometer, and an oscilloscope in a single package weighing only 13 pounds/16 kg. One knob allows you to dial 22 different functions.

Eleven functions measure timing, two register plus and minus peak voltages, three carry out DMM measurements through separate leads, and one reads line voltage at the outlet. Another function allows you to take temperature measurements with an optional temperature probe. The 851 also makes four self-measurements to correctly adjust each of its four input thresholds to the logic levels of the equipment under examination.

Altogether these functions allow you to:

- Measure system parameters.
- Check for signal activity.
- Correct synchronization problems in electro-mechanical subsystems through adjustment or repair.
- Identify boards or component parts of the system in need of replacement.

The measurement capabilities of the 851 make it particularly suitable for servicing computer peripherals, small business systems, and industrial control equipment.

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