KAI-0372 Series

768(H) x 484(V) Pixel

Interline CCD Image Sensor

Performance Specification

Eastman Kodak Company

Microelectronics Technology Division

Rochester, New York 14650-2010

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1.1 Features

- **Front Illuminated Interline Architecture**
- **768 (H) x 484 (V) Photosensitive Pixels**
- **11.6mm(H) x 13.6mm(V) Pixel Size**
- **8.9 mm(H) x 6.6 mm(V) Photosensitive Area**
- **Progressive Scan (Noninterlaced)**
- **Electronic Shutter**
- **Integral RGB Color Filter Array (optional)**
- **Advanced 2 Phase Buried Channel CCD Processing**
- **On-Chip Dark Reference Pixels**
- **Low Dark Current**
- **High Output Sensitivity**
- **Antiblooming Protection**
- **Negligible Lag**
- **2/3" Format Compatible**
- **Low Smear (0.01% with microlens)**

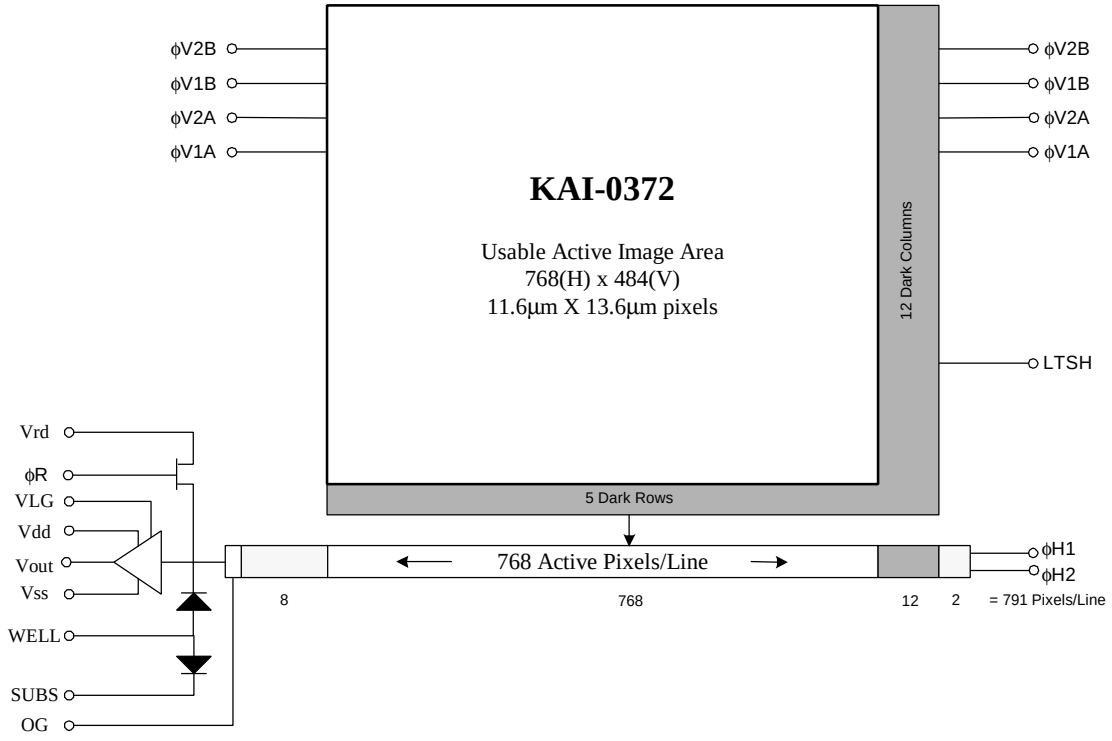

Figure 1 Functional Block Diagram

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1.2 Description

The KAI-0372 series is a high-performance silicon charge-coupled device (CCD) designed for video image sensing and electronic still photography. The device is built using an advanced true two-phase, double-polysilicon, NMOS CCD technology. The p+npn- photodetector elements eliminate image lag and reduce image smear while providing antiblooming protection and electronic-exposure control. The total chip size is 9.9 (H) mm x 7.7 (V) mm. The KAI-0372 comes in monochrome and color versions, both with microlens for sensitivity improvement.

Device	Color	Microlens
KAI-0372M	No	Yes
KAI-0372CM	Yes	Yes

1.3 Architecture

The KAI-0372 consists of 371,712 photodiodes, 768 vertical (parallel) CCD shift registers (VCCDs), one horizontal (serial) CCD shift register and one output amplifier. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The pixels are arranged in a 768 (H) x 484 (V) array in which an additional 12 columns and 5 rows of light shielded pixels are added as dark reference.

1.4 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

1.5 Charge Transport

The accumulated or integrated charge from each photodiode is transported to the output by a three step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock (ϕV2). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock, ϕH2, these charge packets are dumped over the output gate (OG, Figure 2) onto the floating diffusion (FDA Figure 2).

Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the horizontal CDD begins when ϕV2 is brought low (and ϕV1 high) causing a line of charge to transfer from ϕV2 to ϕV1 and subsequently into the horizontal register. The sequence completes when ϕV1 is brought low before the horizontal CCD reads the first line of charge.

1.6 Output Structure

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression ΔVfd=ΔQ/Cfd.

A three stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of μV/e^-. After the signal has been sampled off-chip, the reset clock (ϕR) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage (VRD).

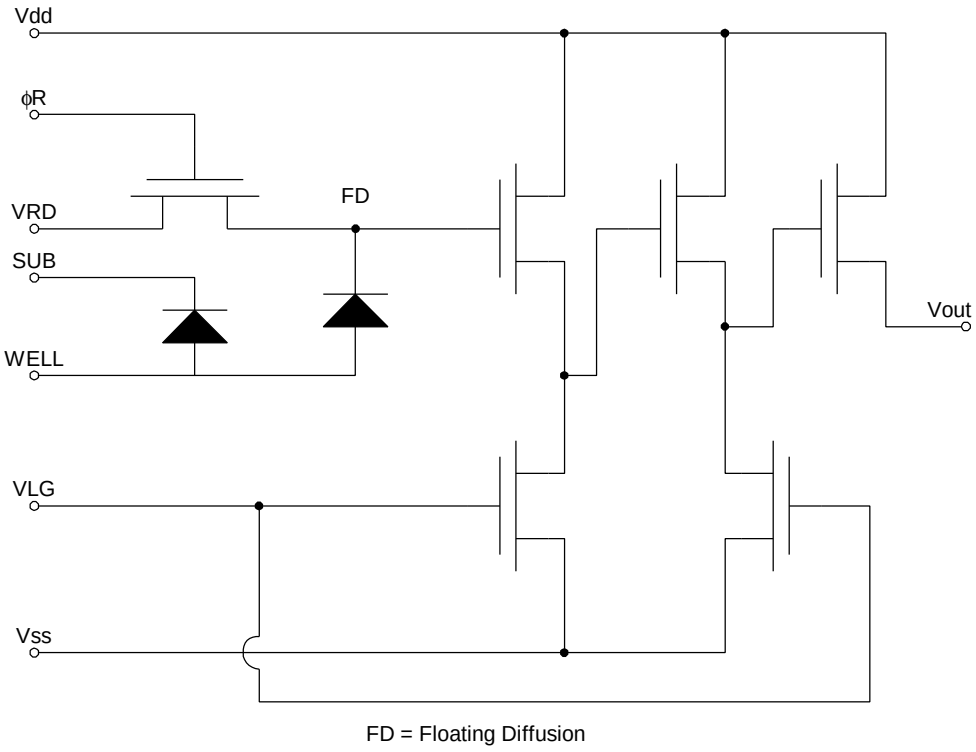

Figure 2 Output Structure

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1.7 Electronic Shutter

The KAI-0372 provides a structure for the prevention of blooming which may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD). This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse (VES ≈ 40V) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on ϕV2. The integration time is then the time between the falling edges of the substrate shutter pulse and ϕV2. This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feedthrough. The shutter pulse VES must be "hidden" in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

1.8 Color Filter Array (optional; for KAI-0372CM only)

The pattern used is the staggered "3G" color mosaic filter pattern (Figure 3), The CFA contains 75% green photosites and 25% red and blue photosites. Other CFA patterns may be available upon request.

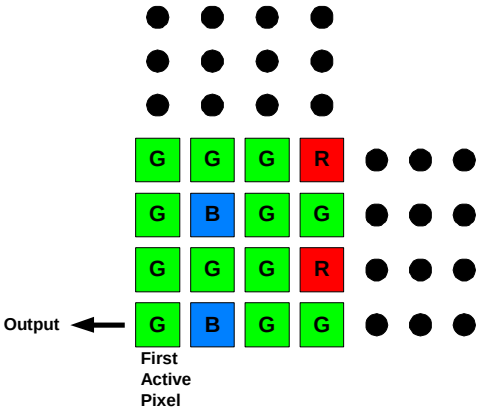

Figure 3 CFA Pattern

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1.9 On-Chip Gate Protection Circuitry

Gates OG, ϕR, VLG ϕH1 and ϕH2 are internally connected to diodes as shown in Figure 4 and Figure 5 to provide some gate protection from transient voltages more positive than the voltage applied to SUB. For this protection to work, SUB must be connected. This circuitry does not protect from all voltages more positive than SUB, or from any voltages more negative than SUB. Also application of voltages more positive than SUB for other than transient periods will forward bias the protection diode and may damage the sensor.

This sensor, like other MOS-based images sensors, is extremely sensitive to electrostatic discharge (ESD) damage. The handling and environment of the sensor must be controlled to protect this device from ESD damage.

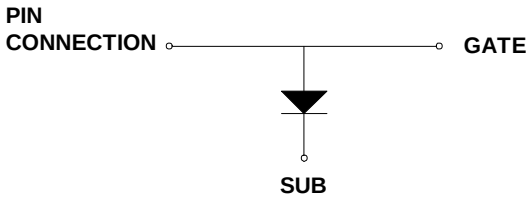

Figure 4
Internal Protection Circuit for ϕH1 and ϕH2

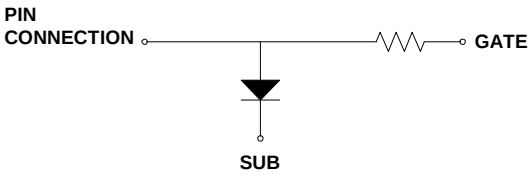

Figure 5
Internal Protection Circuit for OG, ϕR, and VGL

2.1 Packaging Configuration

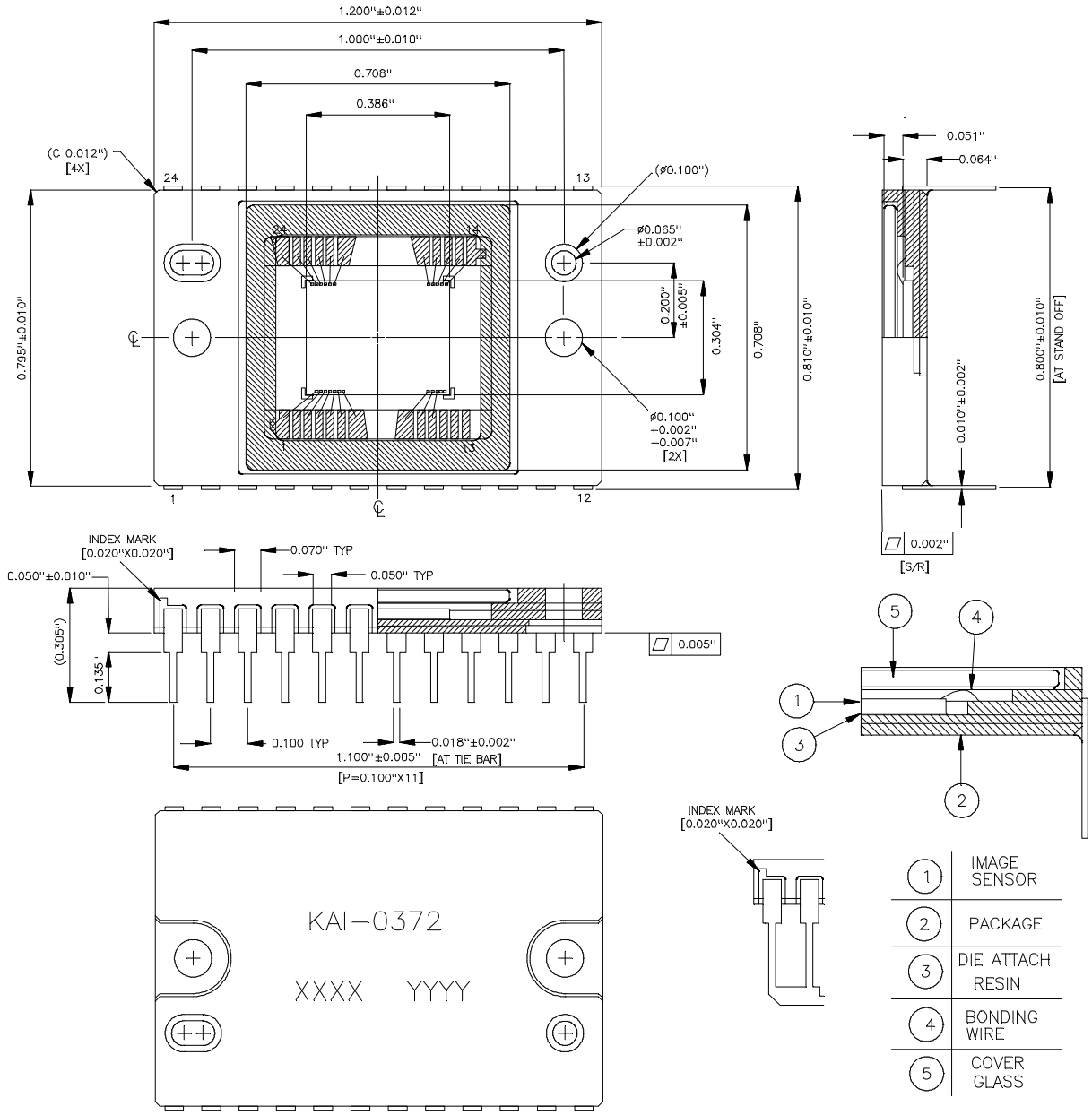

Figure 6 Device Drawing

2.2 Pin Description

PIN NO.	SYMBOL	DESCRIPTION
1	OG	Output Gate
2	ϕR	Reset Clock
3	VRD	Reset Drain
4	VSS	Output Amplifier Return
5	VLG	Output Amplifier Load Gate
6	VOUT	Video Output
7	VDD	Output Amplifier Supply
8, 20	WELL	

PIN NO.	SYMBOL	DESCRIPTION
9	ϕH2	Horizontal CCD Clock - Phase 2
10	ϕH1	Horizontal CCD Clock - Phase 1
11, 12, 13	NC	
14, 16, 22,24	ϕV2A, ϕV2B	Vertical CCD Clock - Phase 2
15, 17, 21, 23	ϕV1A, ϕV1B	Vertical CCD Clock - Phase 1
18	LTSH	Lightshield
19	SUB	Substrate

Table 1 Package Pin Assignments

Notes:

1. Pins 14, 16, 22, 24 must be connected together - only one Phase 2 clock driver is required.
2. Pins 15, 17, 21, 23 must be connected together - only one Phase 1 clock driver is required.

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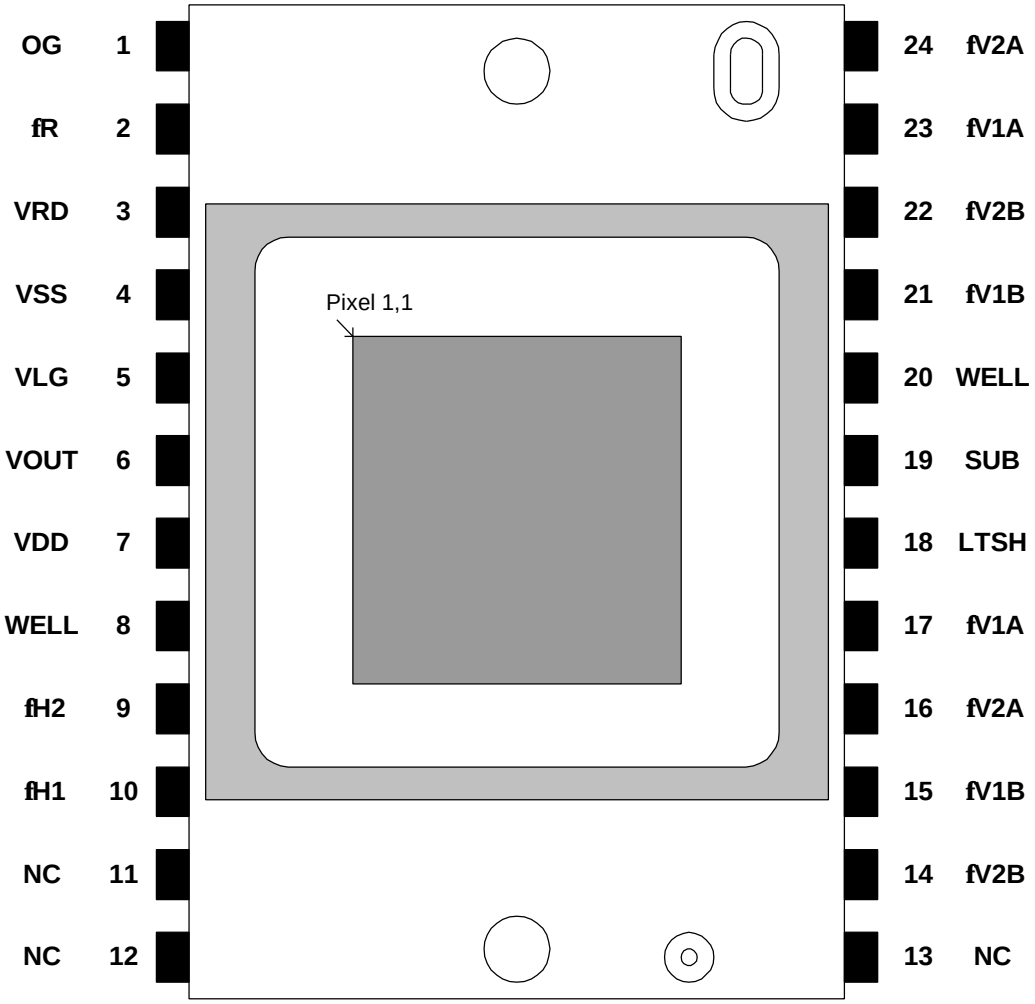

Figure 7 Pinout Diagram Top and Side Views

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2.3 Absolute Maximum Ranges

RATING	DESCRIPTION	MIN.	MAX.	UNITS	NOTES
Temperature (@ 10%±5%RH)	Operation to Specification	+25	+40	°C	
	Operation Without Damage	-25	+55	°C	
	Storage	-25	+70	°C	
Voltage (Between Pins)	SUB-WELL	0	+50	V	1
	VRD,VDD,&VSS-WELL	0	+25	V	2
	All Clocks - WELL		17	V	2
	ϕV1 - ϕV2		17	V	2
	ϕH1 - ϕH2		17	V	2
	ϕH1, ϕH2 - ϕV2		17	V	2
	ϕH2 - OG		17	V	2
	All Clocks - LTSH		17	V	2
	VLG, OG - WELL		17	V	2
	All Gates - LTSH		17	V	2
Current	Output Bias Current (IDD)	----	10	mA	
Capacitance	Output Load Capacitance (CLOAD)	----	10	pF	

Table 2 Absolute Maximum Ranges

Notes:
1. Under normal operating conditions the substrate voltage should be above +7V, but may be pulsed to 40 V for electronic shuttering.
2. Care must be taken in handling so as not to create static discharge that may permanently damage the device.

2.4 DC Operating Conditions

SYMBOL	DESCRIPTION	MIN.	NOM.	MAX.	UNITS	NOTES
OG	Output Gate	+1.5	+2.0	+2.5	V	
VRD	Reset Drain	+10.0	+10.5	+11.0	V	
VSS	Output Amplifier Return	+0.4	+0.5	+0.6	V	
VLG	Output Amplifier Load Gate	+1.7	+2.0	+2.5	V	
VDD	Output Amplifier Supply	+14.5	+15.0	+15.5	V	
WELL	Well		0.0		V	
LTSH	Lightshield		0.0		V	
SUB	Substrate	+7.0	Vab	+25	V	1
IOUT	Output Bias Current	3	5	7	mA	2

Table 3 DC Operating Conditions

Notes:
1. The operating value of the substrate voltage, Vab, will be marked on the shipping container for each device. The substrate is clocked in electronic shutter mode operation. A shutter pulse with voltage less than 50V for less than 100 µs is allowed. See AC Clock Level Conditions and AC Timing Requirements. Well and substrate biases should be established before other gate and diode potentials are applied.
2. A 1.8kΩ resistor between VOUT and ground is recommended to obtain IOUT = 5mA. VOUT must not be shorted to ground.

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2.5 AC Clock Level Conditions

SYMBOL	DESCRIPTION	MIN.	NOM.	MAX.	UNITS	NOTES
ϕV1H, ϕV2H	Vertical CCD Clocks - High	+14.5	+14.7	+15.0	V	1
ϕV1M, ϕV2M	Vertical CCD Clocks - Mid	-0.5	-0.2	0.0	V	1
ϕV1L, ϕV2L	Vertical CCD Clocks - Low	-9.0	-8.0	-7.0	V	1
ϕH1H, ϕH2H	Horizontal CCD Clocks - High	+1.0	+2.0	+3.0	V	1
ϕH1L, ϕH2L	Horizontal CCD Clocks - Low	-10.0	-9.0	-8.0	V	1
ϕRH	Reset Clock - High	+7.0	+8.0	+9.0	V	
ϕRL	Reset Clock - Low	+2.0	+3.0	+4.0	V	
VES (SUB)	For Electronic Shutter Pulse Only	+40	+42	+45	V	2

Table 4 AC Clock Level Conditions

Notes:
1. For best results, the CCD clock swings must be maintained at (or greater than) the values indicted by the nominal level conditions noted above.
2. This pulse, used only for electronic shutter mode operation, is applied to the substrate, as described in Section 1. Dynamic resistance is 3kΩ and typical DC current is 3 mA at VSUB = 40V.

This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

2.6 Clock Capacitances

SYMBOL	DESCRIPTION	TYPICAL	UNIT	NOTES
C ϕV1, ϕV2 (A, B combined)	Vertical CCD Clocks - Well	10	nF	
C ϕV1 - ϕV2 (A, B combined)	VCCD Clock Phase 1 - VCCD Clock Phase 2	1.5	nF	
C ϕH1, ϕH2	Horizontal CCD Clocks - Well	150	pF	
C ϕH1 - ϕH2	HCCD Clock Phase 1 - HCCD Clock Phase 2	60	pF	
C ϕR	Reset Clock - Well	5	pF	
C SUB	For Electronic Shutter Pulse	400	pF	

Table 5 Clock Capacitances

2.7 AC Timing Requirements

SYMBOL	DESCRIPTION	MIN.	NOM.	MAX.	UNITS	NOTES
t ϕVH	Vertical High Level Duration	5	17	20	µsec	
t ϕV	Vertical Transfer Time		2.8		µsec	
t ϕVPD	Vertical Pedestal Delay	10			µsec	
t ϕHD	Horizontal Delay	5.3			µsec	
t ϕR	Reset Duration	15	20	25	nsec	1
f ϕH	Horizontal Clock Frequency			14.32	MHz	
t L	Line Time		63.5		µsec	
t ϕVD	Vertical Delay	200			nsec	
t ϕHVES	Horizontal Delay with Electronic Shutter	1.0			µsec	
t cd	Clamp Delay				nsec	2
t sd	Sample Delay				nsec	2
t es	Electronic Shutter Pulse Duration	4	5		µsec	3

Table 6 AC Timing Requirements

Notes:
1. The rising edge of ϕR should be coincident with the rising edge of ϕH2, within ±5 nsec.
2. The clamp delay and sample delay should be adjusted for optimum results.
3. This pulse is used only with electronic shuttering and should not be used during horizontal readout. The electronic shutter pulse should be hidden in the horizontal retrace interval.

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Frame Timing

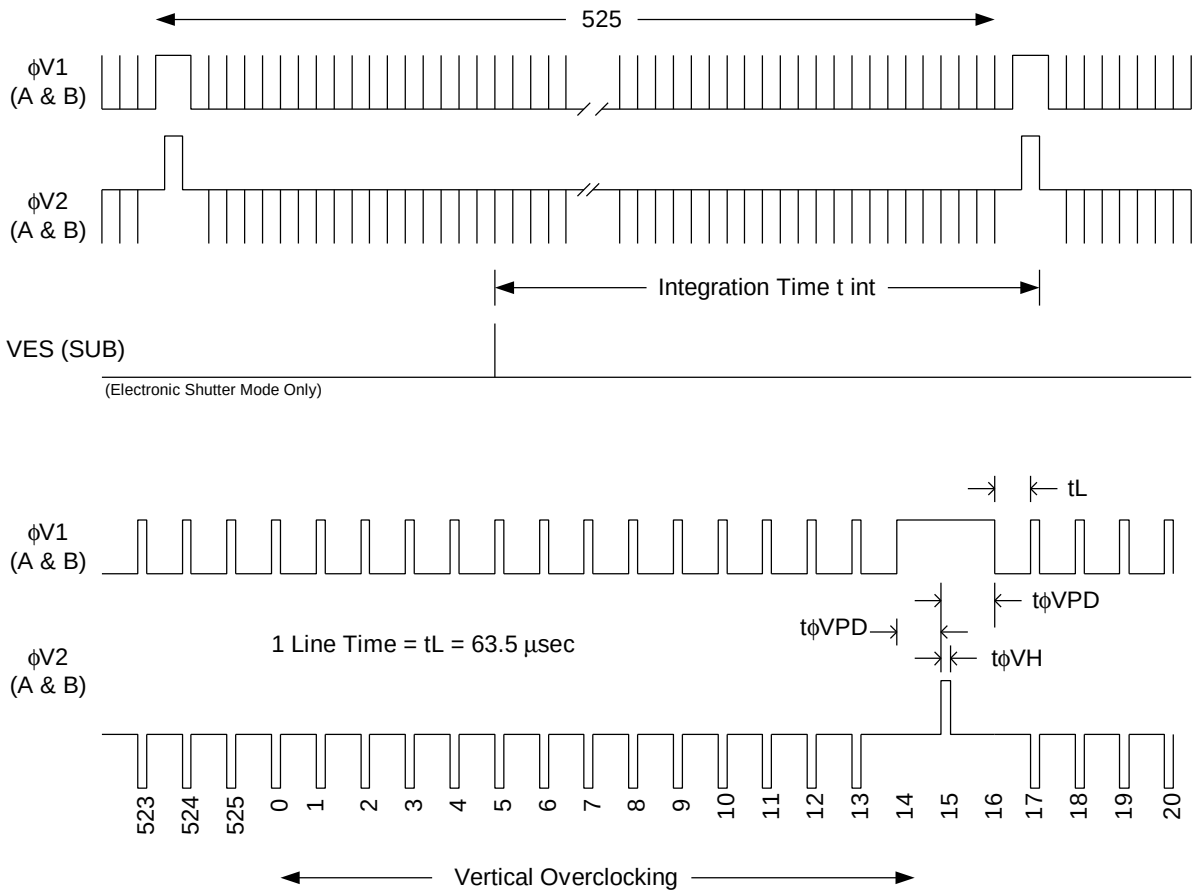

Figure 8 Frame Timing

Note: When no electronic shutter is used, the integration time is equal to the frame time.

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Line Timing

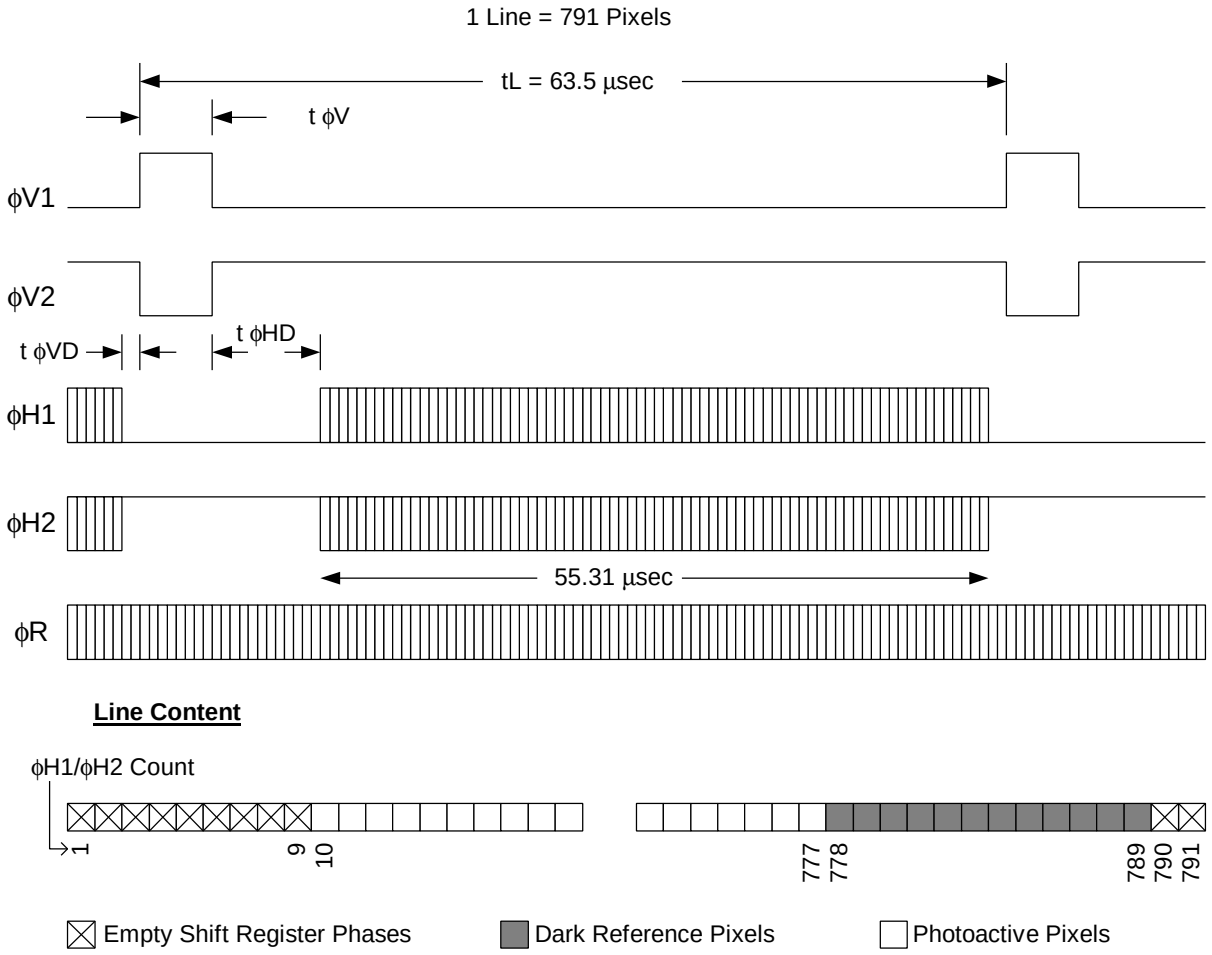

Figure 9 Line Timing

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Pixel Timing

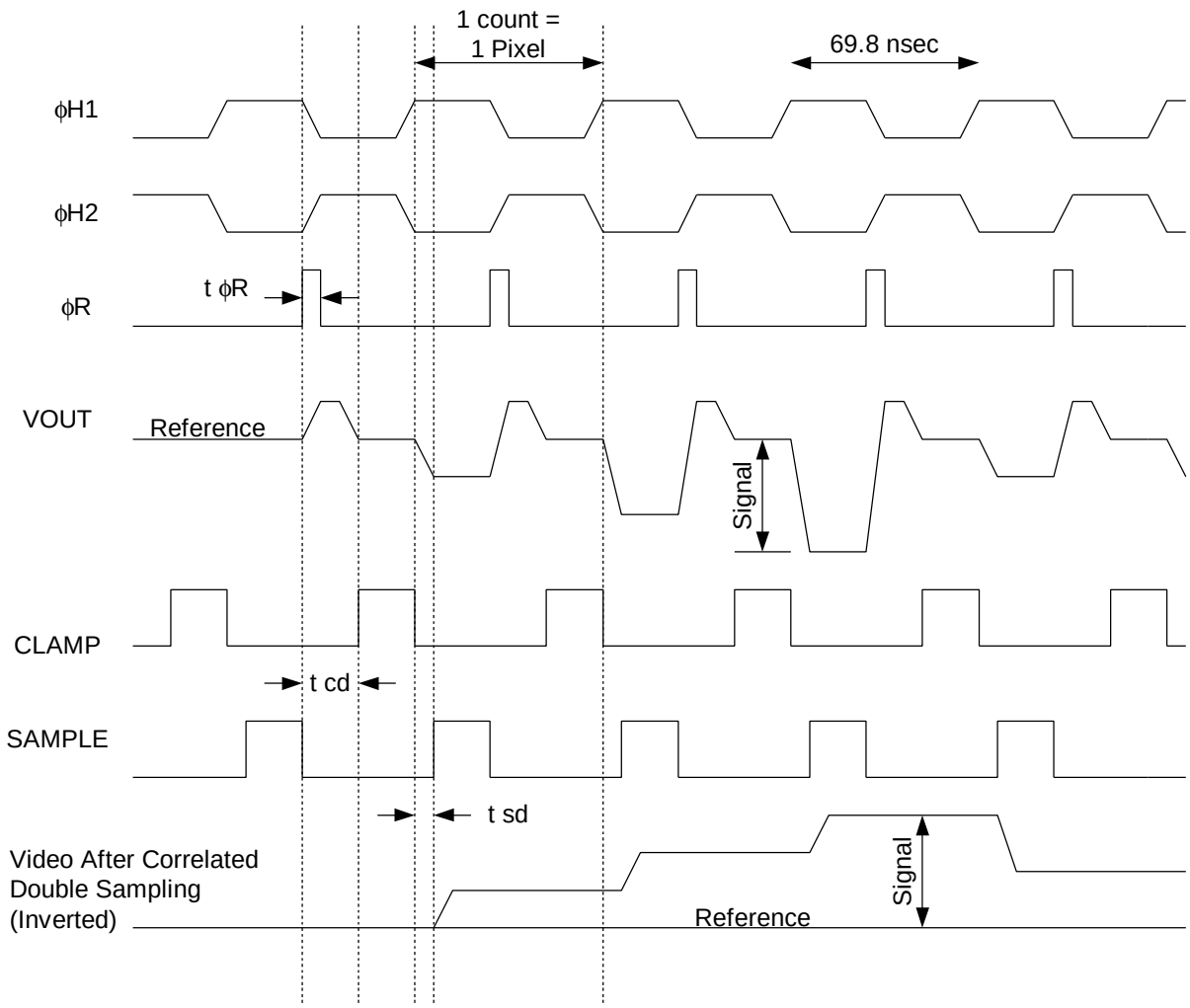

Figure 10 Pixel Timing Diagram

Electronic Shutter Timing

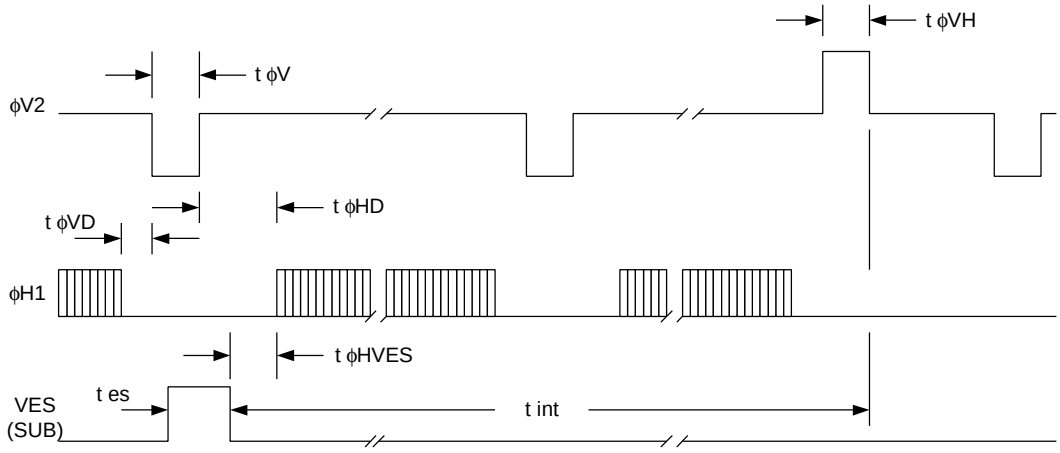

Figure 11 Electronic Shutter Timing Diagram - Single Register Readout

2.8 CCD Clock Waveform Conditions

SYMBOL	DESCRIPTION	twh	twl	tr	tf	UNITS	NOTES
ϕV1M	Vertical CCD Clocks - Phase 1	2.8	59.8	0.6	0.3	µsec	1
ϕV2M	Vertical CCD Clocks - Phase 2	60.0	2.5	0.5	0.5	µsec	1
ϕV2H	Vertical CCD Clocks - Phase 2, High	17	------	0.5	0.5	µsec	1
ϕH1	Horizontal CCD Clocks - Phase 1	25	27	8.5	8.5	nsec	1
ϕH2	Horizontal CCD Clocks - Phase 2	25	27	8.5	8.5	nsec	1
ϕR	Reset Clock	20	40	4.0	5.0	nsec	1
VES (SUB)	For Electronic Shutter Pulse Only	5	------	0.2	0.2	µsec	1

Table 7 CCD Clock Waveform Conditions

Note:
1. Typical values measured with clocks connected to image sensor device.

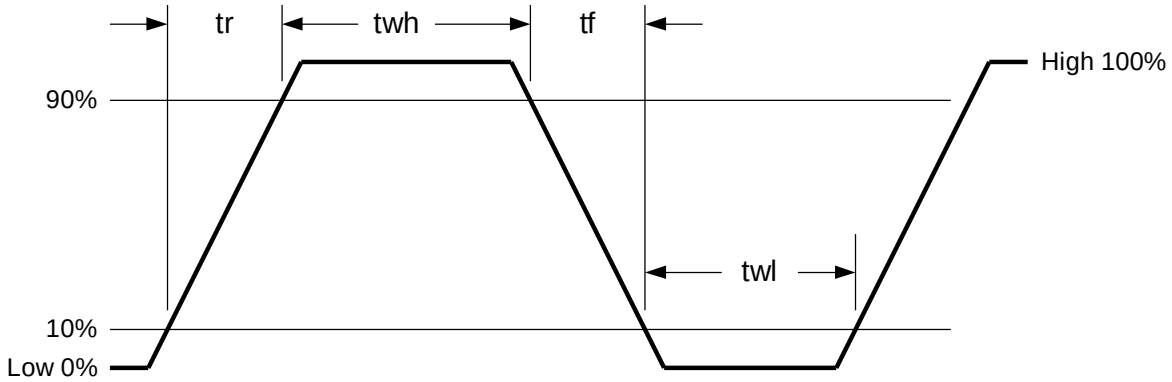

Figure 12 CCD ClockWaveform

3.1 Image Specifications

All following values were derived for the KAI-0371M series devices (with microlens array) using nominal operating conditions and the recommended timing. Unless otherwise stated, readout time = 33 msec, integration time = 33msec, no electronic shutter pulse is applied, and sensor temperature = 40°C. Correlated double sampling of the output is assumed and recommended. Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

Electro-Optical for KAI-0372M

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Esat	Saturation Exposure		0.044		$\mu J/cm^2$	1
QE	Peak Quantum Efficiency		30		%	2
PRNU	Photoresponse Non-uniformity			2.0	% rms	3
PRNL	Photoresponse Non-linearity			2.0	%	
Rs	Photoresponse Shading			10	%	4

Table 8 Electro-Optical Image Specifications KAI-0372M

Notes:
1. For λ = 530nm wavelength, and Nsat= 55ke$^-$
2. Refer to typical values from Figure 13 – Nominal KAI-0372M Spectral Response.
3. For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal. Saturation signal, Vsat, is the output voltage at the knee of the output vs illumination curve as shown in Figure 15 – KAI-0372 Series Photoresponse
4. This is the global variation in chip output across the entire chip measured at 80% saturation and is expressed as a percentage of the mean pixel value. Saturation signal, Vsat, is the output voltage at the knee of the output vs illumination curve as shown in Figure 15.

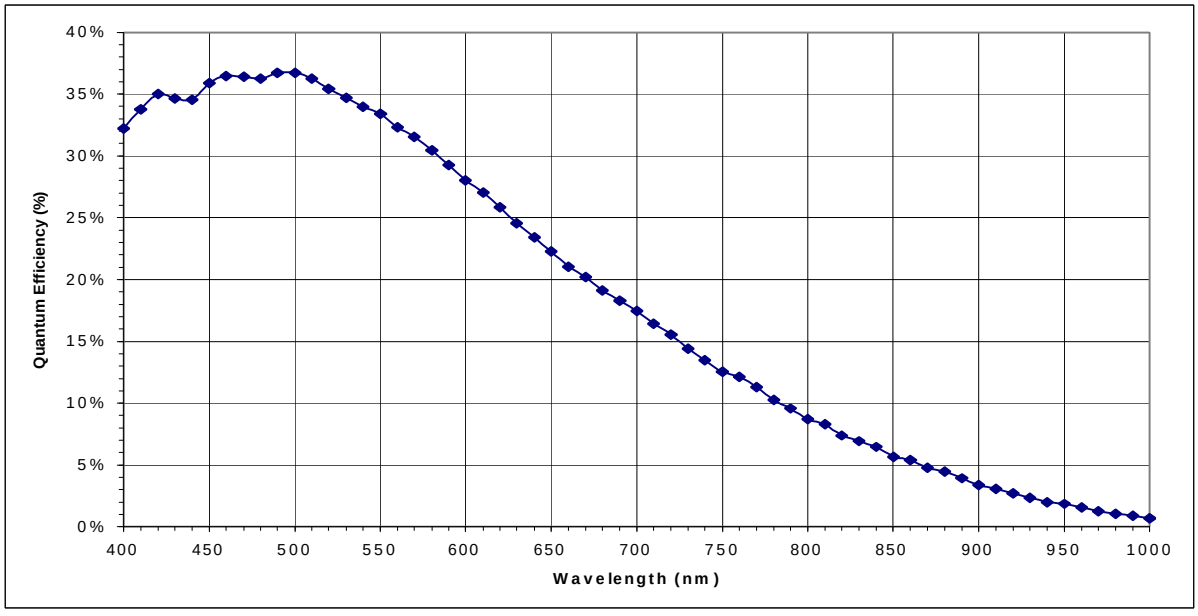

Figure 13 Nominal KAI 0372M Spectral Response

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Electro-Optical for KAI-0372CM

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Esat	Green Pixel Saturation Exposure		0.059		$\mu J/cm^2$	1
QEr	Red Peak Quantum Efficiency λ = 650 nm		12		%	2
QEg	Green Peak Quantum Efficiency λ = 530 nm		20		%	2
QEb	Blue Peak Quantum Efficiency λ = 450 nm		17		%	2
PRNU	Photoresponse Non-uniformity			5.0	% rms	3
PRNL	Photoresponse Non-linearity			2.0	%	
Rgs	Green Photoresponse Shading			10	%	4

Table 9 Electro-Optical Image Specifications KAI-0372CM

Notes:
1. For λ = 530nm wavelength, and Vsat = 55ke$^-$.
2. Refer to typical values from Figure 14, Nominal KAI-0372CM Spectral Response
3. For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal. Saturation signal, Vsat, is the output voltage at the knee of the output vs illumination curve as shown in Figure 15, Typical KAI-0372 Series Photoresponse
4. This is the global variation in chip output for green pixels across the entire chip measured at 80% saturation and is expressed as a percentage of the mean pixel value. Saturation signal, Vsat, is the output voltage at the knee of the output vs illumination curve as shown in Figure 15.

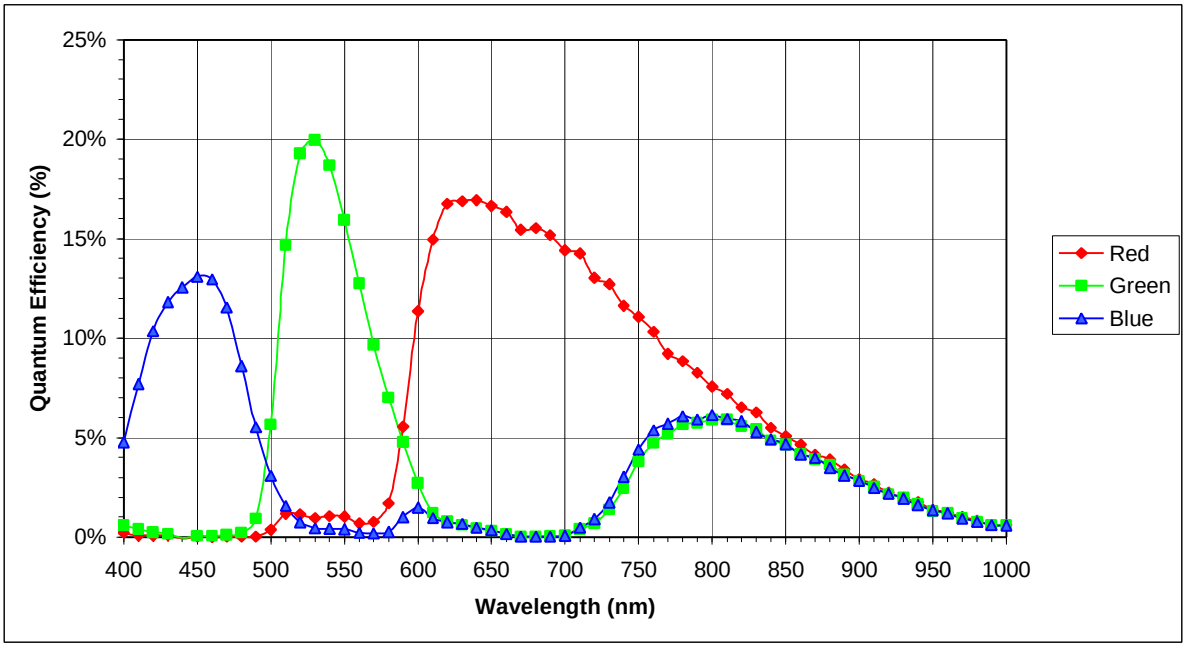

Figure 14 Nominal KAI-0372CM Spectral Response

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CCD

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Ne^-sat	Saturation Signal - VCCD	55			ke^-	
Vsat	Output Saturation Signal	500			mV	1, 2, 6
Id	Photodiode Dark Current			0.5	nA	
CTE	Charge Transfer Efficiency		0.99999			2, 3
f_H	Horizontal CCD Frequency		14.3		MHz	
IL	Image Lag		negligible			
Xab	Blooming Margin		300			4, 6
Smr	Smear		0.01	0.04	%	5

Table 10 CCD Image Specifications

Notes:

1. Vsat is the mean value at saturation as measured at the output of the device with Xab=300. This value is guaranteed only when Vsub=Vab as indicated on the sensor package. Vsat can be varied by adjusting Vsub.
2. Measured at the sensor output.
3. With stray load capacitance of C_L = 10pF between the output and AC ground.
4. Xab represents the increase above the saturation-irradiance level (Hsat) that the device can be exposed to before blooming of the vertical shift register will occur. It should be noted that Vout rises above Vsat for irradiance levels above Hsat.
5. Measured under 10% (~48 lines) image height illumination with white light source and without electronic shutter operation and below Vsat.
6. It should be noted that there is a tradeoff between Xab and Vsat.

Output Amplifier @ V_{DD} = 15V, V_{SS} = 0.5V

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vodc	Output DC Offset	5	6.3	7.5	V	
Pd	Power Dissipation		75		mW	
f_{-3db}	Output Amplifier Bandwidth	100			MHz	1
$\Delta Vo/\Delta N$	Sensitivity (Output Referred)		9		$\mu V/e^-$	
C_L	Off-Chip Load			10	pF	

Table 11 Output Amplifier Image Specifications

Notes

1. With stray output load capacitance of C_L = 10 pF between output and AC ground.

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General

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Ne^- total	Total Sensor Noise		55		e^- rms	1
DR	Dynamic Range		60		dB	2

Table 12 General Image Specifications

Notes:
1. Includes amplifier noise, dark pattern noise and dark current shot noise at data rates of 14 MHz.
2. Uses 20 LOG (Ne^-sat/Ne total) where Ne^-sat refers to the vertical CCD saturation signal.

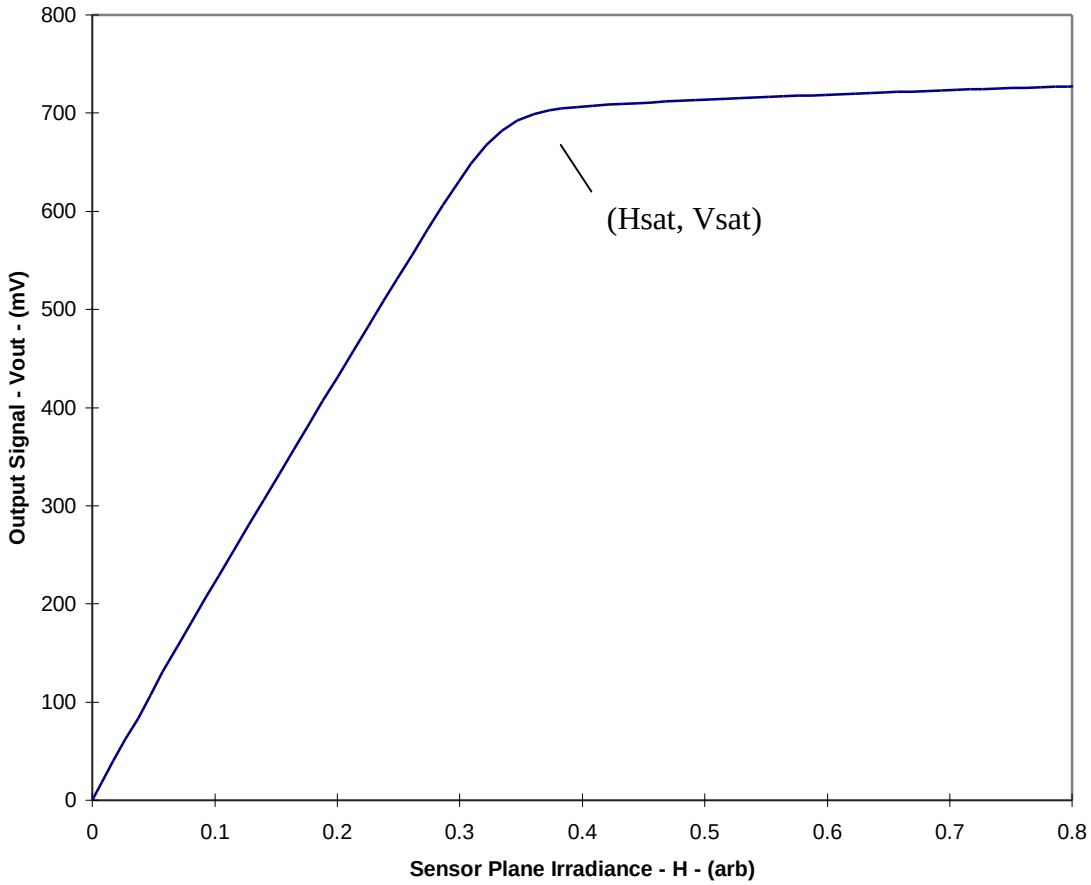


Figure 15 Typical KAI-0372 Series Photoresponse

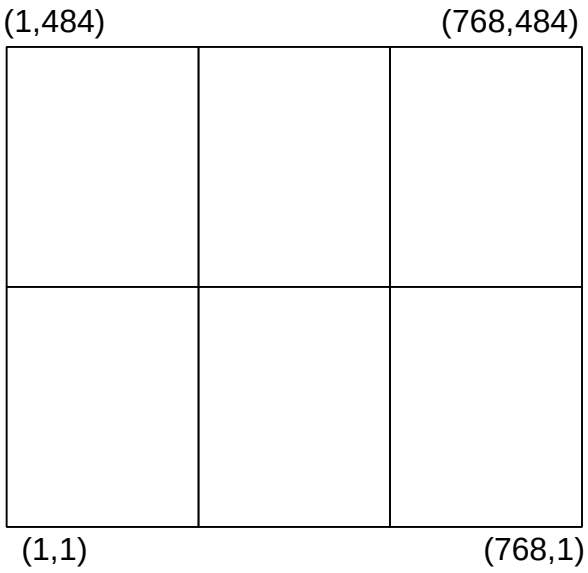
3.2 Defect Classification

All values derived under nominal operating conditions at 40°C operating temperature.

DEFECT TYPE	DEFECT DEFINITION	NUMBER ALLOWED	NOTES
Defective Pixel	Under uniform illumination with mean pixel output of 400mV, a defective pixel deviates by more than 15% from the mean value of all active pixels in its section.	5	1, 2, 3
Bright Defect	Under dark field conditions, a bright defect deviates more than 15 mV from the mean value of all pixels in its section.	0	1, 2, 3
Cluster Defect	Two or more vertically or horizontally adjacent defective pixels.	0	2, 3

Table 13 Defect Classification

Notes:
1. Sections are 256 (H) x 242 (V) pixel groups, which divide the imager into six equal areas as shown below.
2. For the color device, KAI-0372CM, a defective pixel deviates by more than 15% from the mean value of all active pixels in its section with the same color.
3. Test conditions: Junction temperature = 40°C, integration time = 33 msec and readout time = 33 msec.



4.1 Climatic Requirements

ITEM	DESCRIPTION	MIN.	MAX.	UNITS	CONDITIONS	NOTES
Operation to Specification	Temperature	+25	+40	^{o}C	@ 10%±5% RH	1, 2
	Humidity	10±5	86±5	%RH	@ 36±2^{o}C Temp.	1, 2
Operation Without Damage	Temperature	-25	+55	^{o}C	@ 10%±5% RH	2, 3
Storage	Temperature	-25	+70	^{o}C	@ 10%±5%RH	2, 4
	Humidity	-----	90±5	%RH	@ 49±2^{o}C Temp.	2, 4

Table 14 Climatic Requirements

Notes:
1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
3. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
4. The image sensor shall meet the specifications of this document after storage for 15 days at the specified conditions.

4.2 Quality and Reliability

4.2.1 Quality Strategy:
All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

4.2.2 Replacement:
All devices are warranted against failures in accordance with the Terms of Sale.

4.2.3 Cleanliness:
Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

4.2.4 ESD Precautions:
Devices are shipped in static-safe containers and should only be handled at static-safe workstations.

4.2.5 Reliability:
Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied upon request.

4.2.6 Test Data Retention:
Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

4.3 Ordering Information

See Appendix 1 for available part numbers.

Address all inquiries and purchase orders to:

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Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
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Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

Appendix 1

Part Number Availability

Note:
This appendix may be updated independently of the performance specification.
Contact Eastman Kodak Company for the latest revision.

Monochrome, Microlens, Sealed Glass

DEVICE NAME	AVAILABLE PART NUMBERS	FEATURES
KAI-0372M	2H4629	768(H) x 484(V) active pixel, progressive scan CCD with Microlens, Sealed clear glass
KAI-0372M	2H4630	768(H) x 484(V) active pixel, progressive scan CCD with Microlens, Sealed clear glass, Engineering Grade
KAI-0372M	2H4631	768(H) x 484(V) active pixel, progressive scan CCD with Microlens, Sealed clear glass, Mechanical Grade

Table 15 Part Numbers - Monochrome, Microlens, Sealed Glass

Monochrome, Microlens, Taped Glass

DEVICE NAME	AVAILABLE PART NUMBERS	FEATURES
KAI-0372M	2H4632	768(H) x 484(V) active pixel, progressive scan CCD with Microlens, Taped clear glass

Table 16 Part Numbers - Monochrome, Microlens, Taped Glass

Monochrome, Sealed Glass

DEVICE NAME	AVAILABLE PART NUMBERS	FEATURES
KAI-0372	2H4625	768(H) x 484(V) active pixel, progressive scan CCD, Sealed clear glass
KAI-0372	2H4626	768(H) x 484(V) active pixel, progressive scan CCD, Sealed clear glass, Engineering Grade
KAI-0372	2H4627	768(H) x 484(V) active pixel, progressive scan CCD, Sealed clear glass, Mechanical Grade

Table 17 Part Numbers - Monochrome, Sealed Glass

Monochrome, Taped Glass

DEVICE NAME	AVAILABLE PART NUMBERS	FEATURES
KAI-0372	2H4628	768(H) x 484(V) active pixel, progressive scan CCD, Taped clear glass

Table 18 Part Numbers - Monochrome, Taped Glass

Color, Microlens, Sealed Glass

DEVICE NAME	AVAILABLE PART NUMBERS	FEATURES
KAI-0372CM	2H4633	768(H) x 484(V) active pixel, progressive scan CCD with CFA and Microlens, Sealed clear glass
KAI-0372CM	2H4634	768(H) x 484(V) active pixel, progressive scan CCD with CFA and Microlens, Sealed clear glass, Engineering Grade
KAI-0372CM	2H4635	768(H) x 484(V) active pixel, progressive scan CCD with CFA and Microlens, Sealed clear glass, Mechanical Grade

Table 19 Part Numbers - Color, Microlens, Sealed Glass