DAQ

NI PCI-6110/6111
User Manual

Mulitfunction I/O Devices for PCI Bus Computers

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Worldwide Technical Support and Product Information

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Compliance

FCC/Canada Radio Frequency Interference Compliance*

Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.

Consult the FCC Web site at `fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity**, may cause interference to radio and television reception. Classification requirements are the same for the FCC and the Canadian DOC.

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

Readers in the European Union (EU) must refer to the Manufacturer's Declaration of Conformity (DoC) for information** pertaining to the CE Mark compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments PCI-6110/6111 data acquisition (DAQ) device and contains information concerning its operation and programming.

The device is a high-performance multifunction analog, digital, and timing I/O device for PCI bus computers. Supported functions include analog input (AI), analog output (AO), digital I/O (DIO), and timing I/O (TIO).

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 — This icon denotes a note, which alerts you to important information.

 — This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, see the *Unpacking* section of Chapter 1, *Introduction*, for precautions to take.

bold — Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

italic — Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

NI-DAQ	NI-DAQ refers to the NI-DAQ driver software for Macintosh or PC compatible computers unless otherwise noted.
NI PCI-6110/6111	This phrase refers to either the NI PCI-6110 or NI PCI-6111 device.
PCI	PCI stands for Peripheral Component Interconnect. PCI is a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA.
Platform	Text in this font denotes a specific platform and indicates that the text following it applies only to that platform.

National Instruments Documentation

The *NI PCI-6110/6111 User Manual* is one piece of the documentation set for the DAQ system. You could have any of several types of documentation depending on the hardware and software in the system. Refer to `ni.com/manuals` to download the following documents:

- Accessory installation guides or manuals—If you use accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you make the connections.
- DAQ hardware documentation—This documentation has detailed information about the DAQ hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specification information about the DAQ hardware, and application hints.
- Software documentation—You may have both application software and NI-DAQ documentation. NI application software includes LabVIEW, Measurement Studio, and others. After you set up the hardware system, use either the application software documentation or the NI-DAQ documentation to help you write your application. If you have a large, complicated system, it is worthwhile to look through the software documentation before you configure the hardware.

Related Documentation

The following documents contain information that you might find helpful:

- The NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals,* located at `ni.com/zone`
- *PCI Local Bus Specification Revision 2.2*
- *DAQ Quick Start Guide,* located at `ni.com/manuals`
- *DAQ-STC Technical Reference Manual,* located at `ni.com/manuals`
- *NI-DAQ User Manual for PC Compatibles,* located at `ni.com/manuals`
- *NI-DAQ Function Reference Manual* (for NI-DAQ versions 6.6 or earlier), located at `ni.com/manuals`
- *NI-DAQ Function Reference Help* (for NI-DAQ versions 6.7 or later), which is accessible from **Start»Programs»National Instruments» NI-DAQ»NI-DAQ Help**

1 Introduction

This chapter describes the NI PCI-6110/6111, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack the device.

About the NI PCI-6110/6111

Thank you for buying an NI PCI-6110/6111. The NI PCI-6110/6111 is a Plug and Play, multifunction analog, digital, and timing I/O device for PCI bus computers. The NI PCI-6110/6111 features a 12-bit A/D converter (ADC) per channel with four or two simultaneously sampling analog inputs, 16-bit D/A converters (DACs) with voltage outputs, eight lines of TTL-compatible DIO, and two 24-bit counter/timers for TIO. Because the NI PCI-6110/6111 has no DIP switches, jumpers, or potentiometers, it is easily software-configured and calibrated.

The NI PCI-6110/6111 is a completely switchless and jumperless DAQ device for the PCI bus. This feature is made possible by the NI MITE bus interface chip that connects the device to the PCI I/O bus. The MITE implements the PCI Local Bus Specification so that the interrupts and base memory addresses are all software configured.

The NI PCI-6110/6111 uses the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control AI, AO, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamless changes to the sampling rate.

The NI PCI-6110/6111 uses the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. The RTSI bus consists of the RTSI bus interface and a ribbon cable to route timing and trigger signals between several functions on as many as five DAQ devices in the computer.

Detailed specifications of the NI PCI-6110/6111 are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use the NI PCI-6110/6111, you will need the following items:

- ❑ NI PCI-6110/6111
- ❑ *NI PCI-6110/6111 User Manual*
- ❑ NI-DAQ
- ❑ The computer
- ❑ Optional: One of the following software packages and documentation:
  - LabVIEW **(Windows or Mac OS)**
  - Measurement Studio **(Windows)**
  - VI Logger **(Windows)**

Software Programming Choices

When programming the National Instruments DAQ hardware, you can use NI application development environment (ADE) software or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which ships with the NI PCI-6110/6111, has an extensive library of functions that you can call from the ADE. These functions allow you to use all the features of the NI PCI-6110/6111.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to the code. Whether you use LabVIEW, Measurement Studio, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

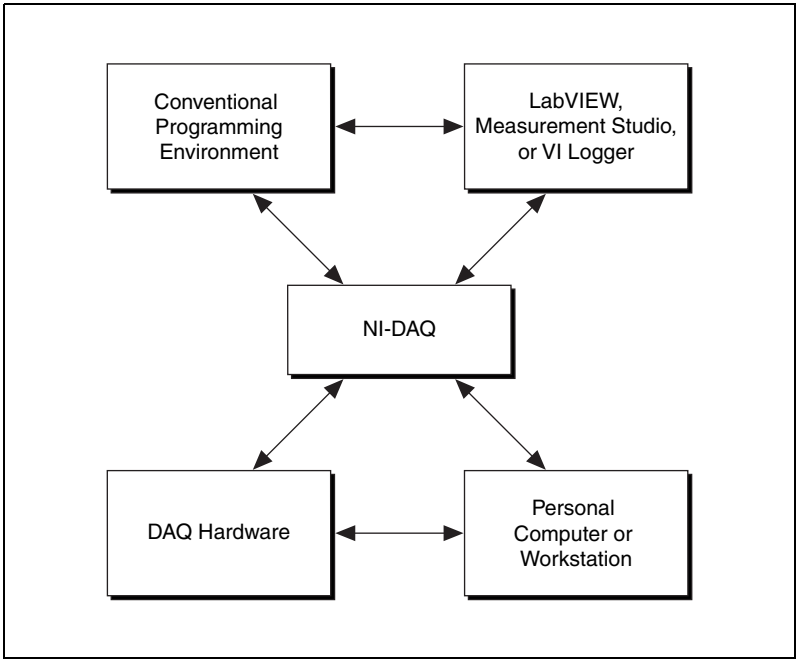


Figure 1-1. The Relationship Between the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows/CVI, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++

developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries, ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

VI Logger is an easy-to-use yet flexible tool specifically designed for data logging applications. Using dialog windows, you can configure data logging tasks to easily acquire, log, view, and share your data. VI Logger does not require any programming; it is a stand-alone, configuration-based software.

Using LabVIEW, Measurement Studio, or VI Logger greatly reduces the development time for your data acquisition and control application.

Optional Equipment

NI offers a variety of products to use with the NI PCI-6110/6111, including the following cables, connector blocks, and other accessories:

- Shielded cables and cable assemblies
- Connector blocks, shielded 50- and 68-pin screw terminals
- RTSI bus cables

For more specific information about these products, refer to the NI catalog at `ni.com/catalog`.

Custom Cabling

NI offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

When developing custom cabling, refer to the following guidelines:

- For the AI signals, shielded twisted-pair wires for each AI pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

The following list gives recommended part numbers for connectors that mate to the I/O connector on the NI PCI-6110/6111:

- Honda 68-position, solder cup, female connector
- Honda backshell

Unpacking

The NI PCI-6110/6111 is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge (ESD) can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the computer.

Store the NI PCI-6110/6111 in the antistatic envelope when not in use.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. Operate the product only at or below the pollution degree stated in the Appendix A, *Specifications*. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

Clean the product with a soft nonmetallic brush. Make sure that the product is completely dry and free from contaminants before returning it to service.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate this product only at or below the installation category stated in Appendix A, *Specifications*.

The following is a description of installation categories:

- Installation category I is for measurements performed on circuits not directly connected to MAINS[1]. This category is a signal level such as voltages on a printed wire board (PWB) on the secondary of an isolation transformer.

  Examples of installation category I are measurements on circuits not derived from MAINS and specially protected (internal) MAINS-derived circuits.

- Installation category II is for measurements performed on circuits directly connected to the low-voltage installation. This category refers to local-level distribution such as that provided by a standard wall outlet.

[1] MAINS is defined as the electricity supply system to which the equipment concerned is designed to be connected either for powering the equipment or for measurement purposes.

Examples of installation category II are measurements on household appliances, portable tools, and similar equipment.

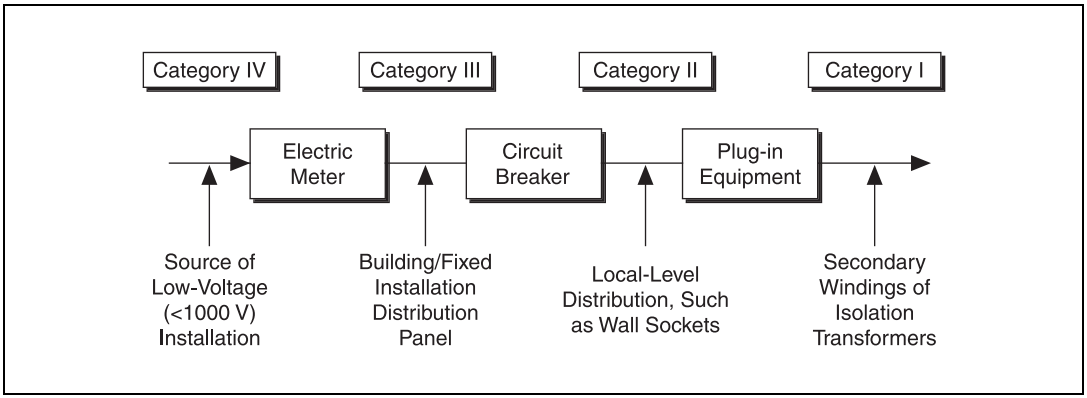
- Installation category III is for measurements performed in the building installation. This category is a distribution level referring to hardwired equipment that does not rely on standard building insulation.

  Examples of installation category III include measurements on distribution circuits and circuit breakers. Other examples of installation category III are wiring including cables, bus-bars, junction boxes, switches, socket outlets in the building/fixed installation, and equipment for industrial use, such as stationary motors with a permanent connection to the building/fixed installation.

- Installation category IV is for measurements performed at the source of the low-voltage (<1,000 V) installation.

  Examples of category IV are electric meters, and measurements on primary overcurrent protection devices and ripple-control units.

Below is a diagram of a sample installation.



2

Installing and Configuring the NI PCI-6110/6111

This chapter explains how to install and configure the NI PCI-6110/6111.

Installing the Software

Note It is important to install the software before installing the NI PCI-6110/6111 to ensure that the device is properly detected.

1. Install the ADE, such as LabVIEW or Measurement Studio, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and in the *DAQ Quick Start Guide* included with the device.

Installing the Hardware

The following are general installation instructions. Consult the computer or chassis user manual or technical reference manual for specific instructions and warnings about installing new devices.

You can install the NI PCI-6110/6111 in any available expansion slot in the computer. However, to achieve best noise performance, leave as much room as possible between the NI PCI-6110/6111 and other devices and hardware.

1. Power off and unplug the computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
5. Insert the NI PCI-6110/6111 into a PCI system slot. Gently rock the device to ease it into place. It may be a tight fit, but do *not* force the device into place.

6. If required, screw the mounting bracket of the NI PCI-6110/6111 to the back panel rail of the computer.
7. Visually verify the installation by making sure the device is not touching other devices or components and is fully inserted into the slot.
8. Replace the cover.
9. Plug in and power on the computer.

The NI PCI-6110/6111 is now installed. You are now ready to configure the device. Refer to the software documentation for configuration instructions.

Configuring the Device

The NI standard architecture for data acquisition and the PCI bus specification make the NI PCI-6110/6111 completely software configurable. You must perform two types of configuration on the NI PCI-6110/6111—bus-related and data acquisition-related configuration.

The NI PCI-6110/6111 is fully compatible with the industry standard *PCI Local Bus Specification Revision 2.2*. This allows the PCI system to automatically perform all bus-related configurations. Bus-related configuration includes setting the device base memory address and interrupt channel.

Data acquisition-related configuration, which you must perform, includes such settings as AI coupling and range, and others. You can modify these settings using NI-DAQ or application level software, such as LabVIEW, Measurement Studio, and VI Logger.

To configure the device using Measurement and Automation Explorer (MAX), refer to either the *DAQ Quick Start Guide* or to the *NI-DAQ User Manual for PC Compatibles*. For operating system-specific installation and troubleshooting instructions, refer to `ni.com/support/daq`.

3

Hardware Overview

This chapter presents an overview of the hardware functions on the NI PCI-6110/6111. Figures 3-1 and 3-2 show block diagrams for the NI PCI-6110 and the NI PCI-6111, respectively.

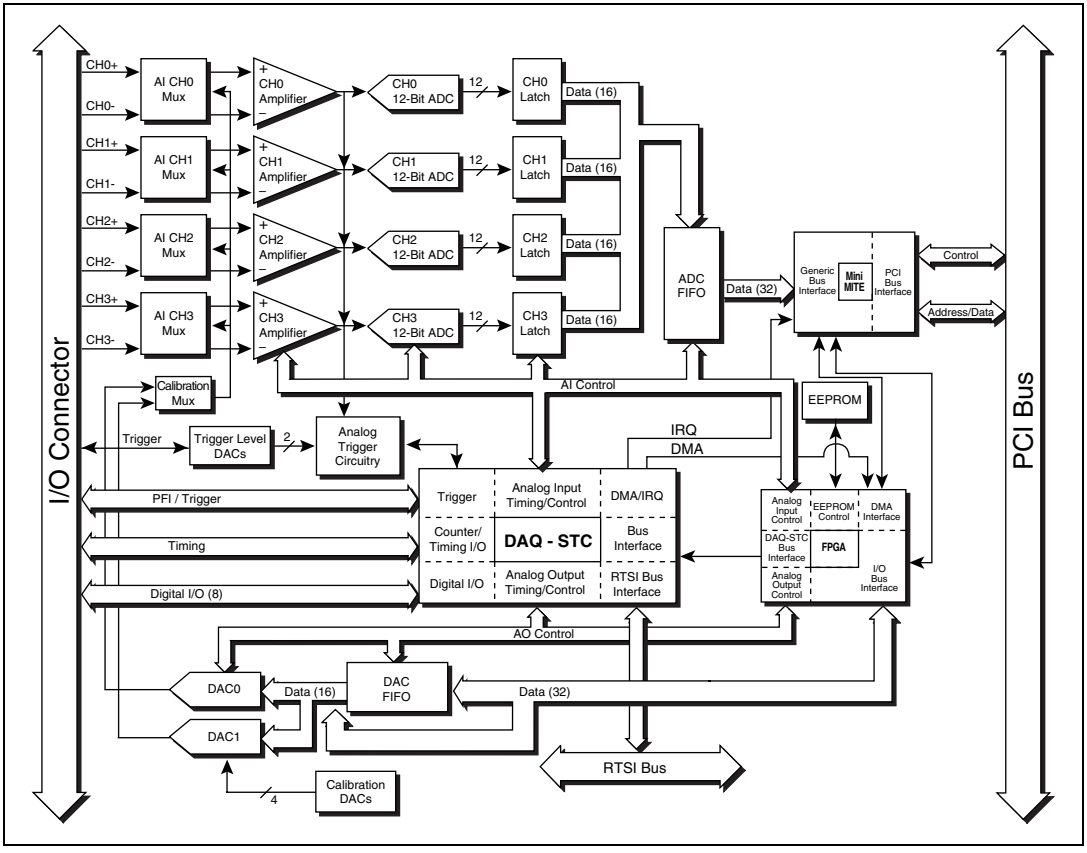


Figure 3-1. NI PCI-6110 Block Diagram

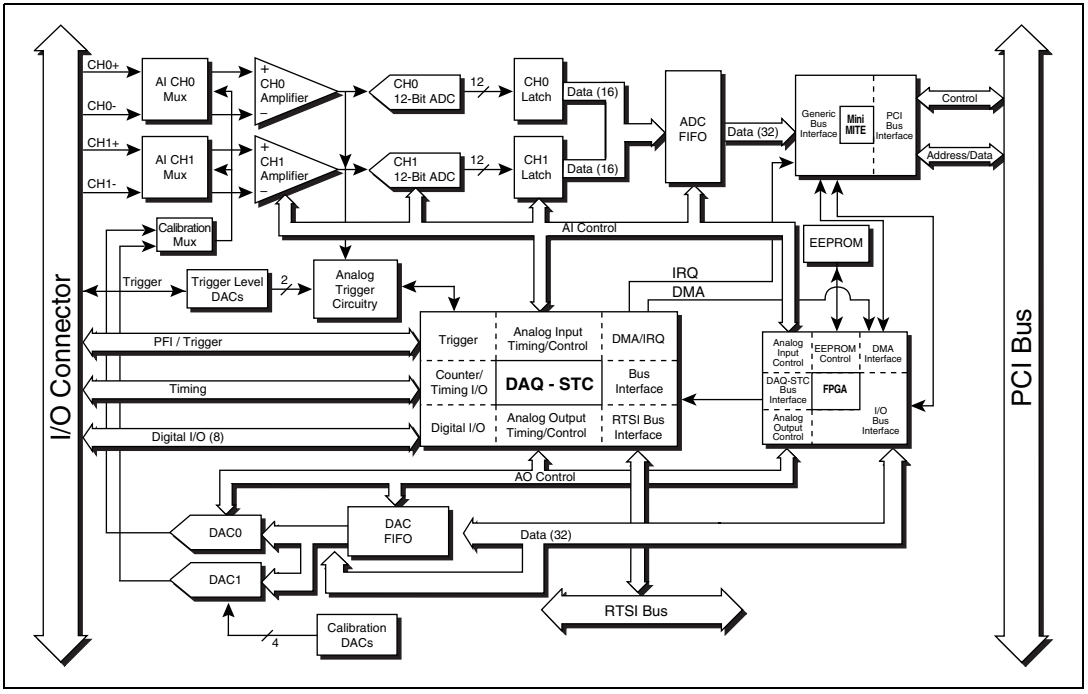


Figure 3-2. NI PCI-6111 Block Diagram

Analog Input

The AI section for the NI PCI-6110/6111 is software configurable. You can select different AI configurations through application software. The following sections describe in detail each AI setting.

Input Mode

The NI PCI-6110/6111 supports only differential (DIFF) inputs. DIFF input mode provides up to four channels on the NI PCI-6110 and up to two channels on the NI PCI-6111.

Note The inputs are differential only in the sense that the ground loops are broken. The negative input is not intended to carry signals of interest, rather it provides a DC reference point for the positive input, which may be different than ground.

A channel configured in DIFF input mode uses two AI channel lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative

input of the PGIA. For more information about DIFF input mode, refer to the *Connecting Analog Input Signals* section of Chapter 4, *Connecting Signals*, which contains diagrams showing the signal paths for DIFF input mode.

Input Polarity and Input Range

The NI PCI-6110/6111 has bipolar inputs only. Bipolar input means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. These devices have a bipolar input range of 20 V (±10 V).

You can program range settings on a per channel basis so that you can uniquely configure each AI channel.

The software-programmable gain on these devices increases flexibility by matching the input signal ranges to those that the ADC can accommodate. The NI PCI-6110/6111 has gains of 0.2, 0.5, 1, 2, 5, 10, 20, and 50, and it is suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-1 shows the overall input range and precision according to the chosen gain.

Table 3-1. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range[1]	Precision[2]
–10 to +10 V	0.2	–50 to +50 V	24.41 mV
	0.5	–20 to +20 V	9.77 mV
	1.0	–10 to +10 V	4.88 mV
	2.0	–5 to +5 V	2.44 mV
	5.0	–2 to +2 V	976.56 µV
	10.0	–1 to +1 V	488.28 µV
	20.0	–500 to +500 mV	244.14 µV
	50.0	–200 to +200 mV	97.66 µV

[1] **Caution:** The NI PCI-6110/6111 is *not* designed for input voltages greater than 42 V, even if a user-installed voltage divider reduces the voltage to within the input range of the device. Input voltages greater than 42 V can damage the NI PCI-6110/6111, any device connected to it, and the host computer. Overvoltage can also cause an electric shock hazard for the operator. NI is *not* liable for damage or injury resulting from such misuse.

[2] The value of 1 least significant bit (LSB) of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

The range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, match the input range as closely as possible to the expected range of the input signal.

Input Coupling

You can configure the NI PCI-6110/6111 for either AC or DC input coupling on a per channel basis. Use AC coupling when the AC signal contains a large DC component. If you enable AC coupling, you remove the large DC offset for the input amplifier and amplify only the AC component. This configuration makes effective use of the ADC dynamic range.

Analog Output

The NI PCI-6110/6111 supplies two channels of AO voltage at the I/O connector. The range is fixed at bipolar ±10 V.

Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a DAQ sequence, these devices also support analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA on any of the channels, as shown in Figures 3-3 and 3-4. The trigger-level range for the direct analog channel is ±10 V in 78 mV steps for the NI PCI-6110/6111. The range for the post-PGIA trigger selection is simply the full-scale range of the selected channel, and the resolution is that range divided by 256.

Note PFI0/TRIG1 pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, which can result in false triggering when the pin is unconnected. To avoid false triggering, make sure this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input using software.

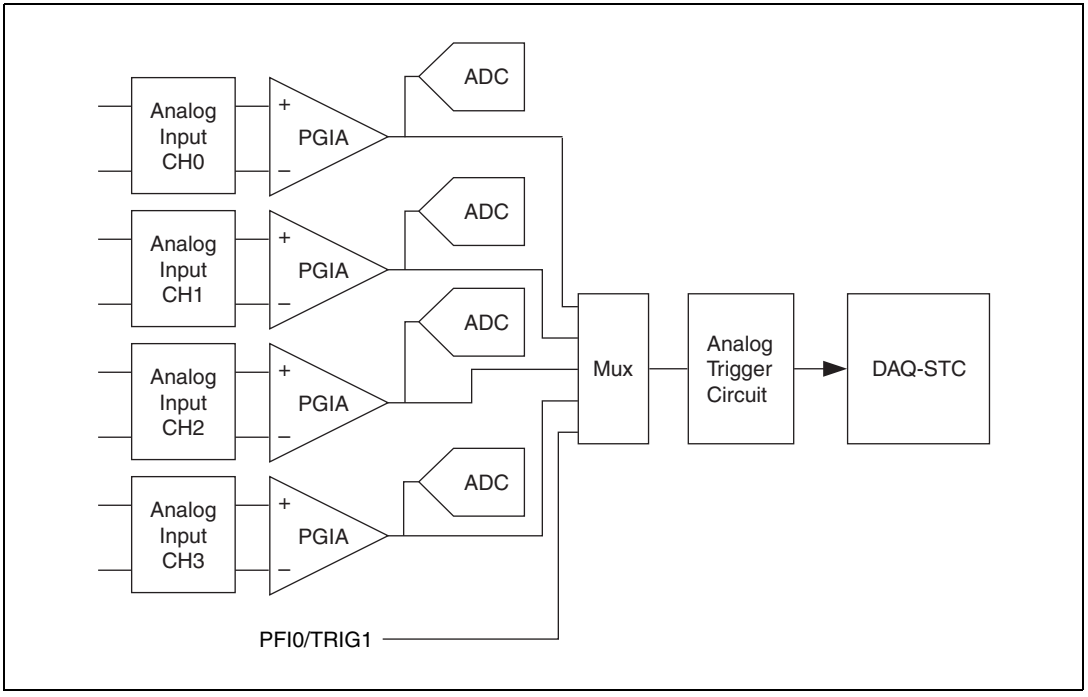


Figure 3-3. Analog Trigger Block Diagram for the NI PCI-6110

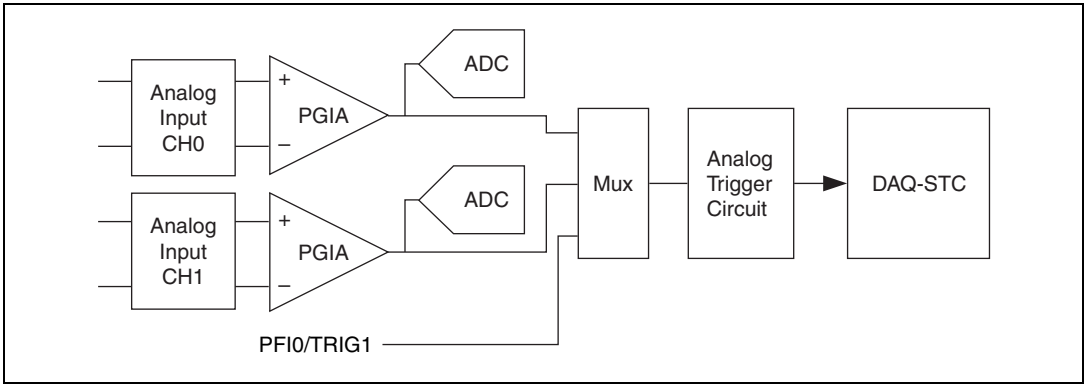


Figure 3-4. Analog Trigger Block Diagram for the NI PCI-6111

Five analog triggering modes are available, as shown in Figures 3-5 through 3-9. You can independently set **lowValue** and **highValue** in software.

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, as shown in Figure 3-5. **HighValue** is unused.

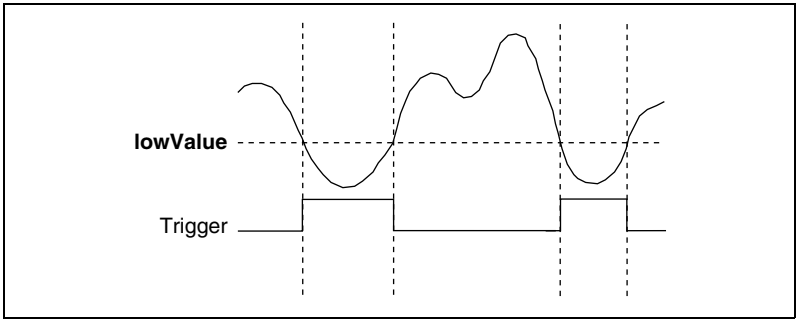


Figure 3-5. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, as shown in Figure 3-6. **LowValue** is unused.

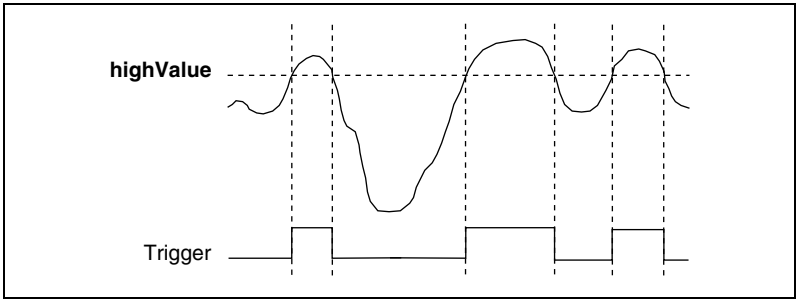


Figure 3-6. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between the **lowValue** and the **highValue**, as shown in Figure 3-7.

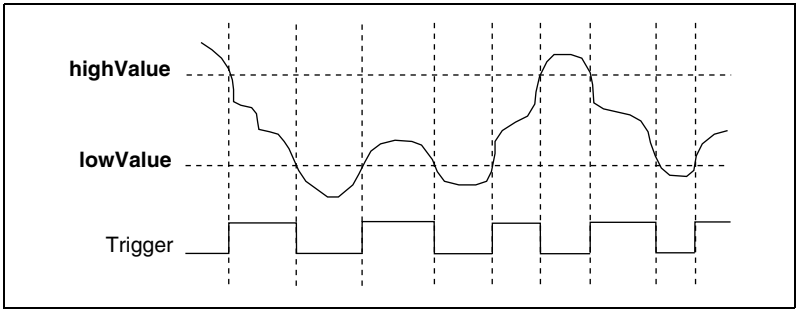


Figure 3-7. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**, as shown in Figure 3-8.

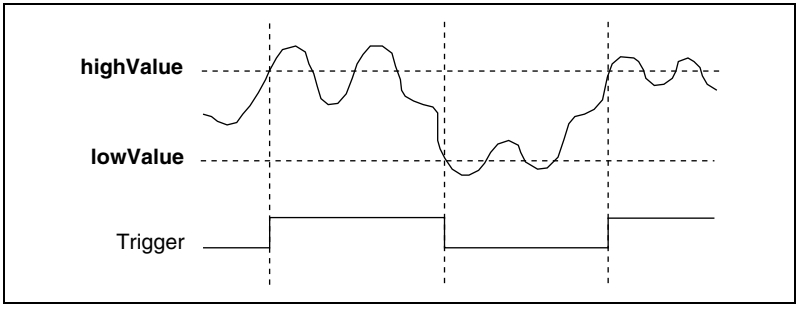


Figure 3-8. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue**, as shown in Figure 3-9.

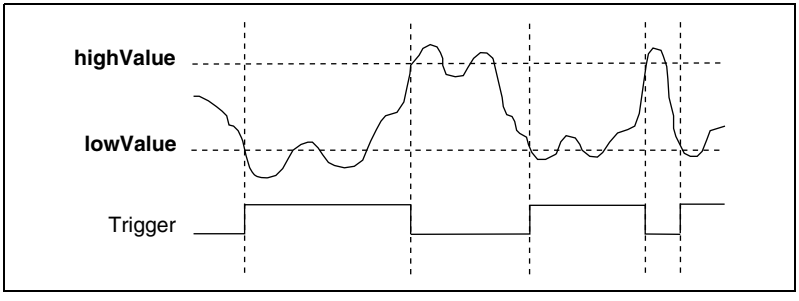


Figure 3-9. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the AI signal and user-defined trigger levels. This digital trigger can be used by any DAQ-STC timing section, including the AI, AO, and general-purpose counter/timer sections. For example, the AI section can be configured to acquire *n* scans after the AI signal crosses a specific threshold. As another example, the AO section can be configured to update its outputs whenever the AI signal crosses a specific threshold.

Digital I/O

The NI PCI-6110/6111 contains eight lines of DIO for general-purpose use. You can individually software-configure each line for either input or output. At system startup and reset, the DIO ports are all high-impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control those counters. The up/down control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The NI PCI-6110/6111 uses the RTSI bus to connect timing signals between devices and the Programmable Function Input (PFI) pins on the I/O connector to external circuitry. These connections enable the NI PCI-6110/6111 to both control and be controlled by other devices and circuits.

You can control 13 timing signals internal to the DAQ-STC with an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the STARTSCAN signal is shown in Figure 3-10.

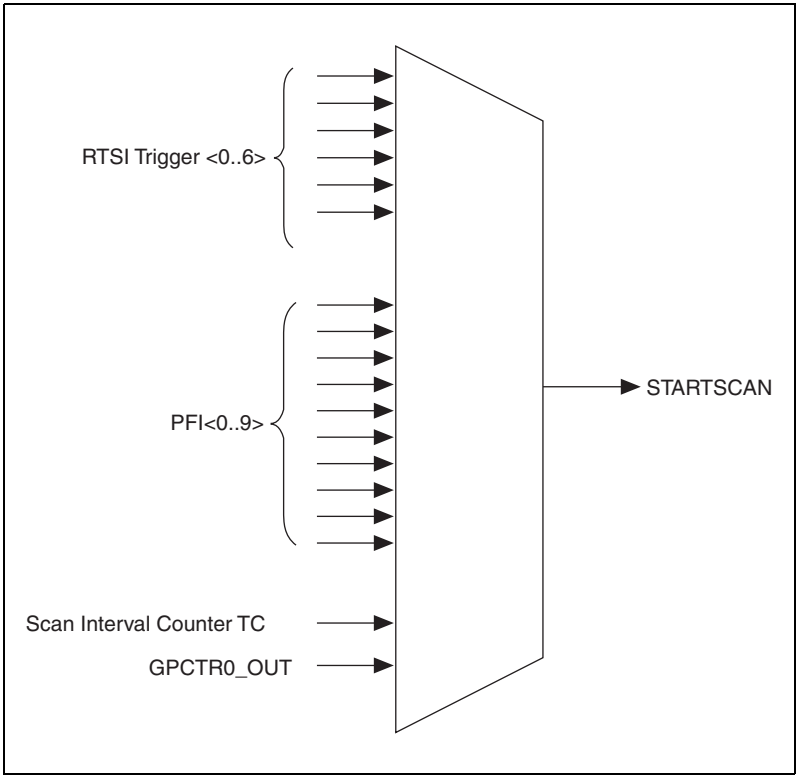


Figure 3-10. STARTSCAN Signal Routing

This figure shows that STARTSCAN can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section, and on the PFI pins, as indicated in Chapter 4, *Connecting Signals*.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select a PFI as the external source for a given timing signal. Any PFI can be used as an input by any timing signal, and multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can also individually enable each PFI pin to output a specific internal timing signal. For example, if you need

the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

Many functions performed by the NI PCI-6110/6111 require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

The NI PCI-6110/6111 can use either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the device to use the internal timebase, you can program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the device as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. This timebase is software-selectable.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for the device sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-11.

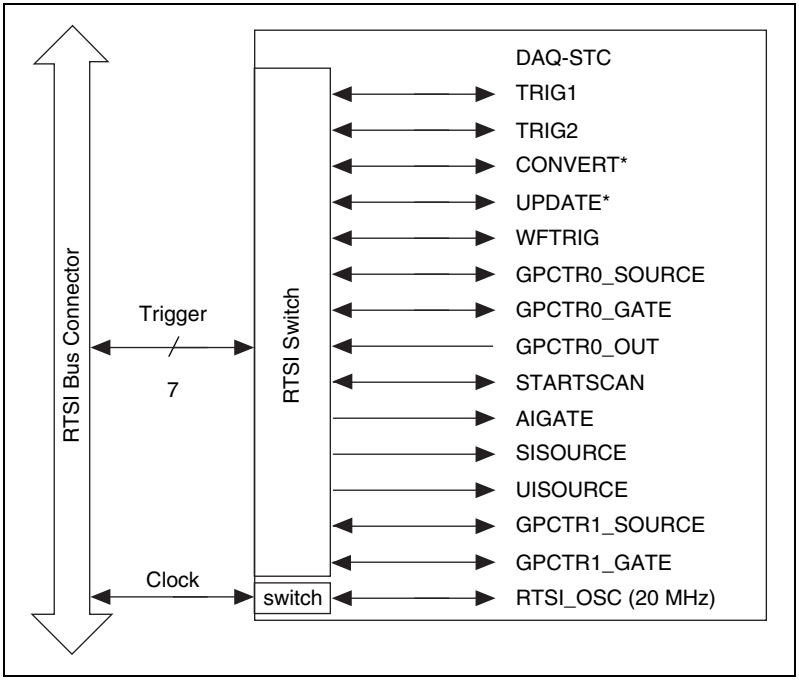


Figure 3-11. RTSI Bus Signal Connection

Refer to the *Timing Connections* section of Chapter 4, *Connecting Signals*, for a description of the signals shown in Figure 3-11.

4

Connecting Signals

This chapter describes how to make input and output signal connections to the NI PCI-6110/6111 through the device I/O connector. Table 4-1 shows the cables that can be used with the I/O connectors to connect to different accessories.

Table 4-1. I/O Connector Details

Device with I/O Connector	Number of Pins	Cable for Connecting to 100-Pin Accessories	Cable for Connecting to 68-Pin Accessories	Cable for Connecting to 50-Pin Accessories
NI PCI-6110, NI PCI-6111	68	N/A	SH68-68EP, SH68-68R1-EP	SH6850

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the NI PCI-6110/6111. A signal description follows the connector pinouts. Figure 4-2 shows the pin assignments for the NI PCI-6110/6111 when used with a 50-pin accessory.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PCI-6110/6111 can damage the device and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table 4-3. NI is *not* liable for any damage resulting from such signal connections.

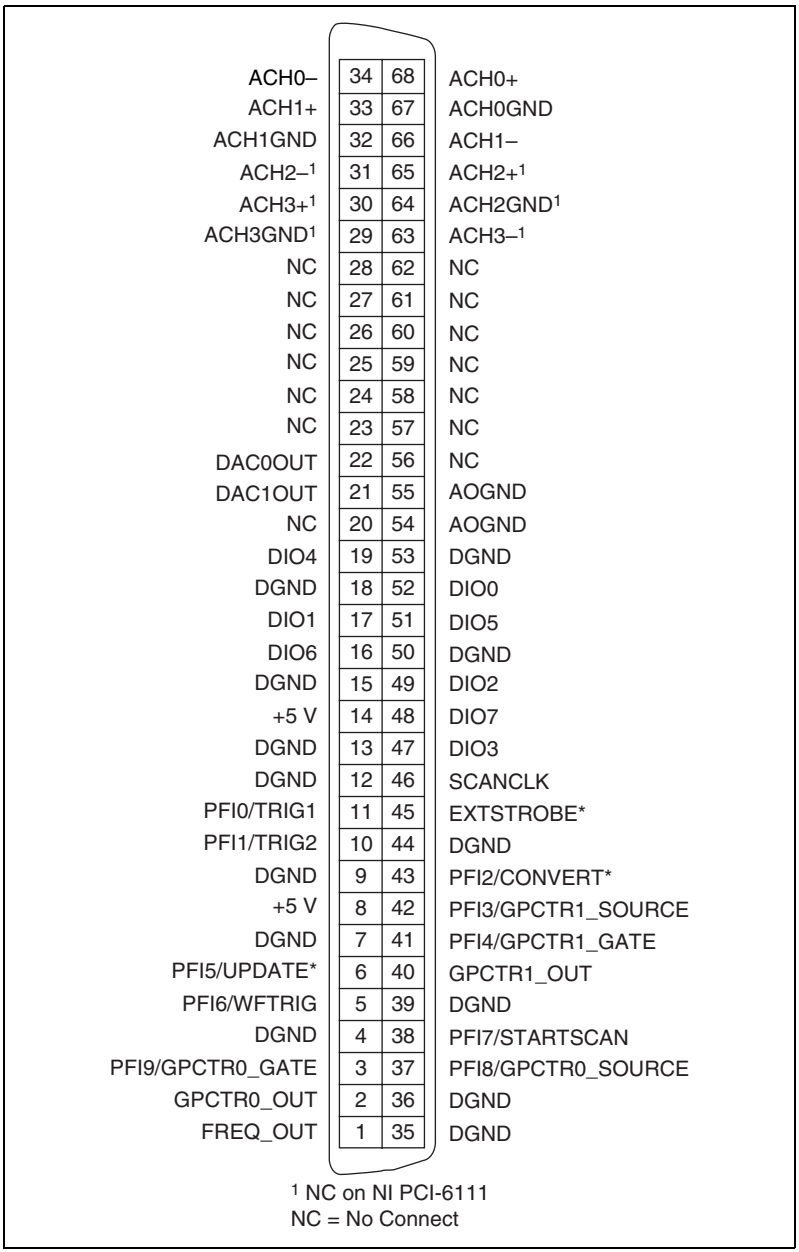


Figure 4-1. 68-Pin I/O Connector Pin Assignment for the NI PCI-6110/6111

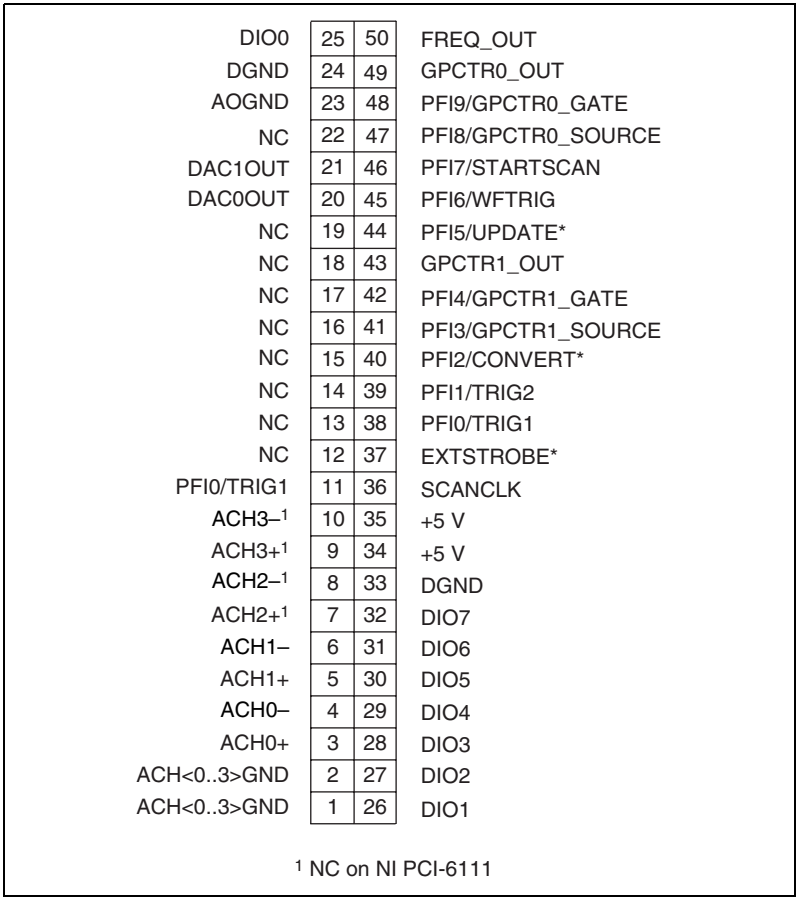


Figure 4-2. 50-Pin Connector Pin Assignments for the NI PCI-6110/6111

I/O Connector Signal Descriptions

Table 4-2. Signal Descriptions for I/O Connector Pins

Signal Name	Reference	Direction	Description
ACH<0..3>GND	—	—	Analog Input Channels 0 through 3 ground—These pins are the bias current return point for differential measurements. ACH<2..3>GND signals are no connects on the NI PCI-6111.
ACH<0..3>+	ACH<0..3>GND	Input	Analog Input Channels 0 through 3 (+)—These pins are routed to the (+) terminal of the respective channel amplifier. ACH<2..3>+ signals are no connects on the NI PCI-6111.

Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
ACH<0..3>–	ACH<0..3>GND	Input	Analog Input Channels 0 through 3 (–)—These pins are routed to the (–) terminal of the respective channel amplifier. ACH<2..3>– signals are no connects on the NI PCI-6111.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of AO channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of AO channel 1.
AOGND	—	—	Analog Output Ground—The AO voltages are referenced to this node.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input Output	PFI0/Trigger 1—As an input, this is either a PFI or the source for the hardware analog trigger. PFI signals are explained in the *Timing Connections* section. Refer to the *Analog Trigger* section of Chapter 3, *Hardware Overview*, for more information about the hardware analog trigger. As an output, this is the TRIG1 signal. In posttrigger DAQ sequences, a low-to-high transition indicates the initiation of the DAQ sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input Output	PFI1/Trigger 2—As an input, this is a PFI. As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.

Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is a PFI.
		Output	As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is a PFI.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is a PFI.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is a PFI.
		Output	As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the AO primary group is being updated.
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is a PFI.
		Output	As an output, this is the WFTRIG signal. In timed AO sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is a PFI.
		Output	As an output, this is the STARTSCAN signal. This pin pulses once at the start of each AI scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is a PFI.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is a PFI.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.

Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-3. I/O Signal Summary for the NI PCI-6110/6111

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..3>+	AI	1 MΩ in parallel with 100 pF[1] 1 MΩ in parallel with 10 pF[2]	42 V	—	—	—	—
ACH<0..3>–	AI	10 nF	42 V	—	—	—	±200 pA
ACH<0..3>GND	AI	—	—	—	—	—	—
DAC0OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at –10	300 V/µs	—
DAC1OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at –10	300 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1 A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	AI/DIO	10 kΩ	±35 V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	9 kΩ pu and 10 kΩ pd
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-3. I/O Signal Summary for the NI PCI-6110/6111 (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

[1] Applies to gain ≤ 1, impedance refers to ACH<0..3>–
[2] Applies to gain > 1, impedance refers to ACH<0..3>–

AI/DIO = Analog Input/Digital I/O, DO = Digital Output, pd = pull-down, pu = pull-up

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual value may range between 17 and 100 kΩ.

Connecting Analog Input Signals

The NI PCI-6110/6111 channels are configured as pseudodifferential inputs. The input signal of each channel, ACH<0..3>+, is tied to the positive input of the PGIA, and each reference signal ACH<0..3>–, is tied to the negative input of the PGIA. The inputs are differential only in the sense that ground loops are broken. The reference signal, ACH<0..3>–, is not intended to carry signals of interest but only to provide a DC reference point for ACH<0..3>+ that may be different from ground.

Pseudodifferential signal connections reduce noise pickup and increase common-mode noise rejection. This connection type also allows input signals to float within the common-mode limits of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-3.

You can use the PGIA in different ways when using different input configurations. Figure 4-3 shows a diagram of the PGIA.

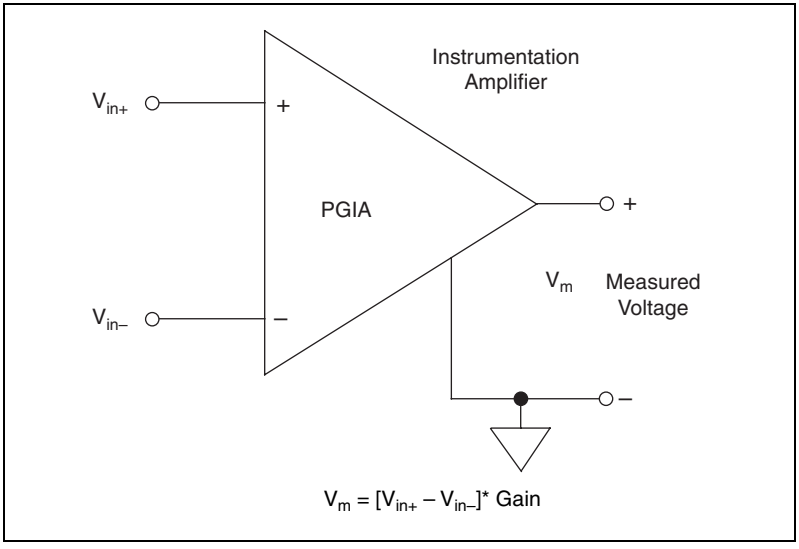


Figure 4-3. NI PCI-6110/6111 PGIA

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the AI signals connected to the NI PCI-6110/6111. Signals are routed to the positive and negative inputs of the PGIA. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the device ground. The ADC measures this output voltage when it performs A/D conversions.

Types of Signal Sources

When making signal connections, first determine whether the signal sources are floating or ground-referenced. The following sections describe these two signal types.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to the NI PCI-6110/6111 AI ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the NI PCI-6110/6111, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

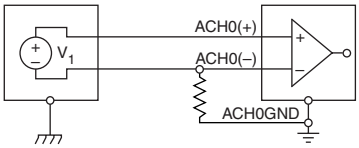
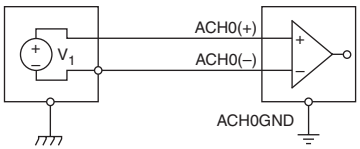
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Differential Measurements

The following sections discuss the use of differential (DIFF) measurements and considerations for measuring both floating and ground-referenced signal sources.

Table 4-4 summarizes the recommended DIFF signal connections and includes input examples for both types of signal sources.

Table 4-4. Signal Source Types

DIFF Input Examples and Signal Source	Floating Signal Source (Not Connected to Building Ground)	Grounded Signal Source
Input Examples	• Ungrounded thermocouples • Signal conditioning with isolated outputs • Battery devices	• Plug-in cards with nonisolated outputs
Differential (DIFF)	 See text for information on bias resistors.	

Differential Connection Considerations

A differential connection is one in which the NI PCI-6110/6111 AI signal has its own reference signal or signal return path. The device channels are always configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

Each differential signal uses two inputs—one for the signal and one for its reference signal.

Differential signal connections reduce noise pickup and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-4 shows how to connect a ground-referenced signal source to a channel on the NI PCI-6110/6111.

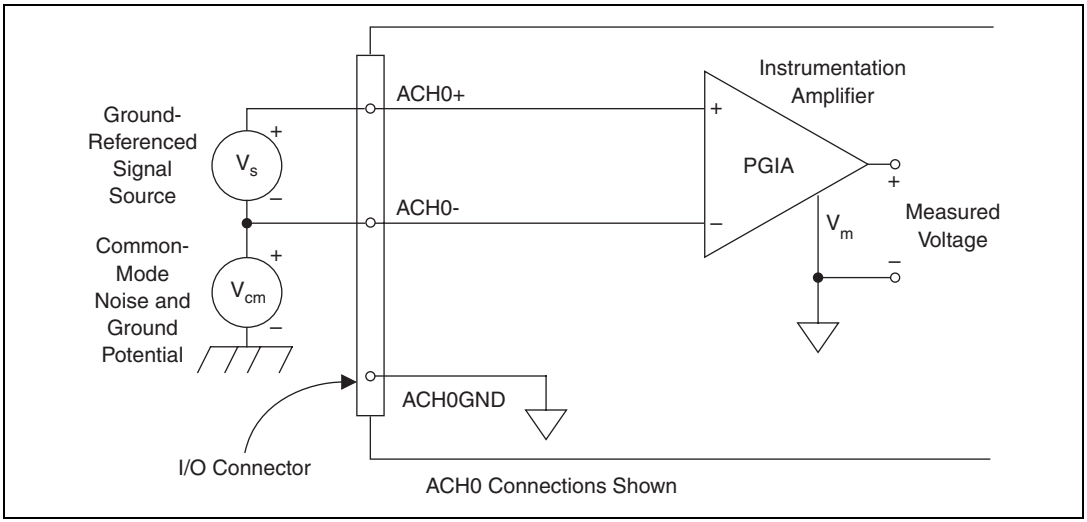


Figure 4-4. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in Figure 4-4.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-5 shows how to connect a floating signal source to a channel on the NI PCI-6110/6111.

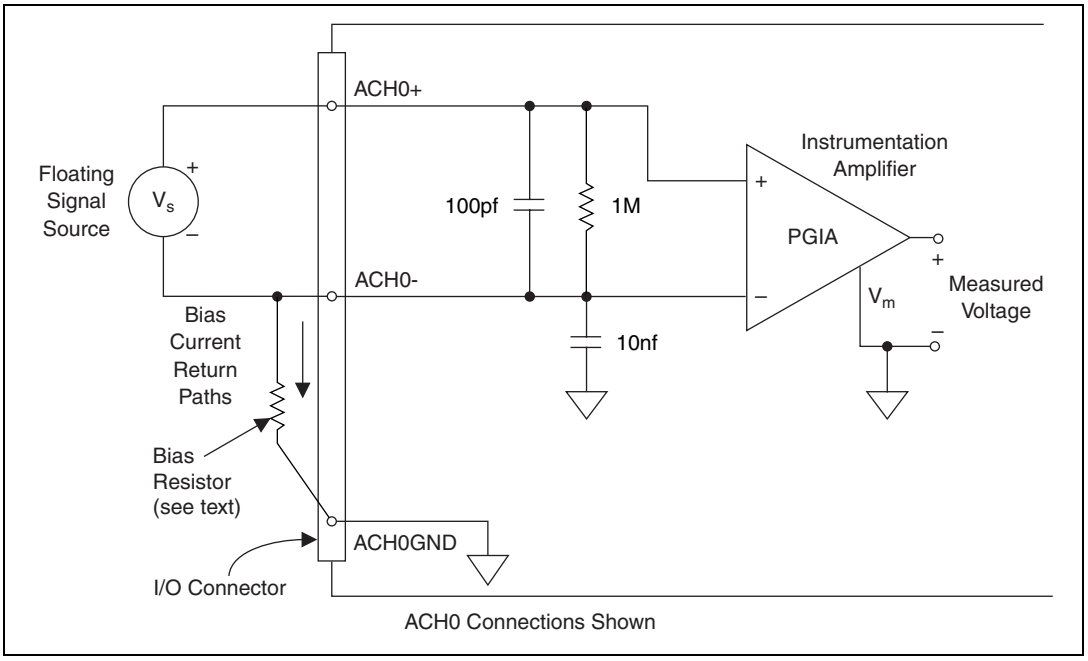


Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows a bias resistor connected between ACH0– and the floating signal source ground. If you do not use the resistor and the source is truly floating, the source often floats outside the common-mode signal range of the PGIA, and the PGIA saturates, causing erroneous readings. You must reference the source to the respective channel ground.

Common-Mode Signal Rejection Considerations

Figure 4-4 shows connections for signal sources that are already referenced to some ground point with respect to the NI PCI-6110/6111. In theory, the PGIA can reject any voltage caused by ground-potential differences between the signal source and the device. In addition, with pseudodifferential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device.

Like any amplifier, the common-mode rejection ratio (CMRR) of the PGIA is limited at high frequency. This limitation has been compensated for in the design of the NI PCI-6110/6111 by using a common-mode choke on each channel. The purpose of the 10 nF capacitance on the ACH<0..3>– connection is to provide an impedance for this choke to work against at high frequency, thus improving the high-frequency CMRR.

Depending upon your application and the type of common noise at your source, further common-noise rejection might be gained by placing a 0.1 µF ceramic bypass capacitor between ACH<0..3> and ACH<0..3>GND.

Working Voltage Range

The PGIA operates normally by amplifying signals of interest while rejecting common-mode signals as long as the following three conditions are met:

1. The common-mode voltage (V_{cm}), which is equivalent to subtracting ACH<0..3>GND from ACH<0..3>– and which is shown in Figure 4-5, must be less than ±11 V. This V_{cm} is a constant for all range selections.
2. The signal voltage (V_s), which is equivalent to subtracting ACH<0..3>– from ACH<0..3>+ and which is shown in Figure 4-5, must be less than or equal to the range selection of the given channel. If V_s is greater than the range selected, the signal clips and information is lost.
3. The total working voltage of the positive input, which can be thought of as ($V_{cm} + V_s$) or simply as subtracting ACH<0..3>GND from ACH<0..3>+, must be less than ±11 V for ranges ≤ ±10 V or less than ±42 V for ranges > ±10 V.

If any of these conditions are exceeded, current limiters limit the input current to 20 mA maximum into any input until the fault condition is removed.

Note All inputs are protected at up to ±42 V.

Analog Output Signal Connections

The AO signals are DAC0OUT, DAC1OUT, and AOGND.

DAC0OUT is the voltage output signal for AO channel 0, DAC1OUT is the voltage output signal for AO channel 1, and AOGND is the ground reference signal for the AO channels.

Figure 4-6 shows how to make AO connections to the NI PCI-6110/6111.

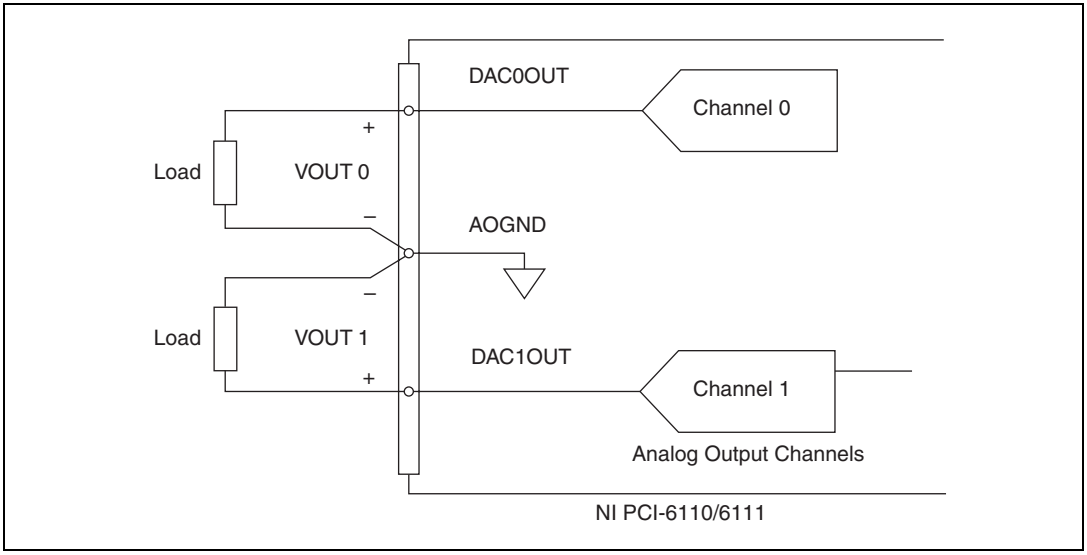


Figure 4-6. Analog Output Connections

Digital I/O Signal Connections

The DIO signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the NI PCI-6110/6111 and the computer. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-7 shows signal connections for three typical DIO applications.

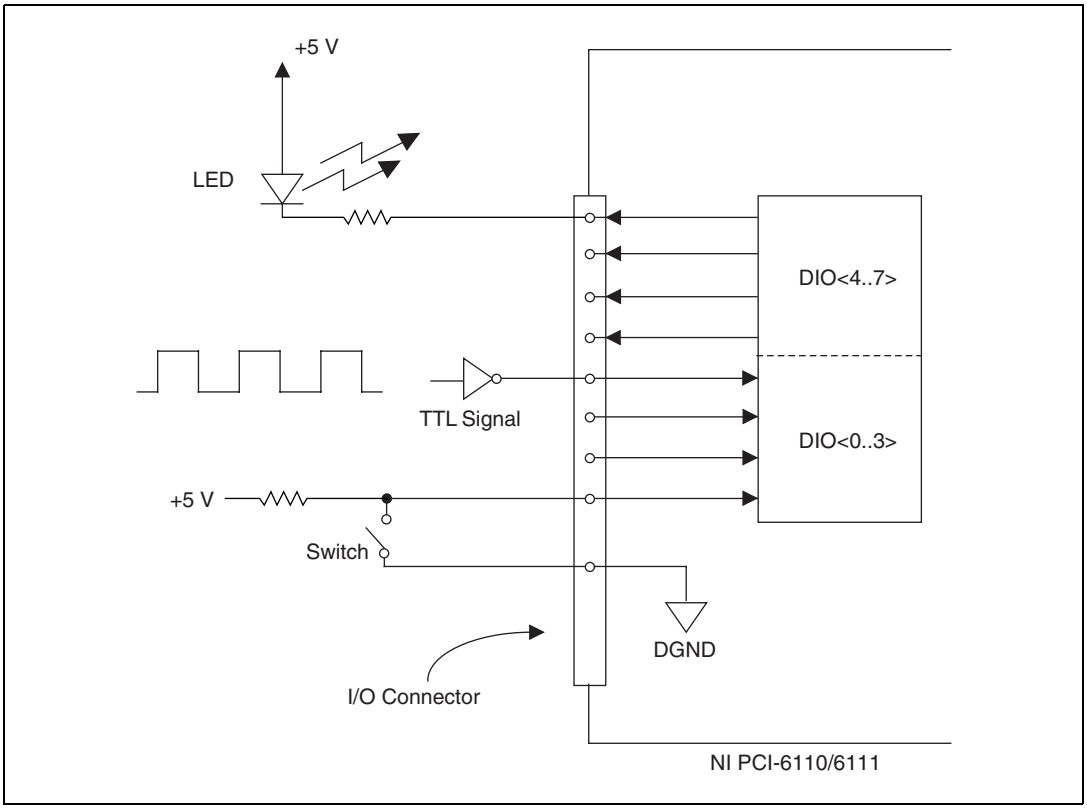


Figure 4-7. Digital I/O Connections

Figure 4-7 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the switch state shown in Figure 4-7. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in Figure 4-7.

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply using a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry.

Power rating +4.65 to +5.25 VDC at 1 A

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the NI PCI-6110/6111 or any other device. Doing so can damage the device and the computer. NI is *not* liable for damage resulting from such a connection.

Timing Connections

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the NI PCI-6110/6111 and the computer. NI is *not* liable for any damage resulting from such signal connections.

All external control over the timing of the NI PCI-6110/6111 is routed through the 10 PFIs, labeled PFI0 through PFI9. These signals are explained in the next section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The DAQ signals are explained in the *DAQ Timing Connections* section. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section.

All digital timing connections are referenced to DGND. Figure 4-8 illustrates how to connect an external TRIG1 source and an external CONVERT* source to two NI PCI-6110/6111 PFI pins.

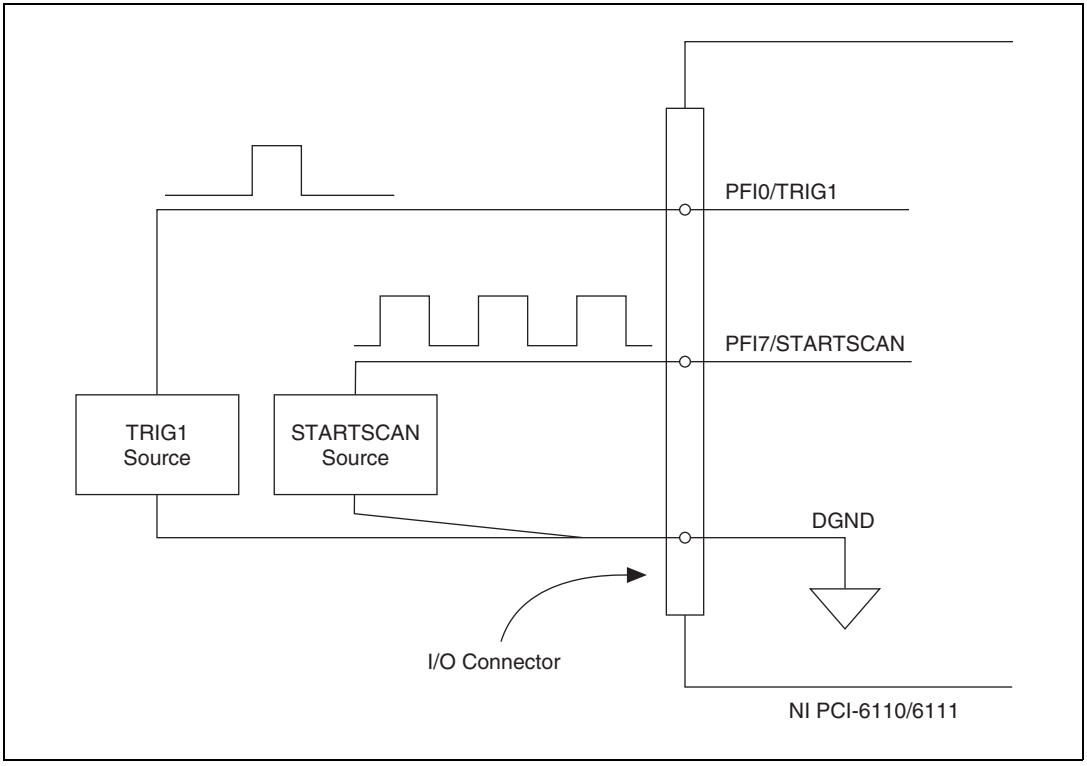


Figure 4-8. Timing I/O Connections

Programmable Function Input Connections

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each signal is software-selectable from any PFI when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for applications requiring alternative wiring.

You can individually enable each PFI pin to output a specific internal timing signal. For example, if you need the STARTSCAN* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/STARTSCAN* pin.

Caution Be careful not to externally drive a PFI signal when it is configured as an output.

In edge-detection mode, the minimum pulse width required is 10 ns. This setting applies for both rising-edge and falling-edge polarity settings. Edge-detect mode does not have a maximum pulse-width requirement.

In level-detection mode, the PFIs themselves do not impose a minimum or maximum pulse-width requirement, but the particular timing signal being controlled can impose limits. These requirements are listed later in this chapter.

DAQ Timing Connections

The DAQ timing signals are TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, SISOURCE, SCANCLK, and EXTSTROBE*.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-9. On the NI PCI-6110/6111, each STARTSCAN pulse initiates one CONVERT* pulse.

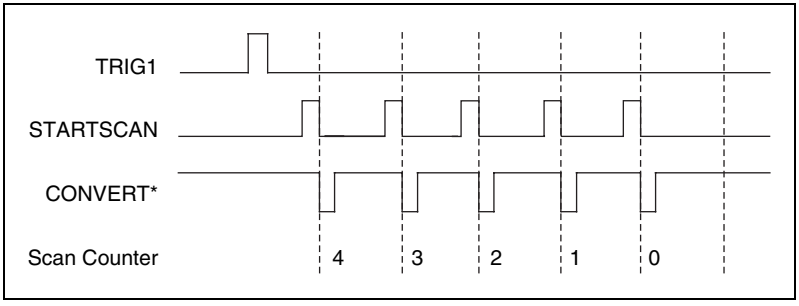


Figure 4-9. Typical Posttriggered Acquisition

Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-10 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures appears later in this chapter.

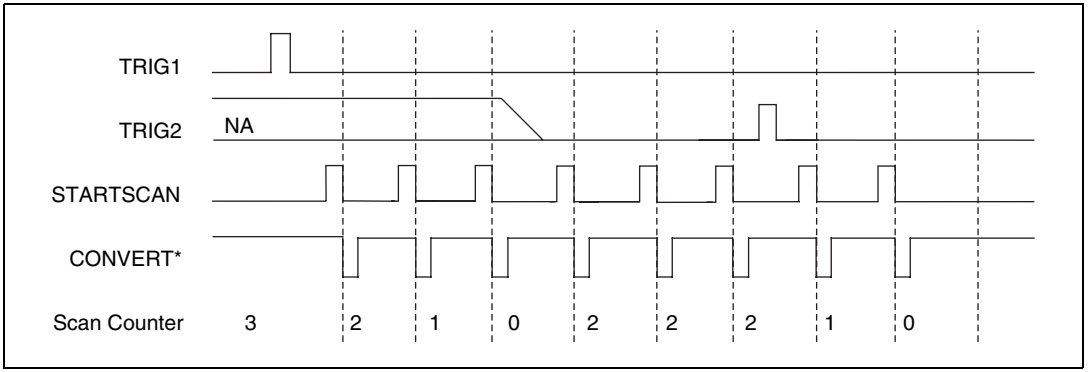


Figure 4-10. Typical Pretriggered Acquisition

TRIG1 Signal

Any PFI pin can receive as an input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-9 and 4-10 for the relationship of TRIG1 to the DAQ sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 starts the DAQ sequence for both posttriggered and pretriggered acquisitions. The NI PCI-6110/6111 supports analog triggering on the PFI0/TRIG1 pin. See Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, TRIG1 reflects the action that initiates a DAQ sequence even if another PFI is externally triggering the acquisition. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to high-impedance at startup.

Figures 4-11 and 4-12 show the timing requirements for TRIG1.

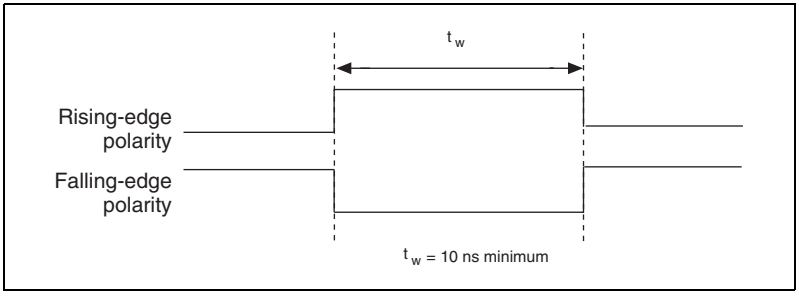


Figure 4-11. TRIG1 Input Signal Timing

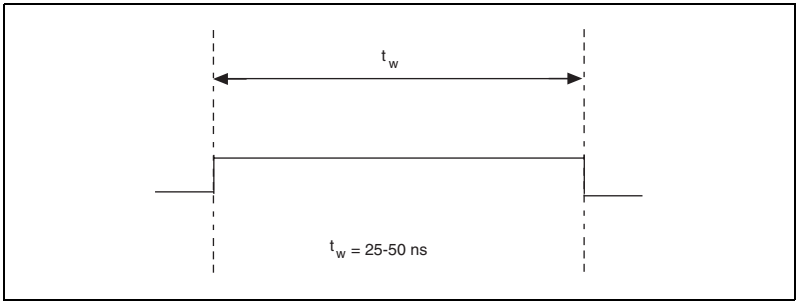


Figure 4-12. TRIG1 Output Signal Timing

The device also uses TRIG1 to initiate pretriggered DAQ operations. In most pretriggered applications, TRIG1 is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can receive as an input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-10 for the relationship of TRIG2 to the DAQ sequence.

As an input, TRIG2 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG2 initiates the posttriggered phase of a pretriggered DAQ sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter (SC) indicates the minimum number of scans before TRIG2 can be recognized. After the SC decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores TRIG2 if it is asserted prior to the SC decrementing to zero. After the selected edge of TRIG2 is received, the device acquires a fixed number

of scans and the acquisition stops. This mode acquires data both before and after receiving TRIG2.

As an output, TRIG2 reflects the posttrigger in a pretriggered acquisition sequence even if another PFI is externally triggering the acquisition. TRIG2 is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to high impedance at startup.

Figures 4-13 and 4-14 show the timing requirements for TRIG2.

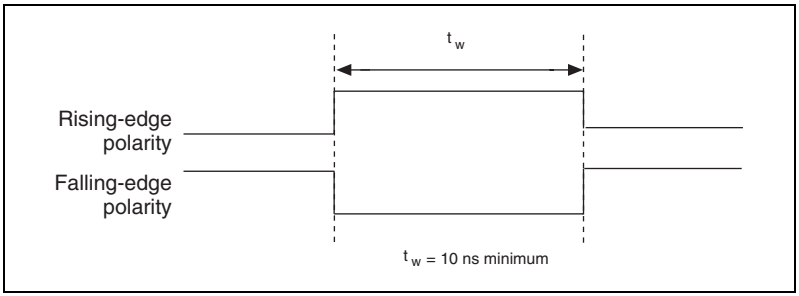


Figure 4-13. TRIG2 Input Signal Timing

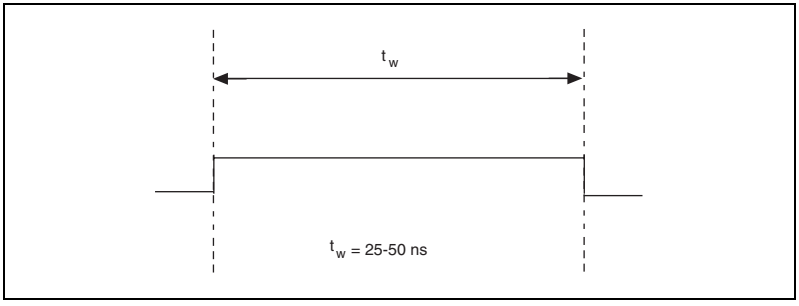


Figure 4-14. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can receive as an input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-9 and 4-10 for the relationship of STARTSCAN to the DAQ sequence.

As an input, STARTSCAN is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of STARTSCAN initiates a scan. The sample interval counter (SI2) starts if you select internally triggered CONVERT*.

As an output, STARTSCAN reflects the actual start pulse that initiates a scan even if another PFI is externally triggering the starts. You have two output options. The first is an active high pulse with a pulse width of 25 to 50 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN is deasserted t_{off} after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

Figures 4-15 and 4-16 show the input and output timing requirements for STARTSCAN.

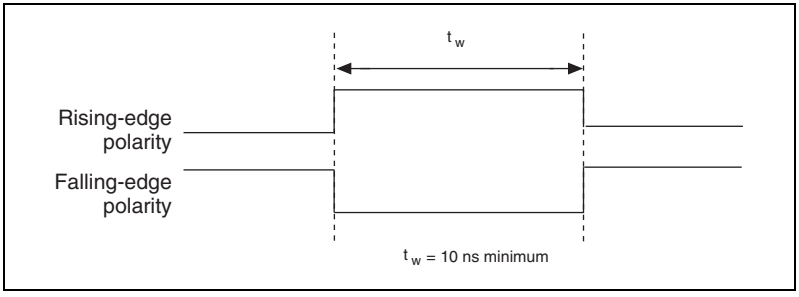


Figure 4-15. STARTSCAN Input Signal Timing

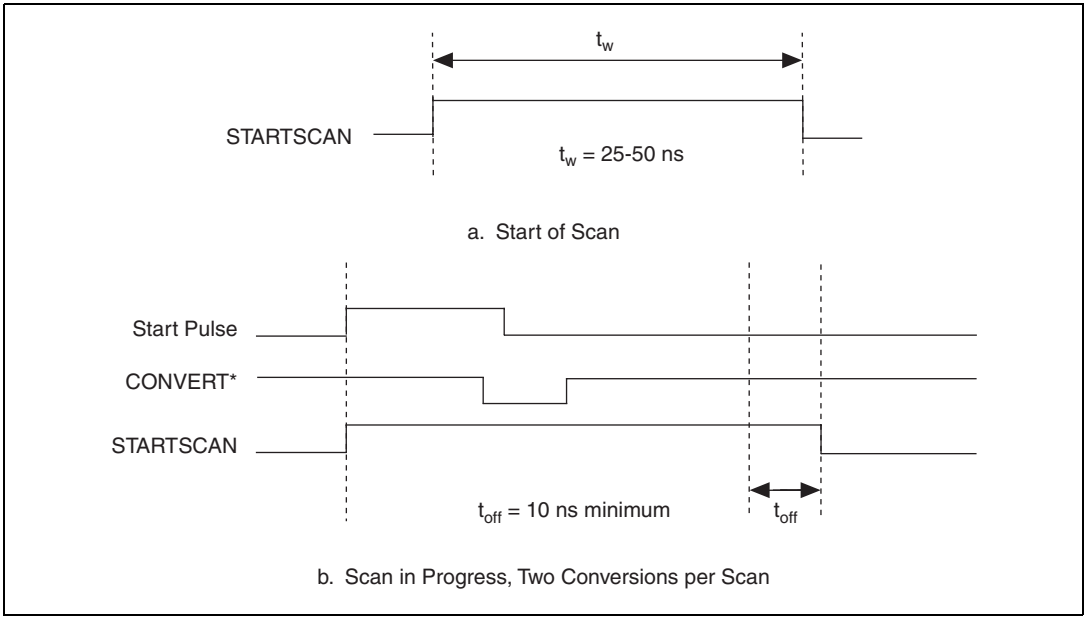


Figure 4-16. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* appears when SI2 reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on the NI PCI-6110/6111 device internally generates STARTSCAN unless you select some external source. This counter is started by the TRIG1 signal and is stopped by either software or the SC.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

The NI PCI-6110/6111 uses a three-point analog FIFO to digitize the input. Although the point is digitized on the appropriate edge of STARTSCAN (internally supplied unless you pass 0 for the scanTimebase), it is not sent to NI-DAQ until three additional edges of STARTSCAN clock the point. Consequently, you may not see the last three points of the acquisition. If you are performing an internally timed acquisition, NI-DAQ generates three extra points to clock the data for you. However, if you perform an

externally clocked acquisition, NI-DAQ does not know when the last point is taken, so you must provide the three extra pulses.

CONVERT* Signal

Any PFI pin can receive as an input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-9 and 4-10 for the relationship of CONVERT* to the DAQ sequence.

As an input, CONVERT* is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of CONVERT* initiates an A/D conversion.

As an output, CONVERT* reflects the actual convert pulse that is connected to the ADC, even if another PFI is externally generating the conversions. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-17 and 4-18 show the timing requirements for CONVERT*.

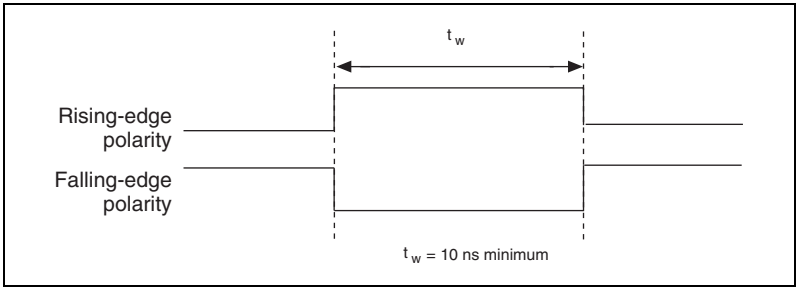


Figure 4-17. CONVERT* Input Signal Timing

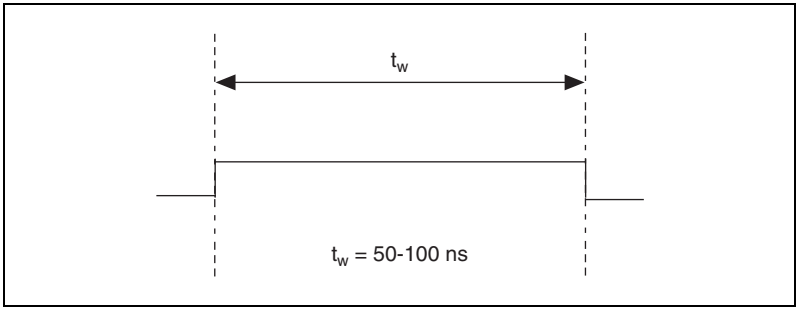


Figure 4-18. CONVERT* Output Signal Timing

The ADC switches to hold mode within 20 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next.

The SI2 on the NI PCI-6110/6111 normally generates CONVERT* unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can receive as an input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

AIGATE can neither stop a scan in progress nor continue a previously gated-off scan. Once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if

conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can receive as an input the SISOURCE signal, which is not available as an output on the I/O connector. The SI2 uses SISOURCE as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for SISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates SISOURCE unless you select some external source. Figure 4-19 shows the timing requirements for SISOURCE.

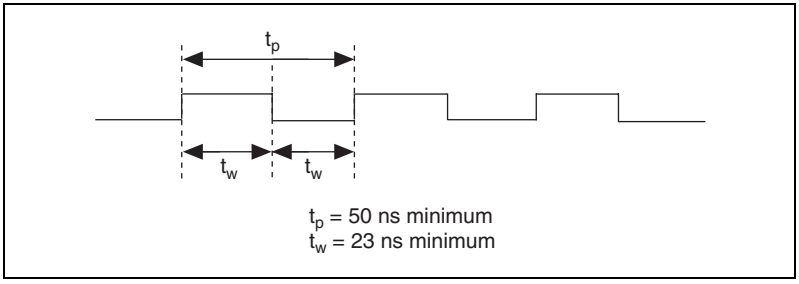


Figure 4-19. SISOURCE Signal Timing

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable, but it is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 450 ns pulse width and is software enabled.

Note SCANCLK polarity is low-to-high and cannot be changed programmatically using NI-DAQ.

Figure 4-20 shows the timing for SCANCLK.

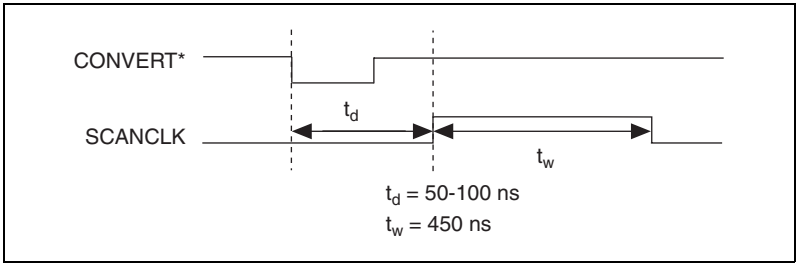


Figure 4-20. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of EXTSTROBE*. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode.

Note EXTSTROBE* cannot be enabled through NI-DAQ.

Figure 4-21 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

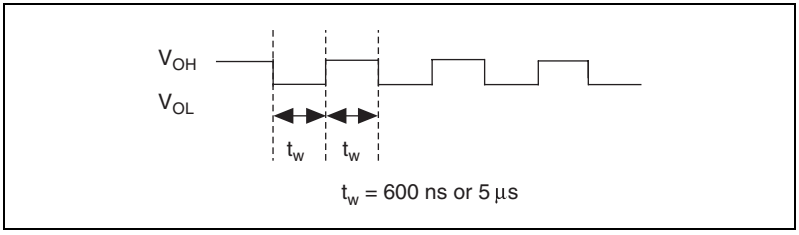


Figure 4-21. EXTSTROBE* Signal Timing

Waveform Generation Timing Connections

The analog group defined for the NI PCI-6110/6111 is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, WFTRIG is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of WFTRIG starts the waveform generation for the DACs. The update interval counter (UI) is started if you select internally generated UPDATE*.

As an output, WFTRIG reflects the trigger that initiates waveform generation, even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to high-impedance at startup.

Figures 4-22 and 4-23 show the timing requirements for WFTRIG.

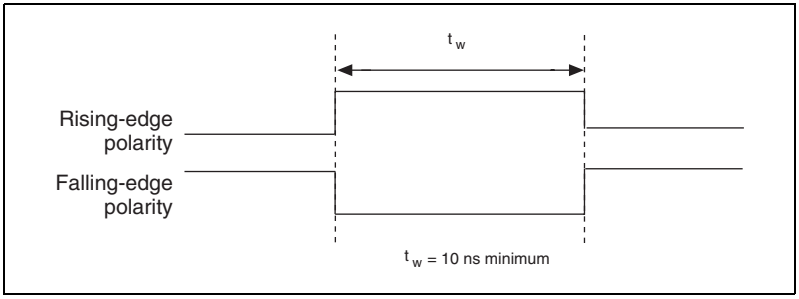


Figure 4-22. WFTRIG Input Signal Timing

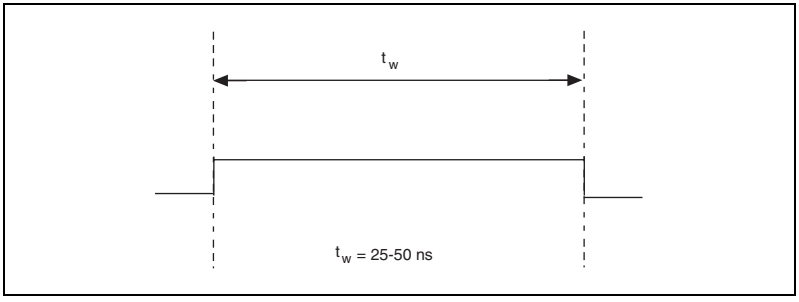


Figure 4-23. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, UPDATE* is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of UPDATE* updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, UPDATE* reflects the actual update pulse that is connected to the DACs, even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 75 ns. This output is set to high-impedance at startup.

Figures 4-24 and 4-25 show the timing requirements for UPDATE*.

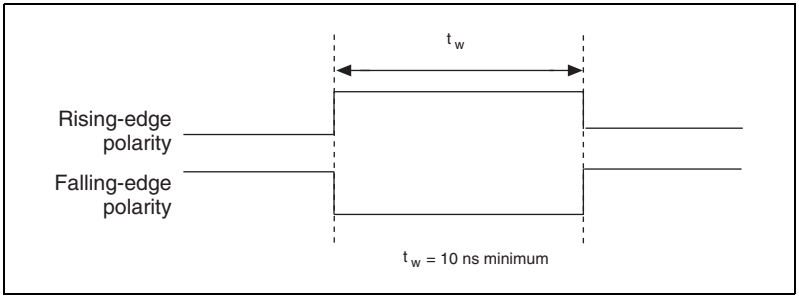


Figure 4-24. UPDATE* Input Signal Timing

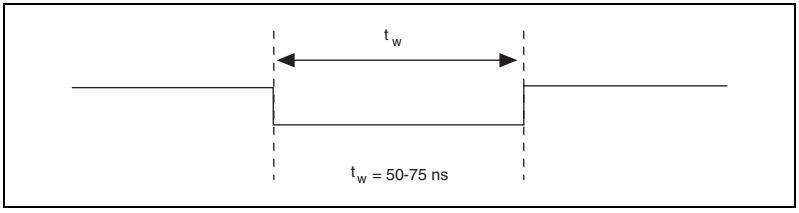


Figure 4-25. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The NI PCI-6110/6111UI normally generates UPDATE* unless you select some external source. The WFTRIG signal starts the UI, and the UI can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI uses UISOURCE as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for UISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

Figure 4-26 shows the timing requirements for the UISOURCE signal.

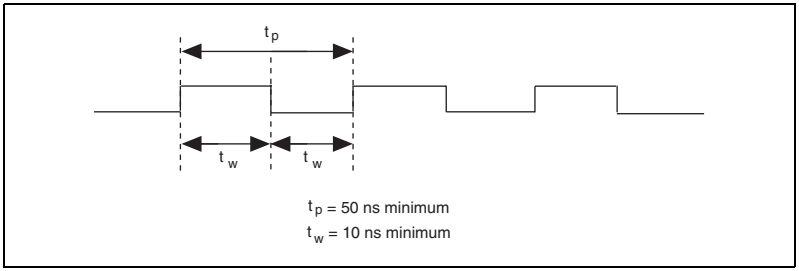


Figure 4-26. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, GPCTR0_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR0_SOURCE reflects the actual clock connected to general-purpose counter 0, even if another PFI is externally inputting the source clock. This output is set to high-impedance at startup.

Figure 4-27 shows the timing requirements for GPCTR0_SOURCE.

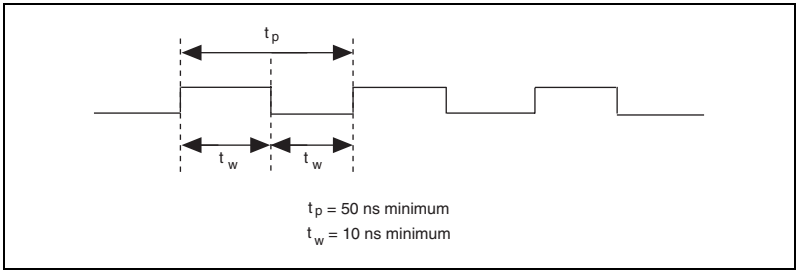


Figure 4-27. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, GPCTR0_GATE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR0_GATE reflects the actual gate signal connected to general-purpose counter 0, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-28 shows the timing requirements for the GPCTR0_GATE signal.

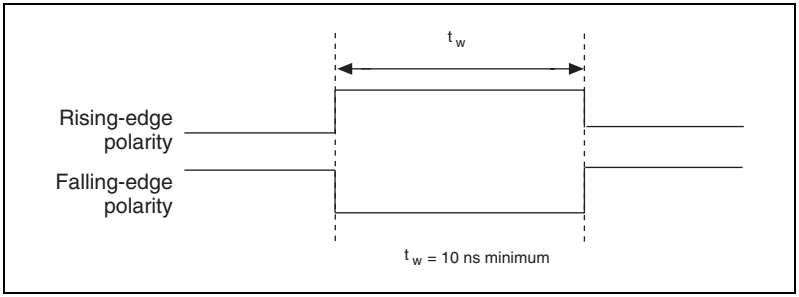


Figure 4-28. GPCTR0_GATE Signal Timing

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup. Figure 4-29 shows the timing of GPCTR0_OUT.

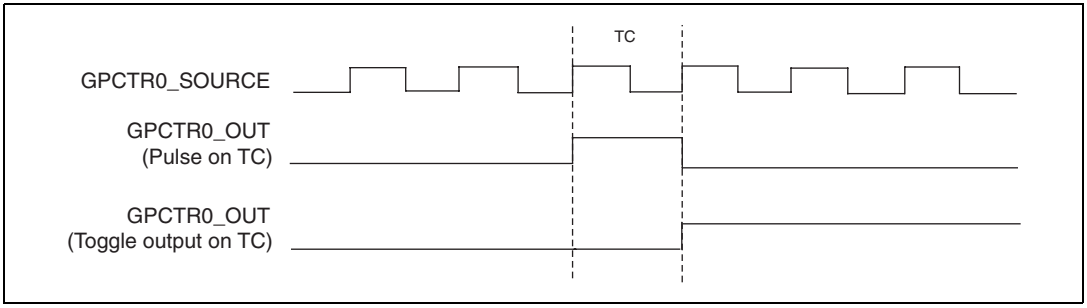


Figure 4-29. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and counts up when it is at a logic high. You can disable this input so that software controls the up-down functionality and leaves the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, GPCTR1_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if the source clock is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-30 shows the timing requirements for GPCTR1_SOURCE.

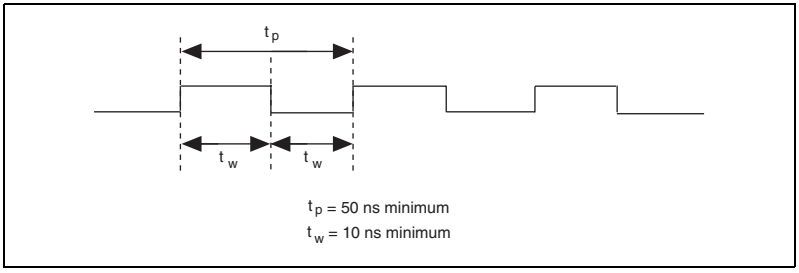


Figure 4-30. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, GPCTR1_GATE is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, GPCTR1_GATE monitors the actual gate signal connected to general-purpose counter 1, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-31 shows the timing requirements for the GPCTR1_GATE signal.

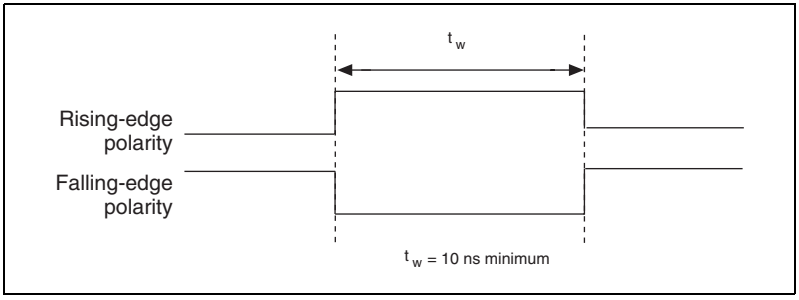


Figure 4-31. GPCTR1_GATE Signal Timing

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC of general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup. Figure 4-32 shows the timing requirements for GPCTR1_OUT.

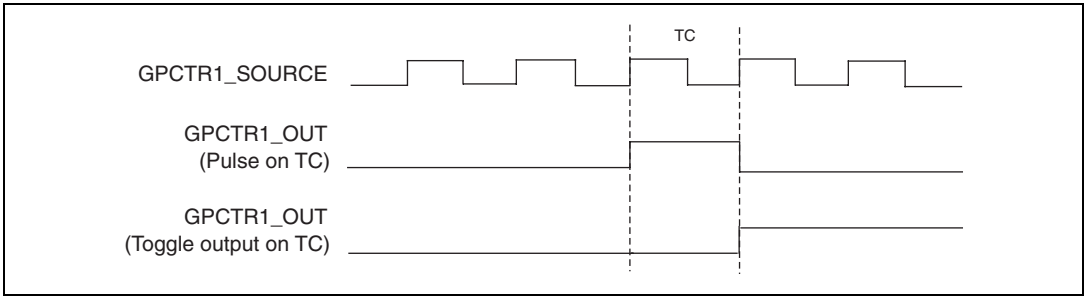


Figure 4-32. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use.

Figure 4-33 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the NI PCI-6110/6111 OUT output signals.

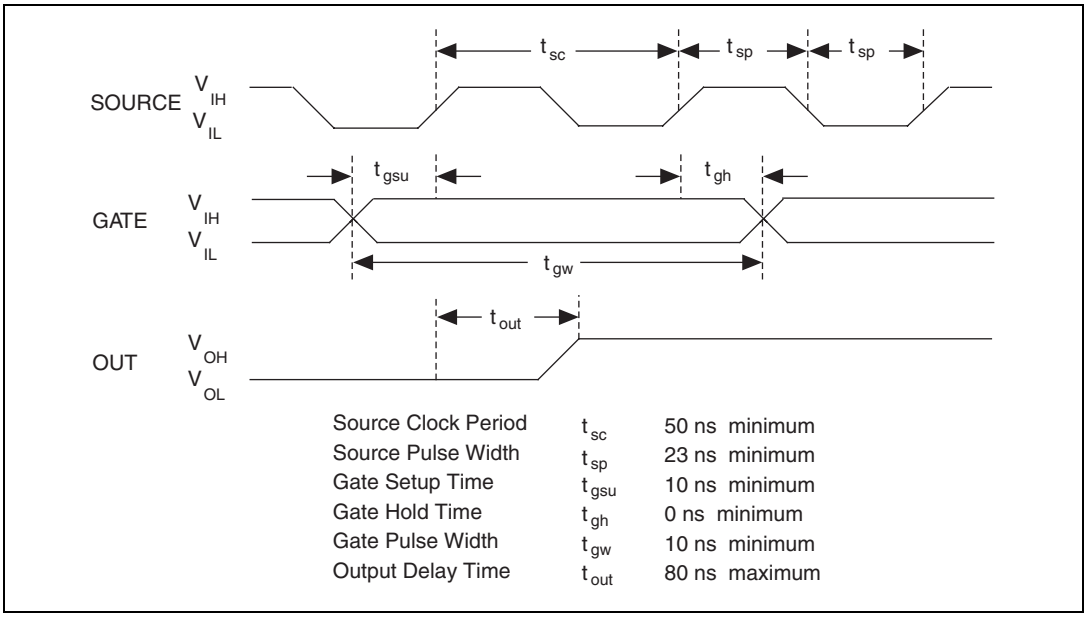


Figure 4-33. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-33 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, applies when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the NI PCI-6110/6111. Figure 4-33 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low)

for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-33. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the NI PCI-6110/6111. Figure 4-33 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The frequency generator for the NI PCI-6110/6111 outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software-selectable. This output is set to high-impedance at startup.

Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the NI PCI-6110/6111 if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to AI signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the ACH+ and ACH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground.

This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.

- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PCI DAQ system is the video monitor. Separate the monitor from the analog signals as far as possible.
- Separate the NI PCI-6110/6111 signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the NI PCI-6110/6111 signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals,* available at `ni.com/zone`.

5

Calibration

This chapter discusses the calibration procedures for the NI PCI-6110/6111. NI-DAQ includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the NI PCI-6110/6111, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Most applications require some form of device calibration. If you do not calibrate the device, the signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate; whereas, the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI PCI-6110/6111 is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can

vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it is used.

Self-Calibration

The NI PCI-6110/6111 can measure and correct for almost all of its calibration-related errors without any external signal connections. NI-DAQ provides a self-calibration method. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of offset, gain, and linearity drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

The NI PCI-6110/6111 has an onboard calibration reference to ensure the accuracy of self-calibration. The specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using the device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate the device.

An external calibration refers to calibrating the device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate the device by calling the NI-DAQ calibration function.

To externally calibrate the device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. For example, to calibrate a 16-bit device, the external reference should be at least ±0.001% (±10 ppm) accurate.

For a detailed calibration procedure for the NI PCI-6110/6111, click **Manual Calibration Procedures** at `ni.com/calibration`.

A

Specifications

This appendix lists the specifications of the NI PCI-6110/6111. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels

NI PCI-6110 ..... 4 pseudodifferential

NI PCI-6111 ..... 2 pseudodifferential

Type of ADC

Resolution ..... 12 bits, 1 in 4,096

Pipeline 3

Sampling rate

Maximum ..... 5 MS/s

Minimum ..... 1 kS/s

Input coupling ..... DC or AC

Max working voltage for all AI channels

Input Channels	Range	Maximum Working Voltage (Signal + Common Mode)
ACH<0..3>+	20 mV to 10 V 20 to 50 V	Should remain within ±11 V of ground Should remain within ±42 V of ground
ACH<0..3>–	All	Should remain within ±11 V of ground

Overvoltage protection ..... ±42 V

Inputs protected

Positive input ..... All channels

Negative input ..... All channels

FIFO buffer size.....8,192 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Scatter-gather (single transfer, demand transfer)

Accuracy Information

Refer to Table A-1.

Table A-1. NI PCI-6110/6111 Accuracy Information

Nominal Range (V)	Absolute Accuracy							Relative Accuracy	
	% of Reading			Offset (mV)	Noise + Quantization (mV)		Temp Drift	Resolution (mV)	
Full Scale	24 Hours	90 Days	1 Year		Single Pt.	Averaged	(%/°C)	Theoretical	Averaged
±50	0.51%	0.51%	0.51%	35 mV	51 mV	4.4 mV	0.0005%	24 mV	5.8 mV
±20	0.51%	0.51%	0.51%	20 mV	20 mV	1.8 mV	0.0005%	9.8 mV	2.3 mV
±10	0.11%	0.11%	0.11%	5.7 mV	10 mV	0.88 mV	0.0005%	4.9 mV	1.2 mV
±5	0.057%	0.058%	0.059%	3 mV	5.1 mV	0.44 mV	0.0005%	2.4 mV	0.58 mV
±2	0.057%	0.058%	0.059%	1.3 mV	2 mV	0.18 mV	0.0005%	0.98 mV	0.23 mV
±1	0.057%	0.058%	0.059%	0.7 mV	1 mV	0.088 mV	0.0005%	0.49 mV	0.12 mV
±0.5	0.057%	0.058%	0.059%	0.4 mV	0.67 mV	0.059 mV	0.0005%	0.24 mV	0.077 mV
±0.2	0.057%	0.058%	0.059%	0.2 mV	0.39 mV	0.035 mV	0.0005%	0.098 mV	0.046 mV

Note: Accuracies are valid for measurements following an internal calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature. One-year calibration interval recommended.

Transfer Characteristics

INL.....±0.5 LSB typ, ±1 LSB max

DNL .....±0.3 LSB typ, ±0.75 LSB max

Spurious free dynamic range (SFDR) ....Refer to Table A-2, *Analog Input Characteristics*

Effective number of bits (ENOB).....11.0 bits, DC to 100 kHz

Offset and gain error.....Refer to Table A-1, *NI PCI-6110/6111 Accuracy Information*

Amplifier Characteristics

Input impedance

ACH<0..3>+ to ACH<0..3>–

Normal powered on.....1 MΩ in parallel with 100 pF

Powered off .....1 MΩ minimum

Overload .....1 MΩ

Impedance to ground

ACH<0..3>– to ground .....10 nF

Input bias current .....±200 pA

Input offset current .....±100 pA

CMRR.....Refer to Table A-2, *Analog Input Characteristics*

Dynamic Characteristics

Interchannel skew .....1 ns typ
f_{in} = 100 kHz
input range = ±10 V

Bandwidth

Range	Small Signal (–3 dB)
200 mV	4 MHz
500 mV to 50 V	5 MHz

Note Bandwidth specifications are for signals on the (+) input with the (–) input at DC ground. The (–) input is slew rate limited to 24 V/µsec and has an additional 10 nF capacitance to ground.

System noise ..... See Table A-2, *Analog Input Characteristics*

Crosstalk..... –80 dB, DC to 100 kHz

Table A-2. Analog Input Characteristics

Input Range	Bandwidth (MHz)[1]	SFDR Typ (dB)[2]	SFDR Max (dB)[3]	CMRR (dB)[4]	System Noise (LSB_{rms})[5]
±50 V	5.5	78	70	34	0.5
±20 V	4.4	78	70	40	0.5
±10 V	7.2	81	75	46	0.5
±5 V	4.8	81	75	52	0.5
±2 V	4.8	85	75	60	0.5
±1 V	4.4	85	75	66	0.5
±500 mV	4.4	85	75	70	0.6
±200 mV	4.1	81	70	72	1.0

[1] –3 dB frequency for input amplitude at 96% of the input range (–0.3 dB)
[2] Measured at 100 kHz
[3] 100% production tested at 100 kHz
[4] All input ranges, DC to 60 Hz
[5] LSB_{rms}, not including quantization

Stability

Recommended warm-up time ..... 15 minutes

Offset temperature coefficient

Pregain ..... ±5 µV/°C

Postgain..... ±50 µV/°C

Gain temperature coefficient..... ±20 ppm/°C

Onboard calibration reference

Level.....5.000 V (±2.5 mV)
(actual value stored in EEPROM)

Temperature coefficient.....±0.6 ppm/°C max

Long-term stability.....±6 ppm/$\sqrt{1,000\ h}$

Analog Output

Output Characteristics

Number of channels.....2 voltage

Resolution.....16 bits, 1 in 65,536

Max update rate

1 channel.....4 MS/s, system dependent

2 channel.....2.5 MS/s, system dependent

FIFO buffer size.....2,048 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes.....Scatter gather (single transfer, demand transfer)

Transfer Characteristics

Relative accuracy (INL).....±4 LSB typ, ±8 LSB max

DNL.....±2 LSB typ, ±8 LSB max

Offset error.....±5.0 mV max

Gain error
(relative to internal reference).....±0.1% of output range max

Table A-3. NI PCI-6110/6111 Analog Output DC Accuracy Information

Nominal Range (V)	Absolute Accuracy				
	% of Reading		Offset (mV)	Temp Drift (%/°C)	Absolute Accuracy at Full Scale (±mV)
	24 Hrs	1 Year			
±10	0.018	0.022	5.933	0.0005	8.133
Note: Temp Drift applies only if ambient is greater than ±10 °C of previous external calibration.					

Voltage Output

Ranges ..... ±10 V

Output coupling ..... DC

Output impedance ..... 50 Ω, ±5%

Short circuit current ..... ±27 mA, typ

Current drive ..... ±5 mA min

Output stability ..... Any passive load

Protection ..... Short-circuit to ground

Power-on output voltage ..... ±400 mV (before software loads calibration values)

Dynamic Characteristics

Settling time and slew rate

Settling Time for Full-Scale Step	Slew Rate
300 ns to ±0.01%	300 V/µs

Noise ..... 1 mV_{rms}, DC to 5 MHz

Spurious free dynamic range ..... 75 dB, DC to 10 kHz

Glitch energy ..... ±30 mV for 1 µs

Stability

Offset temperature coefficient .....±500 µV/°C

Gain temperature coefficient

Internal reference.....±50 ppm/°C

External reference.....±25 ppm/°C

Onboard calibration reference

Level .....5.000 V (±2.5 mV)
(actual value stored in EEPROM)

Temperature coefficient.....±0.6 ppm/°C max

Long-term stability .....±6 ppm/$\sqrt{1,000\ \text{h}}$

Digital I/O

Number of channels.....8 input/output

Compatibility .....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0.0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state .....Input (high-impedance)

Data transfers.....Programmed I/O

Timing I/O

General-Purpose Up/Down Counter/Timers

Number of channels 2

Resolution ..... 24 bits

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Minimum	Maximum
Input low voltage Input high voltage	0 V 2 V	0.8 V 5 V
Input low current (V_{in}= 0 V) Input high current (V_{in} = 5 V)	— —	–320 µA 10 µA
Output low voltage (IOL = 24 mA) Output high voltage (IOH = 13 mA)	— 4.35 V	0.4 V —

Base clocks available ..... 20 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration ..... 10 ns, edge-detect mode

Min gate pulse duration ..... 10 ns, edge-detect mode

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather (single transfer, demand transfer)

Frequency Scaler

Number of channels 1

Resolution ..... 4 bits, 1 in 16

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Minimum	Maximum
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Output low voltage (I_{out}= 5 mA)	—	0.4 V
Output low voltage (I_{out} = 3.5 mA)	4.35 V	—

Base clocks available.....10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Data transfers.....DMA, interrupts, programmed I/O

Triggers

Analog Trigger

Number of triggers.....1

Purpose

- Analog input.....Start and stop trigger, gate, clock
- Analog output.....Start trigger, gate, clock
- General-purpose counter/timers.....Source, gate

Source.....ACH<0..3>, external trigger (PFI0/TRIG1)

Level

- Internal source, ACH<0..3>.....± Full-scale
- External source, PFI0/TRIG1.....±10 V, external

Slope.....Positive or negative (software-selectable)

Resolution.....8 bits, 1 in 256

Hysteresis.....Programmable

Bandwidth (–3 dB)

- Internal source, ACH<0..3>.....5 MHz
- External source, PFI0/TRIG1.....5 MHz

Digital Trigger

Number of triggers 2

Purpose

- Analog input ..... Start and stop trigger, gate, clock
- Analog output ..... Start trigger, gate, clock
- General-purpose counter/timers..... Source, gate

Source..... <PFI0..PFI9>, <RTSI0..RTSI6>

Slope..... Positive or negative (software-selectable)

Compatibility ..... 5 V/TTL

Response ..... Rising or falling edge

Pulse width..... 10 ns min

External Input for Digital or Analog Trigger (PFI0/TRIG1)

Output impedance ..... 10 kΩ

Source impedance (recommended)..... 1 kΩ

Coupling..... DC or AC

Protection

- Digital trigger..... –0.5 V to (V_{cc} + 0.5) V
- Analog trigger
  - On/disabled..... ±35 V
  - Powered off..... ±35 V

RTSI

Trigger Lines..... 7

Bus Interface

Type ..... Master, slave

Power Requirement

+5 VDC (±5%)

NI PCI-6110 .....2.5 A

NI PCI-6111 .....2.0 A

Power available at I/O connector.....+4.65 to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors) .....31.2 by 10.6 cm
(12.3 by 4.2 in)

I/O connector .....68-pin male SCSI-II type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth .....±10 V, installation category I

Channel-to-channel.....±10 V, installation category I

Environmental

Operating temperature .....0 to 45 °C

Storage temperature .....–20 to 70 °C

Humidity .....5 to 90% RH, noncondensing

Maximum altitude.....2000 meters

Pollution degree (indoor use only) 2

Safety

The NI PCI-6110/6111 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3111-1:1994
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions..... EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity..... Evaluated to EN 61326:1997/
A1:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by the product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

B

Cable Connector Descriptions

This appendix describes the cable connectors on the NI PCI-6110/6111.

Figure B-1 shows the pin assignments for the 68-pin NI PCI-6110/6111 connector. This connector is available when you use the SH6868EP cable assemblies with the NI PCI-6110/6111.

Figure B-2 shows the pin assignments for the NI PCI-6110/6111 when used with 50-pin accessories.

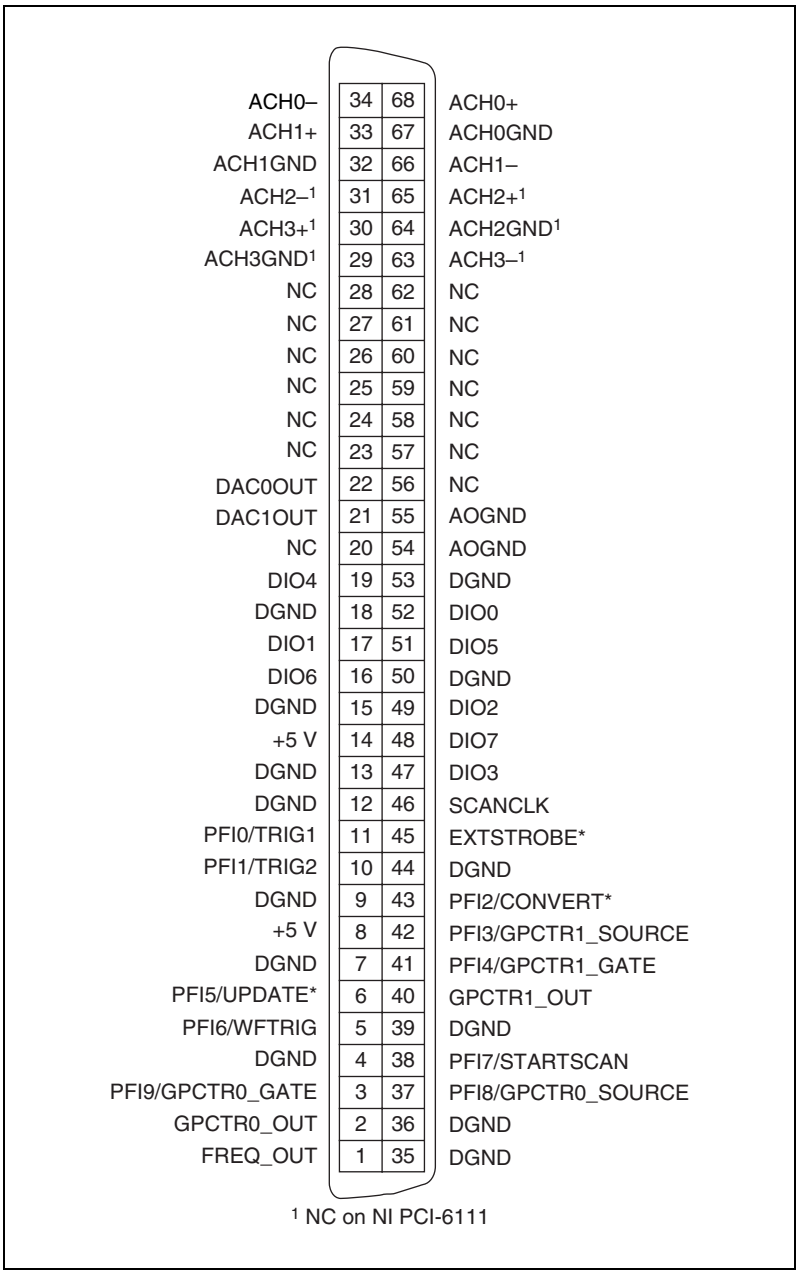


Figure B-1. 68-Pin Connector Pin Assignment for the NI PCI-6110/6111

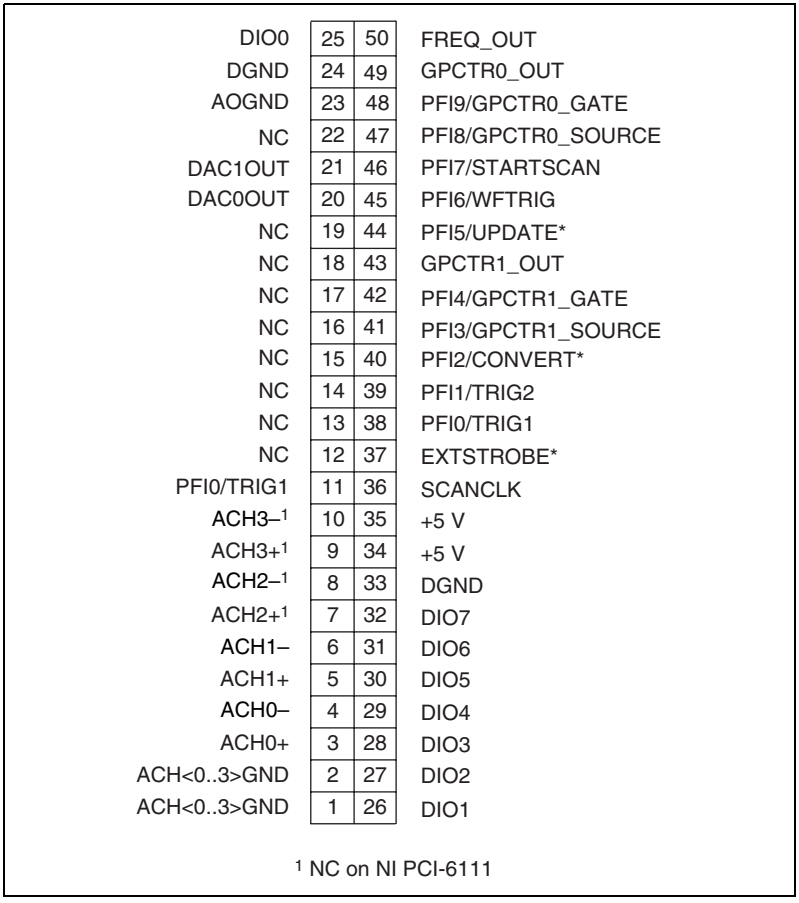


Figure B-2. 50-Pin Connector Pin Assignment for the NI PCI-6110/6111

C

Common Questions

This appendix contains a list of commonly asked questions and answers relating to usage and special features of the NI PCI-6110/6111.

General Information

What is the NI PCI-6110/6111?

The NI PCI-6110/6111 is a switchless and jumperless enhanced Multifunction DAQ device that uses the DAQ-STC for timing.

What is the DAQ-STC?

The DAQ-STC is the system timing control application-specific integrated circuit (ASIC) designed by NI and is the backbone of the NI PCI-6110/6111. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- AI—two 24-bit, two 16-bit counters
- AO—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamless changes to the sampling rate are possible.

What does the maximum sampling rate mean to me?

Sampling rate is the fastest you can acquire data on the device and still achieve accurate results. The NI PCI-6110/6111 has a sampling rate of 5 MS/s. This sampling rate is at 5 MS/s regardless if 1 or 4 channels are acquiring data.

What type of 5 V protection does the NI PCI-6110/6111 have?

The NI PCI-6110/6111 has 5 V lines equipped with a self-resetting 1 A fuse.

How do I use the NI PCI-6110/6111 with the NI-DAQ C API?

The *NI-DAQ User Manual for PC Compatibles* describes the general programming flow and provides example code for using the NI-DAQ API. For a list of functions that support the NI PCI-6110/6111, you can refer to the *NI-DAQ Function Reference Help* (for NI-DAQ version 6.7 or later) or the *NI-DAQ Function Reference Manual* (for NI-DAQ version 6.6 or earlier).

Installing and Configuring

How do you set the base address for the NI PCI-6110/6111?

The base address of the NI PCI-6110/6111 is assigned automatically through the PCI bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring the NI PCI-6110/6111?

The NI PCI-6110/6111 is jumperless and switchless.

Which NI document should I read first to get started using DAQ software?

The *DAQ Quick Start Guide* and the NI-DAQ or application software release notes documentation are good places to start. Refer to `ni.com/manuals` to download these documents.

What is the best way to test the NI PCI-6110/6111 without programming the device?

If you are using Windows, Measurement and Automation Explorer (MAX) has a test panel option that is available by selecting **Devices and Interfaces** in the left-hand panel and then selecting the NI PCI-6110/6111. The test panels are excellent tools for performing simple functional tests of the device, such as AI, DIO, and counter/timer tests. If you are using Mac OS, the NI-DAQ Configuration Utility provides the same functionality as MAX.

Analog Input and Output

Why is there a minimum sampling rate on the NI PCI-6110/6111?

The NI PCI-6110/6111 makes use of a pipelined ADC in order to achieve its high sampling rates. Sampling at rates below 20 kS/s can result in improper digitalization, which would appear as noise in the acquired data.

I connected a DIFF input signal, but the readings are random and drift rapidly. What's wrong?

Check the ground reference connections. The signal may be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Connecting Signals*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a low-pass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal.

Can I synchronize a one-channel AI data acquisition with a one-channel AO waveform generation on the NI PCI-6110/6111?

Yes. One way to accomplish this is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps 1 through 4 below, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke Route Signal.vi with signal name set to PFI5 and signal source set to AO Update.

2. Set up acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_SCAN_START, ND_PFI_5, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke AI Clock Config.vi with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate AI data acquisition, which starts only when the AO waveform generation starts.
4. Initiate AO waveform generation.

Timing and Digital I/O

What types of triggering can be hardware-implemented on the NI PCI-6110/6111?

Hardware digital and analog triggering are both supported on the NI PCI-6110/6111.

What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO devices have a 20 MHz timebase. The Am9513-based MIO devices have a 1 MHz or 5 MHz timebase.

Do the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some applications that were built using the CTR VIs still run. However, there are many differences between the counters of the NI PCI-6110/6111 and those of other devices: the counter numbers are different, timebase selections are different, and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using NI-DAQ or Measurement Studio, the counter/timer applications that you wrote previously do not work with the DAQ-STC. You must use the GPCTR functions because ICTR and CTR functions do not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must first rewrite the application using GPCTR function calls.

I'm using one of the general-purpose counter/timers on the NI PCI-6110/6111, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using NI-DAQ or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are high-impedance.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to almost all internal timing signals.

If you are using NI-DAQ or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, and Counter Set Attribute advanced-level VIs to indicate which function the connected signal serves. Use the Route Signal VI to enable the PFI lines to output internal signals.

Table C-1. Signal Name Equivalencies

Hardware Signal Name	LabVIEW Route Signal	NI-DAQ Select_Signal
AIGATE	—	ND_IN_EXTERNAL_GATE
AOGATE	—	ND_OUT_EXTERNAL_GATE
CONVERT*	AI Convert	ND_IN_CONVERT
SISOURCE	—	ND_IN_SCAN_CLOCK_TIMEBASE
STARTSCAN	AI Scan Start	ND_IN_SCAN_START
TRIG1	AI Start Trigger	ND_IN_START_TRIGGER
TRIG2	AI Stop Trigger	ND_IN_STOP_TRIGGER
UISOURCE	—	ND_OUT_UPDATE_CLOCK_TIMEBASE
UPDATE*	AO Update	ND_OUT_UPDATE
WFTRIG	AO Start Trigger	ND_OUT_START_TRIGGER

Caution If you enable a PFI line for output, do *not* connect any external signal source to it. Connecting external signals to enabled PFI lines can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high-impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-3, *I/O Signal Summary for the NI PCI-6110/6111*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) is in the high impedance state after power-on, and Table 4-3 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor sets the DIO(0) pin to a logic high when the output is in a high-impedance state.

D

Technical Support and Professional Services

Visit the following sections of the NI Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
- **Training**—Visit ni.com/custed for self-paced tutorials, videos, and interactive CDs. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, NI Alliance Program members can help. To learn more, call your local NI office or visit ni.com/alliance.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

°	degrees
>	greater than
≥	greater than or equal to
<	less than
≤	less than or equal to
/	per
%	percent
±	plus or minus
+	positive of, or plus
–	negative of, or minus
Ω	ohms

$\sqrt{}$	square root of
+5 V	+5 VDC source signal

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ACH	analog input channel signal
ACH0GND	analog input channel ground signal
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADE	application development environment
AI	analog input
AIGATE	analog input gate signal
AIGND	analog input ground signal
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions

B

bipolar	a signal range that includes both positive and negative values (for example, –5 V to +5 V)

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
channel rate	reciprocal of the interchannel delay
cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
common-mode noise	unwanted signals that appear in equal phase and amplitude on both the inverting and noninverting input in a differential measurement system. Ideally, but not completely in practice, the measurement device ignores this noise, because the measurement device is designed to respond to the difference between the inverting and noninverting inputs.
common-mode range	the input range over which a circuit can handle a common-mode signal
common-mode signal	the mathematical average voltage, relative to the ground of the computer, of the signals from a differential input
common-mode voltage	any voltage present at both instrumentation amplifier inputs with respect to amplifier ground
CONVERT*	convert signal
counter/timer	a circuit that counts external pulses or clock pulses (timing)
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 voltage output signal
DAC1OUT	analog channel 1 voltage output signal
DAQ	data acquisition—a system that uses the computer to collect, receive, and generate electrical signals
DAQ-STC	data acquisition system timing controller—an application-specific integrated circuit (ASIC) for the system timing requirements of a general A/D and D/A system
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DI	digital input
DIFF	differential mode
DIO	digital input/output
DIP	dual inline package
dithering	the addition of Gaussian noise to an analog input signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output

DOC	the Canadian Department of Communications
DoC	Declaration of Conformity

E

edge detection	a technique that locates an edge of an analog signal, such as the edge of a square wave
EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EMC	electromechanical compliance
ENOB	effective number of bits—a measure of the actual performance of an A/D converter after its various noise sources and nonlinearities are included. The ENOB is computed as the signal-to-noise ratio of the A/D converter (in dB) minus 1.76, divided by 6.02. Also called effective bits.
ESD	electrostatic discharge—a high-voltage, low-current discharge of static electricity that can damage sensitive electronic components. Electrostatic discharge voltage can easily range from 1,000 to 10,000 V.
EXTSTROBE	external strobe signal

F

F	farads
FCC	Federal Communications Commission

FIFO	first-in first-out memory buffer—FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be read or written. For example, an analog input FIFO stores the results of A/D conversions until the data can be read into system memory. Programming the DMA controller and servicing interrupts can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored in the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
FREQ_OUT	frequency output signal
ft	feet

G

gain	the factor by which a signal is amplified, sometimes expressed in decibels
GATE	gate signal
GPCTR	general-purpose counter signal
GPCTR0_GATE	general-purpose counter 0 gate signal
GPCTR0_OUT	general-purpose counter 0 output signal
GPCTR0_SOURCE	general-purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general-purpose counter 0 up down signal
GPCTR1_GATE	general-purpose counter 1 gate signal
GPCTR1_OUT	general-purpose counter 1 output signal
GPCTR1_SOURCE	general-purpose counter 1 clock source signal

GPCTR1_UP_DOWN	general-purpose counter 1 up down signal
ground	an electrically neutral wire that has the same potential as the surrounding earth; a common reference point for an electrical system

H

h	hour
hex	hexadecimal
Hz	hertz

I

ICTR	8253 Programmable Interval Timer—applies to legacy DAQ products, such as the 1200 series
INL	integral nonlinearity—for an ADC, deviation of codes of the actual transfer function from a straight line
interchannel delay	amount of time that passes between sampling consecutive channels. The interchannel delay must be short enough to allow sampling of all the channels in the channel list, within the scan interval. The greater the interchannel delay, the more time the PGIA is allowed to settle before the next channel is sampled. The interchannel delay is regulated by CONVERT*.
I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high
I_{OL}	current, output low
I_{OUT}	current out
IRQ	interrupt request

K

kHz	kilohertz

L

LabVIEW	a graphical programming language
LED	light emitting diode
library	a file containing compiled object modules, each comprised of one of more functions, that can be linked to other object modules that make use of these functions. NIDAQ32.LIB is a library that contains NI-DAQ functions. The NI-DAQ function set is broken down into object modules so that only the object modules that are relevant to your application are linked in, while those object modules that are not relevant are not linked.
linearity	the adherence of device response to the equation R = KS, where R = response, S = stimulus, and K = a constant
LSB	least significant bit

M

m	meter
MB	megabytes of memory
Measurement & Automation Explorer (MAX)	a controlled centralized configuration environment that allows you to configure all of your National Instruments DAQ, GPIB, IMAQ, IVI, Motion, VISA, and VXI devices
MHz	megahertz
MIO	multifunction I/O
MITE	MXI Interface to Everything
MSB	most significant bit

mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel
mV	millivolts

N

NC	not connected
NI	National Instruments
NI-DAQ	National Instruments driver software for DAQ hardware
noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.
pd	pull-down
PFI	Programmable Function Input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2

PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_SOURCE	PFI3/general-purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general-purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_SOURCE	PFI8/general-purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general-purpose counter 0 gate
PGIA	Programmable Gain Instrumentation Amplifier
Plug and Play devices	devices that do not require DIP switches or jumpers to configure resources on the devices—also called switchless devices
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output
posttriggering	the technique used on a DAQ device to acquire a programmed number of samples after trigger conditions are met
potentiometer	an electrical device the resistance of which can be manually adjusted; used for manual adjustment of electrical circuits and as a transducer for linear or rotary position
ppm	parts per million
precision	the measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal
pretriggering	the technique used on a DAQ device to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition
pseudodifferential input	pseudodifferential input channels are all referred to a common ground, but this ground is not directly connected to the computer ground
pu	pull up

R

RAM	random access memory
range	the maximum and minimum parameters between which a sensor, instrument, or device operates with a specified set of characteristics
referenced signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground. Also called grounded signal sources.
resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
RH	relative humidity
rms	root mean square
RTD	resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI bus	real-time system integration bus—the National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise timing synchronization between multiple devices
RTSI_OSC	RTSI Oscillator—RTSI bus master clock

S

s	seconds
S	samples
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
SC	scan counter
scan interval	controls how often a scan is initialized; the scan interval is regulated by STARTSCAN

scan rate	reciprocal of the scan interval
SCANCLK	scan clock signal
SCSI	small computer system interface—a high-speed, peripheral-connect interface primarily used for hard disks, CD-ROM drives, tape drives, and other mass-storage devices to PCs
settling time	the amount of time required for a voltage to reach its final value within specified limits
SFDR	spurious-free dynamic range—the dynamic range from full-scale deflection to the highest spurious signal in the frequency domain
SI2	sample interval counter
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
SOURCE	source signal
STARTSCAN	start scan signal
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count—the ending value of a counter
t_d	delay time
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
t_{out}	output delay time
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage

thermocouple	a temperature sensor created by joining two dissimilar metals; the junction produces a small voltage as a function of the temperature
TIO	timing I/O
t_{off}	an offset (delayed) pulse; the offset is t nanoseconds from the falling edge of the CONVERT* signal
t_{out}	output delay time
t_P	pulse period
TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic
t_w	pulse width

U

UI	update interval counter
UISOURCE	update interval counter clock signal
unipolar	a signal range that is always positive (for example, 0 to +10 V)
UPDATE	update signal

V

V	volts
VDC	volts direct current
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program

V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
V_{rms}	volts, root mean square
V_s	ground-referenced signal source

W

WFTRIG	waveform generation trigger signal

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